Research Article

Simulation of an Improved Design for n-Electrode with Holes for Thin-GaN Light-Emitting Diodes

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A novel design is proposed for n-electrode with holes to be applied in Thin-GaN light-emitting diodes (LEDs). The influence of the n-electrode with holes on the thermal and electrical characteristics of a Thin-GaN LED chip is investigated using a three-dimensional numerical simulation. The variations in current density and temperature distributions in the active layer of n-electrodes both with and without holes are very tiny. The percentages of light output from these holes are 29.8% and 38.5% for cases with 5 μm holes and 10 μm holes, respectively; the side length of the n-electrode (L) is 200 μm . Furthermore, the percentage increases with the size of the n-electrode. Thus, the light output can be increased 2.45 times using the n-electrode with holes design. The wall-plug efficiency (WPE) can also be improved from 2.3% to 5.7%. The most appropriate n-electrode and hole sizes are determined by WPE analysis.

1. Introduction

Light-emitting diodes have many advantages over conventional light sources, such as their narrow spectrum, long lifetime, and good mechanical stability [1, 2]. High-brightness LEDs have been proven to have excellent abilities to function in back and general lighting applications [3]. There are two major methods that can be used to increase the light output of an LED chip: enlarging the area of a single LED chip or manufacturing a monolithic LED chip array [4, 5]. When the area of an LED chip is enlarged, it results in an increase in the input current and the heat dissipation. Several methods have been developed to improve the current distribution and heat transfer in LED chips by means of altering the design of the electrode pattern and the geometry of the structure [6–9]. The Thin-GaN LED has also been demonstrated to have great potential for high-power illumination usage [8, 10–12]. The better current spreading and superior heat dissipation of the Thin-GaN LED allow it to operate under higher power conditions. A better design for the electrode pattern can increase the light-emitting ratio and decrease the thermal burden in the Thin-GaN LED [1]. The current distribution in an LED chip is usually estimated from the light output [8, 10] and is affected by the material properties of the chip, as well as

the size and pattern of the electrode [8, 10–12]. The current crowding effect can be improved by the insertion of the current blocking layer (CBL) in the epitaxial structure of the Thin-GaN LED [8]. Many different LED chip structures have been designed and fabricated in the search for superior LED performance [1, 4, 8, 13]. Several studies have investigated the fabrication and performance of blue/near-UV LEDs composed of an array of nanowires on a p- or n-GaN thin film substrate [14–16]. The problem is that the mass fabrication procedure for LEDs is expensive and time consuming.

Several numerical models have been proposed to explain the phenomenon of current spreading and to find possible ways to obtain better device geometry for LEDs [1, 5, 9, 17–19]. Tu et al. improved the design of the n-electrode patterns to obtain more uniform current spreading [1]. Hwang and Shim [20] developed a three-dimensional numerical simulation model, based on the concept of series and parallel connections, with which to investigate current spreading in an LED. The continuity equation for electronic transport can be used in three-dimensional models to simulate the electric potential and current in lateral-injection LED chips. This has proven to be much more economical than other methods [9, 17]. Using this approach, the simulation of complex LED structures

becomes possible. The influence of the thermal effect on the performance of the LED has been considered in some studies [8, 10, 11, 13, 20, 21]. In our previous study, a numerical model, which considered the thermal effect, was proposed for simulating a vertical LED chip [22]. The simulation results for different areas of the n-electrode and the influence of CBL were discussed. The results were found to be consistent with the experimental results obtained in the study of Kim et al. [8].

The main problem with Thin-GaN LEDs is the shadowing effect of the n-electrode when current crowding under the n-electrode is serious. Recently, a novel n-electrode with holes has been manufactured with wet etching technology to solve this problem. In the present study, we modify the 3D numerical model developed in our previous work [22] to simulate the influence of the n-electrode with holes. This method is used to investigate the thermal and electrical characteristics of Thin-GaN LED chips operating under high-power conditions. The effects of the hole size are considered. In addition, the wall-plug efficiency (WPE) is also discussed in our numerical model.

2. Numerical Simulation

A Thin-GaN LED chip is analyzed in the present study. A schematic representation of a cross section in the lateral direction is shown in Figure 1. The full chip dimensions are $600 \times 600 \mu\text{m}^2$. The thicknesses of the n-type GaN layer, active layer, and p-type GaN layer are 2.5, 0.07, and $0.07 \mu\text{m}$, respectively. A p-type electrode is formed by the application of a $0.93 \mu\text{m}$ thick Ag/Ni/Au metalized layer to the entire wafer ($600 \times 600 \mu\text{m}^2$). The n-type electrode is formed by the application of a $0.7 \mu\text{m}$ thick Ti/Au metalized layer with various square dimensions and different widths ($L = 100, 200, 300, 400, 500, \text{ and } 600 \mu\text{m}$).

The continuity equation for electronic transport in an LED chip is

$$\nabla \cdot (\sigma \nabla V) = 0, \quad (1)$$

where σ is the conductivity and V is the electrical potential. The resistivities of the n- and p-type cladding layers are $\rho_n = 1 \times 10^{-2} \Omega \cdot \text{cm}$ and $\rho_p = 14 \Omega \cdot \text{cm}$, respectively; and the other resistivities for the metallic electrode are $\rho_{\text{Ag}} = 1.59 \times 10^{-6} \Omega \cdot \text{cm}$, $\rho_{\text{Ni}} = 6.9 \times 10^{-6} \Omega \cdot \text{cm}$, $\rho_{\text{Au}} = 2 \times 10^{-6} \Omega \cdot \text{cm}$, and $\rho_{\text{Ti}} = 4.2 \times 10^{-5} \Omega \cdot \text{cm}$. The specific p-contact resistance and the specific n-contact resistance are set to be $2.8 \times 10^{-3} \Omega \cdot \text{cm}^2$ and $3.6 \times 10^{-4} \Omega \cdot \text{cm}^2$, respectively, [8]. Following upon our previous work [22], the current through the active layer is assumed to move in the direction perpendicular to the layer. The equation for calculating the electrical potential in the LED is solved using the finite-element method (FEM). The equivalent conductivity for each element in the active layer is calculated by

$$\sigma = \frac{l_e}{V_j} \cdot J_e, \quad (2)$$

where l_e is the elemental thickness of the mesh; V_j is the voltage drop between the active layer; and J_e is the elemental

FIGURE 1: A cross-sectional schematic representation of a Thin-GaN LED chip in the lateral direction, where L represents the size of the n-electrode.

current density [23]. The current behavior through the active layer of the LED chip is dominated by the following Shockley equation:

$$J_e = J_0 \left(\exp^{eV_j/nkT} - 1 \right), \quad (3)$$

where J_0 is the saturation current density; e is the elementary charge (1.6×10^{-19} coul); n is the ideality factor; k is the Boltzmann constant (1.38×10^{-23} J/K); and T is the absolute temperature [23]. It is well known that J_0 and n are dependent on the material quality and/or device structure. The parameters used for the geometric dimensions and for the Shockley equation are the same as those used in previous studies [8]: that is, the saturation current and n are set to be 4.72×10^{-22} A and 2.5, respectively. The p-pad is set to have a uniform input current and the n-pad is set as the ground. With the exception of the electrodes, the rest of the boundaries in the LED chip are all assumed to be insulated. The relationship between J_0 and T developed by Millman and Grabel [24] is also adopted in the present study:

$$J_0(T) = J_0|_{300K} \times 2^{(T-300)/10}. \quad (4)$$

The equation for conduction heat transfer with the heat source for the steady-state is

$$-k_c \nabla \cdot (\nabla T) = \dot{q}, \quad (5)$$

where k_c is the thermal conductivity [23]. Based on the law of energy conservation, the input electrical power can be divided into two major parts; one is the light output power and the other is heat generation. Given the same assumptions for the active layer as in (2), we propose the following heat generation term $\dot{q}$ in the active layer [22]:

$$\dot{q} = J_e \times \frac{[V_j - (\hbar\omega/e) \times \eta_{\text{int}} \times \eta_{\text{ext}} \times \exp(-(T-300)/1600)]}{l_e}, \quad (6)$$

where $\hbar$ is the reduced Planck constant; ω is the angular frequency; η_{int} is the internal quantum efficiency at room

FIGURE 2: Triangular prism elements of each layer in the LED chip.

TABLE 1: Thermal conductivities used in the simulation [22, 23].

Material	Ni	Ag	Au	Ti	GaN
k_c (W/m · K)	55.2	374	290	17.1	130

temperature; and η_{ext} is the light extraction efficiency at room temperature. The heat generated by light absorption inside the LED chip is assumed to be included in this $\dot{q}$ term. In the present study, the value of the external quantum efficiency ($\eta_{\text{int}} \times \eta_{\text{ext}}$) is 25%, as obtained in the literature [22]. The heat generation term per unit volume $\dot{q}$ due to Joule heating [23] in the other layers of the LED chip is

$$\dot{q} = J_e \cdot \nabla V. \quad (7)$$

The thermal conductivities of the materials are summarized in Table 1 [22, 23]. The thermal boundary conditions of the top, lateral, and bottom surfaces of the LED chip are shown by

$$\hat{n} \cdot (k_c \nabla T) = h_e (T_{\text{inf}} - T), \quad (8)$$

where $\hat{n}$ is the unit normal vector of the interface; T_{inf} is the air temperature; and h_e is the equivalent heat transfer coefficient [23]. A copper slug with a board is usually used to dissipate the heat generated from the LED chip. The size is set to be about 7.2 cm^2 in the present study. Natural convection conditions affect the surfaces with $h_e = 5 \text{ W/m}^2 \cdot \text{K}$ and T_{inf} is 300 K. The convection from the bottom surface of the slug is replaced by the convection condition from the chip with the equivalent heat transfer coefficient h_e . In this case, h_e is about $40000 \text{ W/m}^2 \cdot \text{K}$.

A self-developed correlation coupling of the thermal and electrical equations is added to the FEM software (COMSOL Multiphysics licensed version 3.4) to obtain the temperature, the electrical potential, and the current density in the LED chip. In the present study, the simulation is performed in a three-dimensional, steady-state condition and the mesh for each layer is made up of triangular prism elements. The mesh numbers for n-electrodes with holes are much higher than for those without holes due to the structure of the holes. After

FIGURE 3: Current densities in the active layer with an input current of 100 mA for the case of $L = 200 \mu\text{m}$.

convergence testing, the mesh numbers are found to be 2656, 10681, and 18406 for the cases without holes, with $5 \mu\text{m}$ holes and with $10 \mu\text{m}$ holes, respectively, as shown in Figure 2. A circular area $100 \mu\text{m}$ in diameter is reserved in the central region of the n-electrode for wire bonding. Utilizing a similar testing procedure, the relative tolerance is selected to be 1×10^{-3} for the variables of temperature and voltage.

3. Results and Discussion

Figure 3 displays the current densities in the active layer for an input current of 100 mA for the cases where $L = 200 \mu\text{m}$, without holes, with $5 \mu\text{m}$ holes, and with $10 \mu\text{m}$ holes. The simulated current density distributions show almost the same results. In every case, the current crowding beneath the n-electrode is more serious.

Figure 4 shows the temperature distribution in the active layer for the cases of $L = 200 \mu\text{m}$, without holes, with $5 \mu\text{m}$ holes, and with $10 \mu\text{m}$ holes, under the same operating conditions. There is little difference (about 0.1 K) in the maximum temperature in the active layer between the three cases. The temperature distribution results are also the same. Therefore, the structure of the holes on the n-electrode may not cause the change in thermal behavior in the active layer of the LED. The electrical characteristics of the LEDs will not be affected by this slight temperature difference. According to the analyses of the current distribution and temperature distribution, the influences of the n-electrode for cases with and without holes seem very tiny.

FIGURE 4: Temperature distributions in the active layer for the cases with $L = 200 \mu\text{m}$.

FIGURE 5: Current density distributions in the active layer including the shadow of the n-electrode.

In order to improve the shadowing effect of the n-electrode, the current density distributions in the active layer, including the shadow of the n-electrode are shown in Figure 5 for different cases. For the case with $L = 200 \mu\text{m}$, the area beneath the n-electrode is only 1/9 of the total area in the active layer, but the average current density beneath the n-electrode is 3.78 times that of the rest of the area (see Figure 3). The percentages of the light output power from those holes can be integrated in the present numerical simulation. A comparison between the two cases for n-electrodes with holes of different n-electrode size is shown in Figure 6. The results indicate that the n-electrode with 10 μm holes offers increased light output power, about 2.45 times more than n-electrodes without holes.

The wall-plug efficiency of the LED chip is defined as the output light power divided by the total input electrical power. Here, the output light power is selected as the electrical power generated by the residual region of the active layer not covered by the n-electrode subtracted from the total heat generated in the same region. The WPEs for different sizes of n-electrodes with 5 μm and 10 μm holes are also discussed, and the results are compared with the cases of n-electrodes

without holes, as shown in Figure 7. The welding region occupies most of the area of n-electrodes with 5 μm and 10 μm holes in cases where $L = 100 \mu\text{m}$. The n-electrode thus obstructs most light emission for all the cases with and without holes. The WPE for the case without holes is very close to that of the cases with holes. The WPE then decreases as the size of the n-electrode is increased for the cases without holes since the major part of the light emitting area in the active layer is covered by the n-electrode. However, in the cases with holes, the WPE increases when $L = 200 \mu\text{m}$ and then decreases as the size of the n-electrode increases. The light output from these holes plus that from the residual region of the active layer not covered by the n-electrode equals the total light output. Due to a higher current density under the n-electrode, the WPE for $L = 200 \mu\text{m}$ reaches a maximum value. Otherwise, the size of the hole will also influence the light output. A larger size will emit more light output. Therefore, a better size for the n-electrode would be $L = 200 \mu\text{m}$, in the case with 10 μm holes. The WPE can be increased from 2.33% to 5.72% by the design of n-electrode with holes. Based on the study of nanowire array LEDs [14], these LEDs give an external quantum efficiency of 2.5%. The results of the present

FIGURE 6: Percentage of light output with different sizes of n-electrode for the cases with two different hole sizes.

FIGURE 7: Calculated WPE for different sizes of n-electrode for the cases with and without holes.

study are found to agree with the experimental result obtained in the study of Xu et al. [14].

4. Conclusions

In the present study, a design is proposed for n-electrode with holes for application in Thin-GaN LEDs. A new numerical model is used to investigate the effect of the n-electrode with holes design on the thermal and electrical characteristics of a Thin-GaN LED chip. The variation in current density and temperature distributions in the active layer is very tiny for n-electrodes with and without holes. The percentage of light output power from these holes ranges from 3.5% to 37.5% and from 3.1% to 49% for the cases with 5 μm and 10 μm holes

in n-electrodes with different side lengths (L). Therefore, the light output power can be increased 2.45 times by using the n-electrode with holes design. When $L = 100 \mu\text{m}$, the wall-plug efficiency for the case without holes is very close to that of the cases with holes. For the cases with holes, the wall-plug efficiency increases when $L = 200 \mu\text{m}$ and then decreases as the size of the n-electrode is increased. The devices with larger hole size will emit more light output. Thus, the wall-plug efficiency is also improved from 2.3% to 5.7% for the case of $L = 200 \mu\text{m}$ n-electrodes with $10 \mu\text{m}$ holes. WPE analysis is used to determine better n-electrode and hole sizes.

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