Research Article

Novel BCD Process Platform with Integrated Self-Extracted JTE Trench Technology for EL Drivers ICs

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A low cost silicon BCD technology in place of high cost SOI BCD technology for monolithic integrated EL driver ICs application is put forward. Several key technologies are presented. An advanced SEJTET termination technology was designed instead of the conventional PIOS isolation to obtain smaller chip area and protect HVICs from the occurrence of di/dt effect under PWM operation. Novel VDMOS/Resurf LDPMOS devices were developed compatibly to obtain the lowest $R_{on,sp}$, improve silicon utilization, and simplify key process steps.

1. Introduction

In recent years, many portable consumer electronic products have been sold on the market, such as 3G~4G iPhone mobile. Electroluminescent lamps (EL) technology is widely used as the display application of liquid crystal and backlighting because of the physical thinness and light uniformity, generating low power consumption for illumination lamp load with capacitance structure, especially lower cost than that of LED products recently [1, 2].

The EL load is essentially a capacitor structure with phosphor sandwiched between the electrodes. Recently EL driver integrated with full-bridge stage has been mostly developed on thin HV-BCD SOI material because it can play an important role in withstanding high breakdown voltage and protect the cross-talk effect from the noise through the current path of silicon substrate, employing buried oxide with relative dielectric constant ($\epsilon_{ox} \sim 3.9$) and shallow isolation from HV block and LV block. In general, high breakdown devices based on thin SOI are almost LDMOS with RESURF principle, rather than VDMOS [3]. However, the specific on resistance ($R_{on,sp}$) of the former is larger than that of the later due to large curvature radius of potential distribution. On the other hand, with rich color for humanity display, the large number EL capacitance loads need to be driven, which

requires that device size and the cost increase proportionally once HV-BCD SOI technology is still preferable. Therefore, it is paramount to find out a standard technology for EL driver to reduce the whole cost. Silicon epitaxial BCD technology is a popular technology applied in Plasma Display Panel (PDP) display products [4, 5], but several aspects of isolation and HV block integration are not effectively solved. For conventional p-isolation, not only there exists self-doping effect to degrade seriously the performance of the device and circuit, but also p-isolation structure with large area brings about a lot of defects to reduce the yield of HVICs products during long-time thermal cycle [6]. In addition, the process steps for VDNMOS and LDPMOS are complicated is revised as and isn't easily compatible between two devices. Deep trench structure without cylindrical and spherical junctions is one of the candidates for edge termination design of future high voltage power devices to reduce the chip area and improve the block voltage [7–10], but sacrificial oxidation is always employed to remove the damage induced by dry etch so that widening the trench not only brings about the difficulty for refilling trench but also reduces seriously the integration level of HVICs. In this paper, an advanced wet-etch solution to remove the damage of developed SEJTET is firstly put forward. An 8-channel EL driver with the SEJTET in place of conventional p-isolation, a novel VDNMOS shared with the

FIGURE 1: Cross-section view of HV-BCD process platform.

key process of RESURF LDPMOS, also has been developed on low cost bulk silicon to further save energy with higher efficiency and improve the integration level.

2. HV-BCD Process and Device Development

Figure 1 shows the cross-section view of advanced BCD process platform originated from the 0.35 μm standard CMOS-process technologies. The whole processes were 21 steps and the p-drift step was shared by VDNMOS and LDPMOS for RESURF principle. The process platform provides the following devices isolated by SEJTET, including LVN/PMOS (V_{DD} : 3.3 V) for digital analogical application, MVN/PMOS (V_{DD} : 5 V) as buffer stages to drive the gate of HV device, and VDNMOS/LDPMOS (V_{DD} : 150 V).

The deep trench with the space and depth of 2 μm and 16 μm is firstly etched by different RF power parameters of inductively coupled plasma (ICP) to obtain the vertical sidewall and rounded corners of trench and to avoid the convergence of the electric field, especially at the bottom. The wet-etch process is employed in place of conventional scarified oxidation to remove easily the silicon damage caused by high-energy-ion bombardment while maintaining the original space of trench during the trench-etch step. It is controlled about 15 seconds to uniformly remove the damages without spreading toward bulk silicon by the mixture of $\text{HF}:\text{HNO}_3:\text{H}_2\text{O}$ solution, the ultrasonicator under the frequency of 40 kHz and room temperature. Boron is implanted at large tilt angle of 30° around the trench at doses about $6 \times 10^{13} \text{ cm}^{-2}$ and energies of 35~40 keV to form vertical junction termination extension. A 0.35 μm thermal oxide liner is grown as the dielectric layer of trench and the process also plays an role in driving the implanted boron atoms. Finally, following refilling polysilicon and planarization processes for better shape and coverage, the trench is completed and connected with p-type substrate without long-time thermal cycle of PISO process.

Figure 2 shows SEM micrograph of SEJTET, PISO, and NSINKER. The sidewalls of SEJTET are smooth and slightly tapered, with an angle of $\sim 87^\circ$. On the other hand, the 2 μm space of SEJTET is much narrower than that of PISO with 20 μm to block the same reverse voltage. So the HVICs die can be integrated with high-density level.

FIGURE 2: SEM micrograph of SEJTET, PISO, and NSINKER testing structure.

FIGURE 3: Breakdown voltage characteristics of PISO and SEJTET structure.

3. Results and Discussion

It is shown in Figure 3 that the BV characteristics of SEJTET have lower leakage current and almost 20 V higher than that of PISO. Figure 4 makes a comparison between the distribution of electrical field of SEJTET and that of trench by

FIGURE 4: The distribution of electrical field of (a) SEJTET and (b) the trench with oxide refiller.

FIGURE 5: I_d - V_d characteristics of the VDNMOS (120 μm) with different V_{gs} voltage (start/stop/step: 0 V/5 V/1 V).

oxide refiller, employed by ISE-TCAD simulator. The former in Figure 4(a) is completely around the whole trench due to the polysilicon refiller layer into trench as floating electrode and the breakdown voltage is sustained by the implanted junction termination and grown oxide layer together. However, the distribution of electrical field in Figure 4(b) is two-dimensional and finally converges near the outer wall of the trench. So it is demonstrated that the electrical field of SEJTET appears uniformly and the breakdown voltage is higher.

Figure 5 shows the electrical characteristics of VDNMOS device. The threshold voltage (V_{th}) and the forward current of the device are 1.35 V and 26 mA, respectively. The specific on-resistance of the device, $3 \text{ m}\Omega \cdot \text{cm}^2$, is the lowest by comparison with those other studies reported [4–6]. To obtain

the perfect figure of merit ($\text{FOM} = R_{on,sp} \times Q_g$), the merged poly-Si gate was designed and composed of the enhancement channel with the thin gate oxide and the depletion channel with the field oxide to reduce the gate charge Q_g , especially Q_{gd} induced by the miller capacitances C_{gd} . In addition, the optimized high-energy phosphor implantation through the field oxide of depletion channel is employed to reduce on-resistance near JFET region. Finally, the VDNMOS device is double RESURF structure coshared with PDRIFT process parameter of RESURF LDP MOS to achieve low cost.

For RESURF LDP MOS device, the threshold voltage (V_{th}) and the forward current of the device are -20 V and 3.5 mA , respectively. The gate oxide of the LDP MOS is grown together with the field oxide as the high side driver at full-bridge stage of HVICs.

Figure 6 shows the schematic circuit block of EL driver IC with 8 channels. The EL driver IC is in fact a full-bridge circuit. The high voltage level block can play a role in transforming high voltage power supply into the control signal to drive the full-bridge buffer. To improve the driving capacity, the VDNMOS with the width of $240 \mu\text{m}$ is employed. The SEJTET structure is applied as parasitic NPN with shorted BC junction to sustain di/dt effect.

The switch signal with pulse width modulation (PWM), rather than the sine wave, is employed to improve the efficiency. Figure 7 shows the switching waveforms of 100 V rating EL driver ICs during the operation of 400 Hz frequency. Two signals of the opposite phase are biased at two nodes of EL0 (V_A , V_B) to lighten the load. The rise and fall edge of switching waveforms is about 145 ns and 25 ns and it indicates that the switching power loss is small. On the

FIGURE 6: Schematic circuit block of EL driver IC.

FIGURE 7: The switching waveforms of 100 V rating EL driver ICs.

other hand, the node, V_A or V_B connected with the drain of VDNMOS, is biased at high voltage. However, if V_A is dropped from 100 V to zero at high frequency, V_B will be about -0.7 V at freewheel time, which can be measured by voltmeter. So the parasitic PN junction of N-Epi/P-substrate turns on and a large number of minority-carrier injection charges are stored near the junction. When V_A and V_B are into normal operation, the reverse recovery current, I_{recovery} , which is the same order of VDNMOS' forward current, is extracted at short time under the bias of V_{dd} voltage and the VDNMOS is destroyed due to the effect of di/dt . SEJTET is in fact short BC junction of parasitic BJT transistor to extract the stored minority injection near the junction of N-Epi/P-substrate. The measurement of Emission Microscopes (EMMI) further demonstrated that there are no emission spots at full-bridge stage of HVICs [11].

4. Conclusion

In summary, a 150 V rating EL driver IC is fabricated based on the standard 0.35 μm CMOS technology. The proposed EL

driver ICs integrate SEJTET, the novel VDNMOS, RESURF LDMOS, and full-bridge stages. The experimental results show that the performances of the HV devices and the EL driver IC are good, and the cost makes the consumer satisfied due to cheaper bulk silicon technology than SOI technology.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this article.

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