Research Article

Temperature Effects on a-IGZO Thin Film Transistors Using HfO_2 Gate Dielectric Material

Yu-Hsien Lin and Jay-Chi Chou

Department of Electronic Engineering, National United University, Miaoli 36003, Taiwan

Correspondence should be addressed to Yu-Hsien Lin; yhlin@nuu.edu.tw

Received 18 January 2014; Revised 16 June 2014; Accepted 20 June 2014; Published 6 July 2014

Academic Editor: Kaushal Kumar

Copyright © 2014 Y.-H. Lin and J.-C. Chou. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

This study investigated the temperature effect on amorphous indium gallium zinc oxide (a-IGZO) thin film transistors (TFTs) using hafnium oxide (HfO_2) gate dielectric material. HfO_2 is an attractive candidate as a high- κ dielectric material for gate oxide because it has great potential to exhibit superior electrical properties with a high drive current. In the process of integrating the gate dielectric and IGZO thin film, postannealing treatment is an essential process for completing the chemical reaction of the IGZO thin film and enhancing the gate oxide quality to adjust the electrical characteristics of the TFTs. However, the hafnium atom diffused the IGZO thin film, causing interface roughness because of the stability of the HfO_2 dielectric thin film during high-temperature annealing. In this study, the annealing temperature was optimized at 200°C for a HfO_2 gate dielectric TFT exhibiting high mobility, a high $I_{\text{ON}}/I_{\text{OFF}}$ ratio, low I_{OFF} current, and excellent subthreshold swing (SS).

1. Introduction

In recent years, transparent oxide thin film transistors (TFTs) have attracted substantial attention because of their potential application in the display industry as next-generation thin film transistors. In addition, amorphous indium gallium zinc oxide (a-IGZO) provides numerous advantages compared with polysilicon, including a high carrier mobility rate, a high switching current ratio, a low-temperature process, excellent uniformity, excellent transparency to visible light, and large-area processes, facilitating its integration in high-resolution displays [1–5]. Compared with amorphous silicon TFTs, a-IGZO TFTs exhibit higher mobility (3–30 $\text{cm}^2/\text{V}\cdot\text{s}$) even in the amorphous phase [2, 6–8]. In general, a-Si:H and polysilicon, which are commonly used as channel layers for transistors, have several limitations, including high temperatures, photosensitivity, and high cost when used in conventional complementary metal-oxide-semiconductor processes. IGZO thin film can be deposited at room temperature by using the cosputtering process or sol-gel methods, which involve low thermal budgets and are compatible with glass substrates and flexible plastic substrates [9].

High- κ gate dielectric materials have been widely used to reduce electron tunneling and maintain a large capacitance at a high drive current [10–12]. Hafnium oxide (HfO_2) is an attractive candidate for use as a high- κ dielectric material because it exhibits thermodynamic stability, a high dielectric constant, proper conduction and valence-band offset with Si, low lattice mismatch with Si, and excellent electrical properties at high drive currents. Therefore, by incorporating HfO_2 for the gate dielectric, the operation voltage can be reduced and device scaling can be facilitated. In addition, considering the integration of the TFTs process, the thermal budget is crucial in high-speed and high-resolution display applications. Regarding the high- κ dielectric thin film/IGZO interface, maintaining a high subthreshold swing (SS) and low carrier mobility is the critical concern when a high thermal budget is involved.

To investigate these concerns, the effect of temperature on a-IGZO TFTs with HfO_2 gate dielectric was studied by analyzing electrical characteristics and conducting material analysis. In addition, the optimal electrical characteristics of a-IGZO TFTs were determined.

FIGURE 1: (a) Schematic cross-section of the fabricated bottom-gate a-IGZO TFTs with HfO₂ gate dielectric. (b) Top view of the a-IGZO TFTs with HfO₂ gate dielectric. The device had dimensions of $L/W = 200/1000 \mu\text{m}$.

2. Experiment

The process of fabricating the a-IGZO TFTs with HfO₂ gate dielectric involved using N⁺-type wafers and a bottom-gate structure, as shown in Figure 1(a). First, 100 nm HfO₂ thin film was deposited using the E-gun method with HfO₂ targets. Second, a 30 nm a-IGZO layer was deposited using cosputtering with IGZO₄ targets (In, Ga, Zn, O ratio: 1:1:1:4) in ambient oxygen gas (O₂). The cosputtering process was performed at 4×10^{-3} Torr in room temperature with precursors of O₂ (6 sccm) and Ar (24 sccm), and the DC sputter power was set at 150 W. After active region patterning was performed, 30 nm titanium (Ti) thin film was deposited and used for source and drain electrodes, using the E-gun method at room temperature. After source/drain patterning was conducted, postannealing treatment was performed for 30 minutes at temperatures ranging from 150°C to 450°C at increments of 50°C to fabricate the HfO₂ gate dielectric a-IGZO TFTs. The top-view layout of the a-IGZO TFT is shown in Figure 1(b). All devices used in this study exhibited length/width dimensions of 200/1000 μm .

3. Results and Discussion

Figure 2 shows the basic I_D - V_G electrical characteristics of the a-IGZO TFTs with HfO₂ gate dielectric at a temperature of 200°C during postannealing; the gate voltage varied from -2 to 5 V and the drain voltage was 1 V. The inset of Figure 2 shows the I_D - V_{DS} output characteristics of the a-IGZO TFTs with HfO₂ gate dielectric, in which the drain voltage varied from 0 to 10 V and the gate voltages were 0, 2.5, and 5 V. Based on the transfer and output characteristics, the device operated in enhancement mode and exhibited a large on-to-off current ratio (I_{ON}/I_{OFF}) greater than 10^7 . The apparent field-effect mobility induced by transconductance at a low drain voltage $V_{DS} = 1$ V was determined as follows:

$$\mu_{FE} = \frac{Lg_m}{WC_iV_{DS}}, \quad (1)$$

where C_i and g_m were the gate capacitance per unit area and transconductance, respectively [13]. For our device, the C_i is

FIGURE 2: I_D - V_{GS} transfer characteristics of the a-IGZO TFTs with HfO₂ gate dielectric. The insert figure shows the I_D - V_{DS} characteristics of a-IGZO TFTs with HfO₂ gate dielectric.

$8.63 \times 10^{-9} \text{ F/cm}^2$ measured by test pattern. The maximum g_m is $1.98 \times 10^{-3} \text{ mA/V}$ calculated on the I_D - V_G curve. A high field-effect mobility of $38.29 \text{ cm}^2/\text{V-s}$ was obtained. The threshold voltage (V_{th}) and SS were 1.15 V and 0.137 V/dec, respectively, and were extracted from the linear portion of the $\log(I_D^{1/2})$ versus V_G plot. The a-IGZO TFTs with HfO₂ gate dielectric exhibited superior field-effect mobility compared with that of a-IGZO [14–16]. Table 1 lists a summary of our TFTs. Figure 3 shows the transfer characteristics of the a-IGZO TFTs with HfO₂ gate dielectric at various oxygen gas flow rates of the precursors: 6, 25, and 50 sccm. According to previous studies, the electrical characteristics of a-IGZO film can be controlled using a combination of O₂ and O vacancies [17, 18]. The oxygen vacancies are compensated by O₂ and the conductivity of the IGZO channel is reduced for supplying free electron carriers. According to the results shown in Figure 3, when the oxygen gas flow rate was increased, the V_{th} increased because of less oxygen vacancies; so the resistance of the IGZO channel was enhanced, and a high V_t was required for activating the device. A high conductive channel that exhibited a small SS was also achieved with a low oxygen

FIGURE 3: I_D - V_{GS} transfer characteristics of the a-IGZO TFTs with HfO_2 gate dielectric with precursors of O_2 (6, 25, and 50 sccm) through RTA treatment at room temperature.

TABLE 1: A summary table (I_{ON}/I_{OFF} ratio, V_t , I_{OFF} , and SS) of the a-IGZO TFTs with HfO_2 gate dielectric.

W/L (μm)	V_{th} (volts)	SS (V/dec.)	μ ($\text{cm}^2/\text{V}\cdot\text{s}$)	I_{ON}/I_{OFF}
1000/200	1.15	0.137	38.29	2.9×10^6

TABLE 2: The standard enthalpy of formation for HfO_2 , In_2O_3 , Ga_2O_3 , and ZnO .

Standard enthalpy of formation	HfO_2	In_2O_3	Ga_2O_3	ZnO
ΔH_f° (kJ/mol)	-1144.7	-925	-1089.1	-350.5

gas flow rate. To optimize the conditions of the IGZO thin film, a 6 sccm oxygen gas flow rate was used in subsequent experiments.

Figure 4(a) shows the transfer characteristics of the a-IGZO TFTs with HfO_2 gate dielectric that depended on the annealing temperature when the gate voltage varied from -2 to 5 V. The postannealing temperature ranged from 150°C to 450°C at increments of 50°C and was applied for 30 minutes. The on-to-off current ratio (I_{ON}/I_{OFF}), I_{OFF} , V_t , and SS values are shown in Figure 4(b). Based on the values listed in Figure 4(b), applying a temperature of 200°C enabled the device to demonstrate excellent performance compared with the results of applying other temperatures. The a-IGZO TFTs with HfO_2 gate dielectric exhibited unfavorable electrical characteristics if the postannealing temperature exceeded 300°C. The least favorable HfO_2 /IGZO interface and oxide quality observed during annealing was speculated to be the result of I_{OFF} and SS increasing. Figure 5 shows an atomic force microscope (AFM) image of the HfO_2 /IGZO testing sample annealed at temperatures of 200°C–400°C

FIGURE 4: (a) I_D - V_{GS} transfer characteristics of the a-IGZO TFTs with HfO_2 gate dielectric with different annealing temperature. (b) A comparison of various parameters includes I_{ON}/I_{OFF} ratio, V_t , I_{OFF} , and SS for a-IGZO TFTs with HfO_2 gate dielectric.

at increments of 100°C. The testing sample HfO_2 /IGZO structure was IGZO-film deposited onto the HfO_2 thin film. Based on the AFM results, the root mean square (RMS) of the IGZO film was compatible with the splits when the annealing temperature was below 300°C. When the annealing temperature was increased to 400°C, the RMS of the IGZO film increased from 0.510 to 1.179 nm. The smooth IGZO surface played a critical role in the high-performance device developed in this study. Figure 6 shows the secondary ion mass spectrometry (SIMS) data for the HfO_2 /IGZO testing sample when it was annealed at various temperatures ranging from 200°C to 400°C at increments of 100°C. According to the SIMS results, the hafnium (Hf) intensity in the IGZO film was compatible with the splits when the annealing temperature was below 300°C. The Hf atoms were initially assumed to not diffuse at low temperatures. However, when the annealing temperature was increased to 400°C, the Hf atoms diffused

FIGURE 5: AFM graph for a-IGZO TFTs with HfO₂ gate dielectric with different annealing temperature.

to the IGZO film. Based on the results presented in Figures 5 and 6, surface roughness was expected to develop because of Hf diffusion, maintaining device reliability at high temperatures. Table 2 shows the standard enthalpy of formation of HfO₂, In₂O₃, Ga₂O₃, and ZnO. Based on this information, HfO₂ was determined to have a low standard enthalpy of formation, indicating that HfO₂ is the most stable among the evaluated materials. However, if the HfO₂ dielectric quality was not favorable, such as the poor oxide formation of HfO_x ($x = 1-2$) caused by low-temperature fabrication, the Hf atom and oxygen atom reacted with each other to stabilize because of the low standard enthalpy of formation. Therefore, when high-temperature annealing was performed, the Hf atom readily diffused to the IGZO film. According to Figure 6, when the annealing temperature was 400°C, the Hf atom intensity substantially increased, diffusing into all the IGZO films. This resulted in surface roughness at the

HfO₂/IGZO interface and caused severe device reliability problems. Therefore, the optimal annealing temperature is 200°C for fabricating a-IGZO TFTs with HfO₂ gate dielectric.

4. Conclusion

This study explored the temperature effect of the a-IGZO TFTs with HfO₂ gate dielectric. During high-temperature annealing, the hafnium atom diffused the IGZO thin film easily, and caused interface roughness because of the stability between the HfO₂ dielectric thin film and IGZO thin film. For optimizing the conditions of combining HfO₂ gate dielectrics with a-IGZO thin films, the postannealing at 200°C could yield high mobility, a high I_{ON}/I_{OFF} ratio, low I_{OFF} , and excellent SS. a-IGZO TFTs with HfO₂ gate dielectric that exhibit excellent characteristics were successfully demonstrated through sufficiently low thermal-budget processing.

FIGURE 6: SIMS profiles for a-IGZO TFTs with HfO_2 gate dielectric with different annealing temperature.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgment

This project was sponsored by the National Science Council of Taiwan (no. NSC 102-2221-E-239-034).

References

- [1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 7016, pp. 488–492, 2004.
- [2] H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "Amorphous oxide channel TFTs," *Thin Solid Films*, vol. 516, no. 7, pp. 1516–1522, 2008.
- [3] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: electronic structure, electron transport, defects and doping," *Journal of Display Technology*, vol. 5, no. 7, pp. 273–288, 2009.
- [4] A. Takagi, K. Nomura, H. Ohta et al., "Carrier transport and electronic structure in amorphous oxide semiconductor, a- InGaZnO_4 ," *Thin Solid Films*, vol. 486, no. 1-2, pp. 38–41, 2005.
- [5] C. J. Chiu, Z. W. Pei, S. P. Chang, and S. J. Chang, "Influence of weight ratio of poly(4-vinylphenol) insulator on electronic properties of InGaZnO thin-film transistor," *Journal of Nanomaterials*, vol. 2012, Article ID 698123, 7 pages, 2012.
- [6] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors," *Japanese Journal of Applied Physics*, vol. 45, no. 5, pp. 4303–4308, 2006.
- [7] H. Hosono, "Ionic amorphous oxide semiconductors: material design, carrier transport, and device application," *Journal of Non-Crystalline Solids*, vol. 352, no. 9–20, pp. 851–858, 2006.
- [8] T. Iwasaki, N. Itagaki, T. Den et al., "Combinatorial approach to thin-film transistors using multicomponent semiconductor channels: an application to amorphous oxide semiconductors in In-Ga-Zn-O system," *Applied Physics Letters*, vol. 90, no. 24, Article ID 242114, 2007.
- [9] Y. Wang, S. W. Liu, X. W. Sun et al., "Highly transparent solution processed In-Ga-Zn oxide thin films and thin film transistors," *Journal of Sol-Gel Science and Technology*, vol. 55, no. 3, pp. 322–327, 2010.
- [10] B. H. Lee, L. Kang, R. Nieh, W. Qi, and J. C. Lee, "Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing," *Applied Physics Letters*, vol. 76, no. 14, pp. 1926–1928, 2000.
- [11] L. Kang, B. H. Lee, W.-J. Qi et al., "Electrical characteristics of highly reliable ultrathin hafnium oxide gate dielectric," *IEEE Electron Device Letters*, vol. 21, no. 4, pp. 181–183, 2000.
- [12] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "Hafnium and zirconium silicates for advanced gate dielectrics," *Journal of Applied Physics*, vol. 87, no. 1, pp. 484–492, 2000.
- [13] M. Kim, J. H. Jeong, H. J. Lee et al., "High mobility bottom gate InGaZnO thin film transistors with SiO_x etch stopper," *Applied Physics Letters*, vol. 90, no. 21, Article ID 212114, 2007.
- [14] S. Hwang, J. H. Lee, C. H. Woo, J. Y. Lee, and H. K. Cho, "Effect of annealing temperature on the electrical performances of solution-processed InGaZnO thin film transistors," *Thin Solid Films*, vol. 519, no. 15, pp. 5146–5149, 2011.
- [15] J. Park, J. K. Jeong, H. Chung, Y. Mo, and H. D. Kim, "Electronic transport properties of amorphous indium-gallium-zinc oxide indium-gallium-zinc oxide semiconductor upon exposure to water," *Applied Physics Letters*, vol. 92, no. 7, Article ID 072104, 2008.
- [16] S. Kim, Y. W. Jeon, Y. Kim et al., "Impact of oxygen flow rate on the instability under positive bias stresses in DC-sputtered amorphous InGaZnO thin-film transistors," *IEEE Electron Device Letters*, vol. 33, no. 1, pp. 62–64, 2012.
- [17] E. Chong, Y. S. Chun, S. H. Kim, and S. Y. Lee, "Effect of oxygen on the threshold voltage of a-IGZO TFT," *Journal of Electrical Engineering and Technology*, vol. 6, no. 4, pp. 539–542, 2011.
- [18] C. G. Van de Walle, "Hydrogen as a cause of doping in zinc oxide," *Physical Review Letters*, vol. 85, no. 5, pp. 1012–1015, 2000.