Research Article

AlGa_N/Ga_N High Electron Mobility Transistors with Multi-Mg_xN_y/Ga_N Buffer

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We report the fabrication of AlGa_N/Ga_N high electron mobility transistors with multi-Mg_xN_y/Ga_N buffer. Compared with conventional HEMT devices with a low-temperature Ga_N buffer, smaller gate and source-drain leakage current could be achieved with this new buffer design. Consequently, the electron mobility was larger for the proposed device due to the reduction of defect density and the corresponding improvement of crystalline quality as result of using the multi-Mg_xN_y/Ga_N buffer.

1. Introduction

GaN-based materials demonstrate an outstanding potential for significantly advancing the solid-state electronic and optoelectronic technologies. However, there are still no suitable substrates that are commercially available for homoepitaxial growth of Ga_N thin films. Instead, devices must be grown heteroepitaxially on sapphire or other substrates with an expense of high lattice mismatch. As of result, extremely high threading dislocation (TD) densities are thus generated. Very recently, it was found that Ga_N epitaxial layer prepared on multi-Mg_xN_y/Ga_N buffer exhibited a reduced TD density and better crystalline quality. In addition, we have also reported high performance Schottky barrier diodes or photodetectors on multi-Mg_xN_y/Ga_N buffer [1]. In this paper, we extend the applicability of this buffer scheme by fabricating AlGa_N/Ga_N high electron mobility transistors (HEMTs) on multi-Mg_xN_y/Ga_N buffer. Physical and electrical properties of the fabricated HEMTs will also be discussed afterward.

2. Materials and Methods

All of the samples used in this study were grown on c-face (0001) sapphire substrates by metalorganic vapor phase epitaxy (MOVPE) system. Al_{0.22}Ga_{0.78}N/Ga_N HEMTs structure

with a conventional low temperature Ga_N buffer layer (i.e., sample A) and a multi-Mg_xN_y/Ga_N buffer (i.e., sample B) were both prepared. Detailed growth procedures of these HEMT structures can be found elsewhere [2]. Device fabrication started with mesa isolation using BCl₃ etchants from the reactive ion etching system. Ohmic contacts were formed by thermal evaporation of Ti/Al/Ti/Au (13/80/13/60 nm) metals, which were subsequently annealed at 800°C for 8 min in N₂ ambient. Finally, Ni and Au (40/100 nm) were used for gate electrodes with a dimension of 1 × 50 μm². The schematic device structure can be found in Table 1. Device performance was measured at room temperature by using an HP-4155B semiconductor parameter analyzer for DC characteristics, an HP-4284A LCR meter for capacitance-voltage (C-V) measurements.

3. Results and Discussion

Electron mobility (μ) of sample A and sample B was measured at temperatures from 120 K to 500 K using Hall-effect measurement technique with van der Pauw configuration. As shown in Figures 1(a) and 1(b), the theoretical μ is limited by the various scattering mechanisms, such as piezoelectric, acoustic-mode deformation potential, and polar optical

FIGURE 1: Temperature-dependent mobility of (a) sample A and (b) sample B.

TABLE 1: The schematic device structures of samples A and B.

Sample A	Sample B
20 nm $n\text{-Al}_{0.22}\text{Ga}_{0.78}\text{N}$ ($1 \times 10^{17} \text{ cm}^{-3}$)	20 nm $n\text{-Al}_{0.22}\text{Ga}_{0.78}\text{N}$ ($1 \times 10^{17} \text{ cm}^{-3}$)
2.2 μm un-GaN	2.2 μm un-GaN
LT-GaN buffer	multi-Mg _x N _y /GaN buffer
Sapphire	Sapphire

phonon, assuming that Matthiessen's rule [3] is applied. A good fit is obtainable at low temperature, while a large deviation occurs at high temperature. Therefore, besides the aforementioned scattering mechanisms, scattering due to extended crystalline defects such as TDs and planar defects may also be significant and must be taken into account in order to achieve a good fit especially at high temperature. The strain associated with and the charge collected at these defects may introduce a potential that tends to scatter electrons. In our work, the empirical limit of crystal defect function with the form of $C/T^{1.5}$ at high temperature has to be included. It was found that the fitting parameter C is equal to 2.11×10^7 and 3.65×10^7 for samples A and B, respectively. It was also found that μ below the room temperature was higher in sample B compared to that of sample A. The larger magnitudes of C and μ observed from sample B suggest smaller defect density and better crystalline quality. On the other hand, the reason for observing sample A with lower μ at higher temperature remains unclear. One possible cause could be due to the fields being induced by the domain boundaries or a change of strain as a result of incorporating the multi-Mg_xN_y/GaN buffer.

Atomic force microscopy (AFM) was also used to characterize these two samples. Figures 2(a) and 2(b) show AFM images ($5 \times 5 \mu\text{m}^2$) of samples A and B, respectively. As shown in Figure 2(a), dark pits can be clearly observed from sample A. These pits generally originate from the surface

termination of TDs and are thought to be one of the leakage current sources in GaN-based devices [4]. In contrast, a more flat surface with invisible dark pits is observed from sample B. Therefore, one suggests that the multi-Mg_xN_y/GaN buffer could significantly improve the crystalline quality and thereby reduce the TD-related leakage paths. This agrees well with the aforementioned results obtained by Hall-effect measurement.

HEMT was fabricated as follows: mesa etching was performed by a reactive ion etcher for device isolation. Ti/Al/Ti/Au (13 nm/80 nm/13 nm/60 nm) was subsequently deposited on the samples as the source and drain contact electrodes, followed by 800°C furnace annealing in N₂ ambient for 8 min. Finally, $1 \mu\text{m} \times 50 \mu\text{m}$ Ni/Au (40 nm/100 nm) gate metal was deposited on the samples. HEMT device performances were measured using an HP 4155 semiconductor parameter analyzer. Figures 3(a) and 3(b) show the drain-source current (I_{DS}) as a function of the drain-source voltage (V_{DS}) when the gate-source voltage (V_{GS}) was varied from 1 to -5 V with a step of -0.5 V for sample A and sample B, respectively. As shown in Figure 3(b), sample B is completely pinched off at V_{GS} of -1 V. On the other hand, the source-drain (S-D) leakage current of sample A was relatively large. For example, with $V_{\text{DS}} = 10 \text{ V}$ and $V_{\text{GS}} = -5 \text{ V}$ applied, the resultant S-D leakage current was as high as 6.9 mA/mm for sample A, as shown in Figure 3(a). In other words, the transistor corresponding to sample A could not be turned off completely, even with a large negative gate bias applied. It has been reported that nonisolated channel or poor Schottky gate contact could result in a large S-D leakage current in HEMT devices [5]. However, since the same processing condition was implemented on both samples, we believe that the large S-D leakage current was originated instead from the 2.2 μm thick unintentionally doped GaN layer. It was found that GaN epitaxial layer prepared on multi-Mg_xN_y/GaN buffer exhibited higher carrier mobility and lower background concentration, which lead to lower S-D leakage current and better pinch-off characteristic.

FIGURE 2: AFM images of (a) sample A and (b) sample B.

FIGURE 3: Output characteristics of drain-source current (I_{DS}) as a function of drain-source voltage (V_{DS}) of (a) sample A and (b) sample B. Gate-source voltage (V_{GS}) varied from 1 V to -5 V with step of -0.5 V.

FIGURE 4: Drain-source current (I_{DS}) and transconductance (g_m) as a function of gate-source voltage (V_{GS}) of both samples. The inset shows pinch-off characteristics of both samples at $V_{DS} = 10$ V.

The I_{DS} and the transconductance (g_m) as a function of V_{GS} at $V_{DS} = 10$ V are shown in Figure 4. It was found that the maximum extrinsic g_m values were 106 and 116 mS/mm for samples A and B, respectively. The enhancement of g_m could be attributed to the higher carrier mobility and better pinch-off characteristic obtained from sample B with multi- Mg_xN_y /GaN buffer. The inset of Figure 4 shows pinch-off characteristics at $V_{DS} = 10$ V of both samples, including subthreshold I_D - V_{GS} and gate leakage current (I_G)- V_{GS} curves. Sample B demonstrated a larger subthreshold slope compared to that of sample A. Furthermore, sample B also showed larger I_{on}/I_{off} ratio compared to that of sample A. These results were attributed to the lower pinch-off current associated with sample B. In addition, we also found that I_G of sample B was one order of magnitude lower than that of sample A. Lower gate and S-D leakage currents thus obtained both suggest that the pinch-off characteristics of HEMT could be substantially improved through the incorporation of the multi- Mg_xN_y /GaN buffer.

4. Conclusions

In summary, AlGaIn/GaN HEMTs with conventional low temperature GaN buffer and with multi- Mg_xN_y /GaN buffer were both fabricated. It was found that the gate and S-D leakage current of the HEMTs could be substantially reduced by using multi- Mg_xN_y /GaN buffer. The improvements in transfer and pinch-off characteristics of the HEMTs were also realized by the adoption of the multi- Mg_xN_y /GaN buffer scheme.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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