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Research Article

The Si Nanocrystal Trap Center Studied by Deep Level Transient Spectroscopy (DLTS)

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Si nanocrystal (NC) embedded into the SiO_2 matrix was made by SiO/SiO_2 superlattice method. Here we investigate the storage phenomena of MOS structure having Si NC inside the dielectric layer by high frequency *C-V* method and DLTS. DLTS treated the individual Si NC as a single point deep level defect in the oxide and revealed essences of Si NC storage, such as a large capture cross section at about 1–7 $\times 10^{-13}$ cm^2 and potential barrier at about 1.6 eV. These two properties we observed are consistent with Si NC dimensions of 5–7 nm in the planar TEM image, and previous *I-V* characterization in the MOS-like structure. These results are helpful to understand the principle of charge storage of this structure and optimize the performance of real Si NC device. The trapping mechanism in MOS systems containing Si NCs is related to the quantum levels of the Si NC band structure at around 300 K.

1. Introduction

Memory-cell structures employing discrete traps as the charge storage media have received much attention as promising candidates to replace conventional polycrystalline silicon or silicon nitride nonvolatile memories for future high capacity and low power consuming memory devices. NC memory devices employing distributed nanodots as storage elements have shown great potential in device applications [1]. A floating gate composed of individual nanocrystals reduces the problem of charge loss encountered in conventional commercial floating gate, such as short retention, endurance, and SILC (stress induced leakage current), and allows further scaling down of tunnel oxides thereby lowering working bias and faster write/erase speeds.

Meanwhile, the efficient visible luminescence at room temperature from silicon NCs was a focus of interest because it might lead to the development of a Si-based efficient light source. Due to the excellent quantum confinement effect, nanosized Si is also advanced material for various applications, such as solar cell, and photonic applications. Crystalline nano-Si as an absorber based tandem solar cell is promising way to exceed the limit of efficiency of single-junction solar cell, since tandem solar cell could cover most solar spectra, compared to single solar structure [2]. Cheng developed a mutlicolor electroluminescent MOSLED structure based on Si nanodots because its indirect band gap was tuned and radiative emissions were enhanced [3]. Except for the above, other photonic applications, such as waveguide [4] and Raman laser [5], are investigated. Stimulated Raman scattering and lasing have been demonstrated in the nanoscale silicon.

However, the real origin of the trap/detrap phenomena in the silicon nanofloating gates is still under debate, even including the generation of the luminescence of the nanocrystalline silicon. Several models of charge storage were proposed such as three-dimensional quantum confinement effect [6] and interface and defects states [7]. The existence of defects due to lattice damage of ion implantation and hydrogen effects from CVD process [8] in the Si NC based MOS structure might generate parasitic traps and influence the charge performance. Among these methods, considering the good adhesion of SiO with SiO_2 and simplicity of the sources, the SiO/SiO_2 superlattice method shows robust charging capability due to its low interface and defect density.

In contrast to the steady-state high frequency *C-V* methods described so far, transient capacitance spectroscopy gives information by measuring how the nonsteady state high frequency capacitance changes with the time. DLTS invented by Lang [9] is now widely used to detect traps of the so-called "deep levels" in the band gap. Initially, the method utilized measurements of transient capacitance following the pulsed bias in a *p-n* junction or Schottky barrier diode to monitor changes in the charge state of defect centres. Schulz and Johnson [10] extended applying DLTS to study the charge emission from interface states in MOS structures. Therefore, for Si NCs embedded MOS structure, if the charge emission from interface states of Si NC is detectable, it is worthwhile to use DLTS for characterization. The DLTS signal is the difference in capacitances at two different times after a filling pulse. It shows peaks for different trap levels in the sample at the respective temperatures T. If traps are filled by a filling pulse and the reverse bias is switched on again, the sample is in thermal nonequilibrium and relaxes into equilibrium by detrapping the charges back. This relaxation process is related to capacitance transient. Its time constant is governed by the thermal emission rate, $e_{n,p}$, which depends on the trap energy E_t and the temperature T:

$$e_{n,p} = \frac{1}{\tau_e} = \frac{N_{n,p}\sigma_{n,p}\nu_{n,p}}{g} \exp\left(-\frac{E_t}{kT}\right). \quad (1)$$

Here $N_{n,p}$ is the effective density of states in the conduction band or valence band, $\sigma_{n,p}$ is the capture cross section of the trap, $\nu_{n,p}$ is the carrier velocity, g is the degeneracy factor. We can see here that the emission rate is exponential dependent on $1/T$, so the thermal energy (or activation energy E_t) determining its slope and the capture cross section σ determining its intercept are the main features of the curve. Because

$$\text{DLTS} = a\left(C\left(t_2\right) - C\left(t_1\right)\right). \quad (2)$$

The DLTS signal is scaled in units of capacitance (usually pF). In principle, a DLTS measurement starts at a low temperature. The signal is recorded, and temperature is ramped up for measurement. During the raising of T, according to $\exp(-E_t/kT)$ dependence of the thermal emission rate, as long as T is too low for significant thermal emission until t_2, the difference in (2) is zero. If T is so high that the thermal emission is already over at t_1, the difference in (2) is also zero. Only if the emission time constant (or its inverse, the emission rate for convenience) of one level falls into the so-called "rate window" given by the definition of t_1 and t_2, a DLTS peak appears. We obtain the following condition for the DLTS peak to appear:

$$e_{n,p} = \frac{\ln\left(t_2/t_1\right)}{\left(t_2 - t_1\right)}. \quad (3)$$

The "rate window" is the inverse of τ_e, according the formula of the relaxation time constant τ_e, and has the unit of s^{-1}. Because of (1), for each trap, the trap energy and the capture cross section are determined by its slope and intercept, respectively, may be determined from an Arrhenius plot $\ln(e_{n,p}) \sim 1/T$.

Few researchers have used DLTS to observe the Si NCs charging process [11], however. Because of the drawback of their fabrications methods, only limited information about Si nanodots was obtained and was usually hidden by artificial parasitic traps. Here we present our DLTS measurements of Si NCs samples based on the SiO/SiO_2 superlattice. Several results are explained and are consistent with previous reports [12]. These results might help us to understand the trap process of the Si nanofloating gates and optimize the future operation of nonvolatile memory devices based on Si nanocrystals. The charge-pumping method is a kind of nonsteady-state measurement, but it is widely used to evaluate the interface states in MOS transistors which has a more complex 4-terminal structure; we do not concentrate on this method in this paper.

2. Experimental Details

The nonsymmetrical sandwich structure samples were prepared as usually on highly doped *n*-type (100) silicon substrates (0.05–0.1 Ω cm). After RCA cleaning, first, a 4 nm SiO_2 film was deposited as a tunnel oxide, and then a 4 nm layer of SiO was deposited by SiO powder evaporation. On top of this structure, an additional SiO_2 layer was evaporated as the upper control oxide with the layer thickness of 24 nm. In order to form the Si NCs, thermal annealing was performed in a quartz tube furnace under N_2 ambient (1100°C, 0.5 h) for phase separation and crystallization. For comparison, a control sample, that is, a pure SiO_2 film with the same total dioxide thickness as the sample with Si nanocrystals, was prepared on the same type of substrate using the same deposition conditions. Schematic sample structure is show in Figure 1(a).

The electrical measurements were performed at 100 kHz using an HP4194A impedance analyzer at room temperature. For more information about the traps of the samples, DLTS was performed in the 100–310 K temperature range with variable pulse bias and rate windows. The heating rate was 0.4 K/min. The cryostat containing the sample was attached to the capacitance meter with preamplifier, and the amplified transient capacitance was processed by the electronics and a PC. The capacitance of the sample is measured under depletion region conditions. The "rate windows" were chosen as 34.7, 17.3, and 8.7 s^{-1} for the measurements.

3. Results and Discussions

3.1. Structural Characterizations. Atomic-resolution plane-view TEM images were investigated using a JEOL JEM4010 with 400 KV. Because the electron beam is vertically transmitted through the sample, the texture of (111) lattice plane is easier to visualize for diamond cubic crystal of Si. Several Si NCs are marked in Figure 1(b). Zooming into this inplane image, only NCs having the right orientation to the incident electron beam can be seen. We roughly estimate the interplanar spacing (d spacing) to be about 3.14 A, and the size of Si dots is about 5–7 nm. These interplanar spacing values are identical to the bulk values from literature [13]

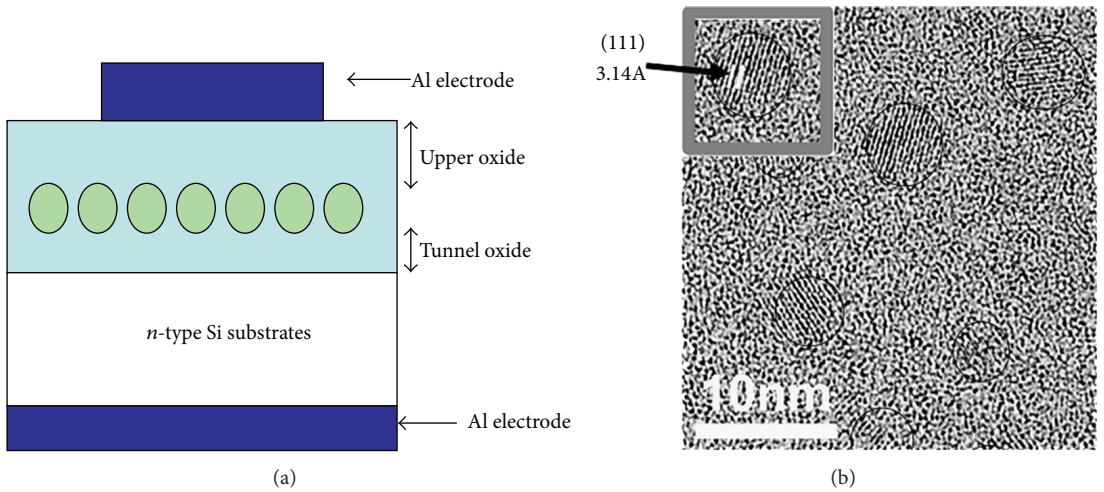

Figure 1: (a) A schematic model of sample structure; (b) plane-view high resolution TEM image of sample. This image was taken by JEOL JEM400. Average size of Si NC is about 5–7 nm.

and demonstrate that dots are unstrained by the surrounding SiO_2. This evidence could help us to understand the mechanic property of the Si dots in the matrix. Strain could influence the carrier mobility; hence, the message that the Si NCs obviously are not under strain is important property.

Here we use SiO/SiO_2 superlattices method to make Si NC inside SiO_2 layer. This method results in ordered arranged silicon NC and independently control of particle sizes as well as of particle density and spatial position by using a constant stoichiometry of the layers. Since SiO/SiO_2 superlattice method uses the controllable SiO layer thickness to control the size of Si nanocrystal when SiO layer takes phase separation to Si and SiO_2 at annealing process, the size distribution of Si from this technology will be narrow. In the following electrical characterizations we will find that the FWHM of DLTS is small.

3.2. Electrical Characterizations. Figure 2 presents typical *C-V* curves of the sample. The voltage sweep range is from −3 V to 6 V. The loop of the forward and reverse sweep *C-V* characteristics indicates the electron charging and discharging process of Si NCs embedded in SiO_2. The details of charging behavior of Si NC were discussed previously [14]. The width of flat-band shift from high frequency *C-V* measurement is related to charge density. The DLTS study gives more detailed information, in addition to *C-V* characterization in Figure 2. The process of measurement is the following.

Electron injections to dots appear by positive reverse bias on the gate, whereby, near the interface of Si–SiO_2, the potential slope is so steep that electrons are populated and confined by oxide and the steep potential. The electron energy perpendicular to the interface is now quantized into discrete states; this phenomenon is called surface quantization and it helps the electron injection [15]. Electron escape emission is from the interface or quantum levels of the dots by repeating bias filling pulses. The emission of electrons is recorded by measuring the capacitance transient. Figure 3 shows the

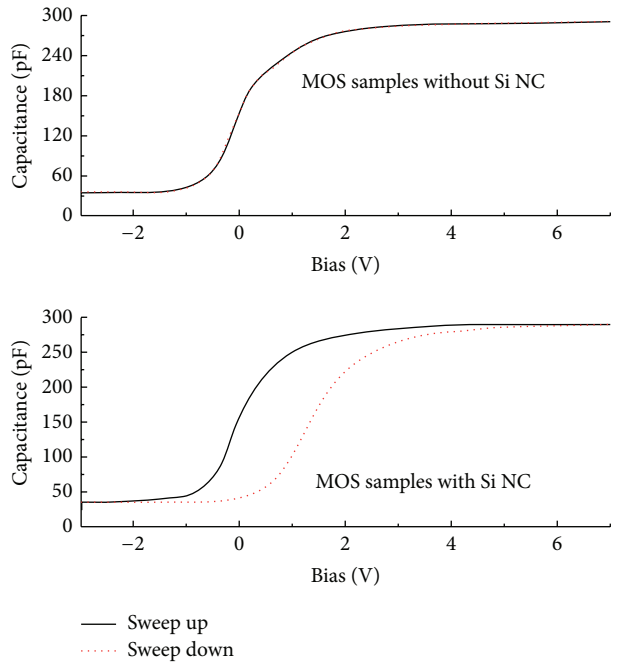

Figure 2: High frequency *C-V* curves of the control sample and sample with Si NC.

DLTS signal of the control SiO_2 sample in Figure 3(a) and a sample with Si NC in Figure 3(b).

Negative peaks mean that the electrons (majority carriers) are in the space charge region. In Figure 3(a), only one peak around 190 K is obtained in the spectra, but the spectra in Figure 3(b) present two peaks around 190 K and 250 K, respectively. The signal noise in its left part is due to problems associated with the metal contact at low temperatures. For the simple MOS control sample, the signal consists of the interface charge states between the oxide and Si substrate, and, for the MOS sample with Si NC, except for the above

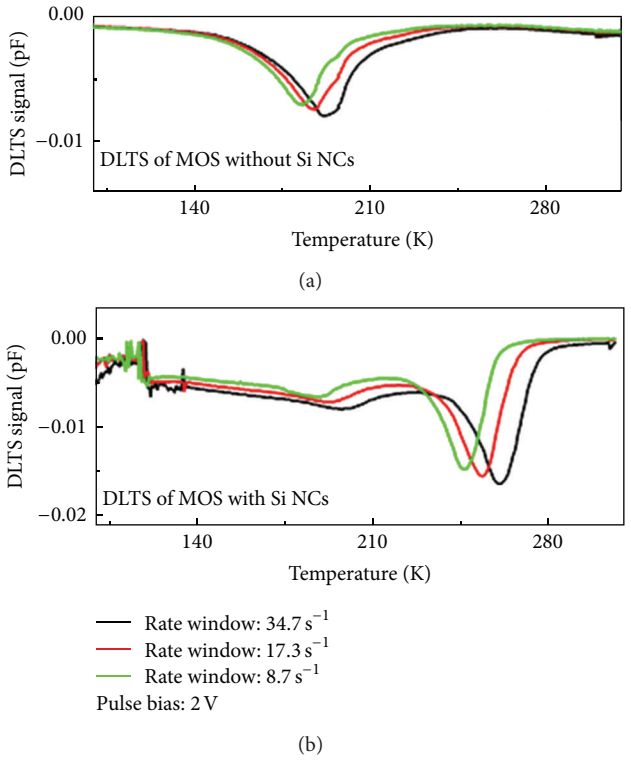

FIGURE 3: DLTS spectra of control sample (a) and sample with Si NC layer (b) dependent on rate window: sample has same thickness, but (a) is the sample without Si NCs and (b) is the sample with Si NCs.

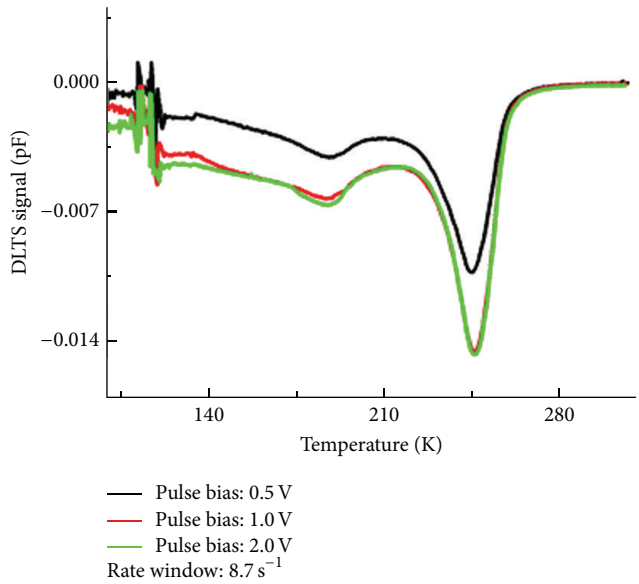

FIGURE 4: DLTS spectra of MOS sample containing Si NCs dependent on fitting pulse bias: as the pulse bias is rising, the transient signal rises too until saturation.

peak, a second and dominant peak appears. It should be related to the charge within the Si NCs. Furthermore, to distinguish whether the charges are stored in the quantum confined conduction band or in deep levels of the band gap in the Si NCs, we tuned the rate window of DLTS to obtain the thermal activation energy and capture cross sections to explain this peak. In Figure 3, we measure the DLTS spectra under three rate windows 34.7, 17.3, and 8.7 s^{-1} by choosing certain t_2 and t_1, and corresponding peak shifts are shown.

Yamasaki theoretically analyzed and measured the bulk traps and interface states in Si MOS diodes [16] and demonstrated the distinction between interface charge and bulk traps. Because the emission rate of bulk traps at a temperature is constant regardless of the pulse bias, the peak temperature and shape of variation of transient capacitance $\Delta(C)$ should not change with pulse bias. We keep the same rate window and constant reverse bias 1 V but variable pulse biases 0.5, 1, and 2 V on the samples. The obtained spectra are presented in Figure 4. The same peak temperature at around 250 K and shape convince us that this trap is probably a bulk trap, unrelated to the interface states. Without applying a pulse bias, the MOS sample is in the accumulation region and electrons are injected from the substrate and stored in the Si NCs. It is well known that these stored electrons alter the electrostatic potential and cause the positive flat-band shift. Therefore, the sample actually is in the inversion region under the pulse bias. Electron emission from Si NCs occurs and contributes to transient capacitance. Similar phenomena were observed by Souifi et al. [11] in their CVD samples. However, the results from Souifi show other noisy peaks in the DLTS spectra, which means there exist trap sites which are different from the Si quantum dots and interface in their oxide, such as hydrogen-related traps in CVD process or defects. Their sample had only a 2 nm tunnel oxide, whereas my sample had a 4 nm tunnel oxide. We believe it is because of high density (>10^{12} cm^{-2}) of Si NCs in our sample, since the tunnel probability is proportional to the total electron emission number. Normally, because of the Si–O bond breaking in the phase separation process, the sample used here might contain some dissociating dangling bonds in the matrix as a deep level, but sufficient heat treatment nucleates them for the crystallization of Si dots, so their amount appears to be below the detection limit of DLTS.

In the case of pulse biases 1 V and 2 V, the DLTS signals at the peak around 250 K are nearly the same, because the stored electrons in Si NCs are fully released under these pulse biases and contribute to the same transient capacitances. From the shape of the DLTS peaks, we consider these deep traps as consistent with the expected discrete behavior of the nanocrystal. We observe the shift of DLTS peak related to Si NCs for different "rate windows." This emission rate shift as function of temperature will be presented in the Arrhenius plot in Figure 5. The different DLTS peaks have their own corresponding temperature T, so the Arrhenius plot is used to determine the parameters of the trap center in Figure 5. We can find the value of carrier velocity $\nu_{n,p} = 10^7$ cm/s and $N_c = 8.4 \times 10^{18}$ cm^{-3} from the literature [17] and use them in (1).

For measuring E_f and σ, we fitted the Arrhenius plot in Figure 5, according to (1). The calculated activation energy E_t of the main peak is about 0.56 eV. Using this value and the above value of $m*$, $\nu_{n,p}$, and N_c in (1), the capture cross section is about 1–7 $\times 10^{-13}$ cm^2.

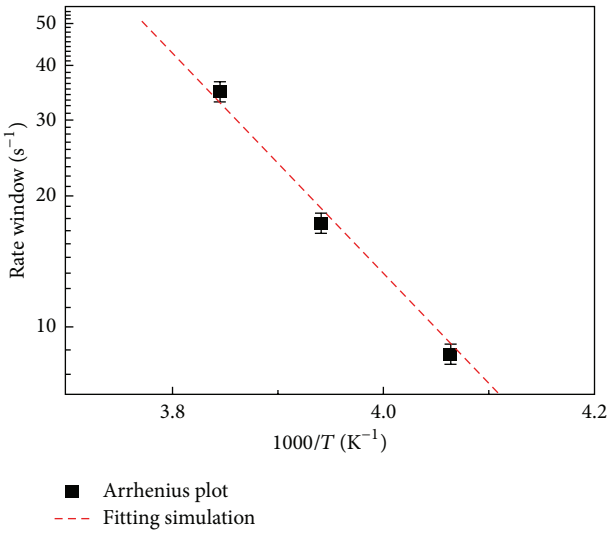

FIGURE 5: The Arrhenius plot of MOS sample containing Si NC, together with parameter simulation.

The feature of DLTS is transient capacitance signal which is captured for the emission of deep energy state by bulk trap; however so far there is almost no DLTS data available for the defect-related emission, such as oxygen related defect, but few teams did comprehensive researches for Si NC related defects within matrix, using time-resolved PL or high frequency *C-V* measurements. Their results show that the intrinsic properties of Si NC related defects are not the same as what we obtain from DLTS measurements.

These calculated results are much larger than the counterparts of trap impurities associated with the deep levels of silicon band gap but are adjacent to the values of Si NCs in the SiO_2 matrix, such as the obtained potential barrier of Si NCs by our method to SiO_2 insulator is 1.6 eV in previous *I-V* characterization [18]. Biteen et al. [19] and Kovalev et al. [20] showed that the large cross section of silicon NCs is at the 10^{-13} cm^2 level and is much larger than the cross section of usual deep level trap centers. Silva et al.[21] confirmed the large capture cross section of Si NCs in a dielectrics matrix as well. In contrast, interfacial traps or single dangling bands are mainly located at the gap center with a capture cross section of 10^{-15} cm^2–10^{-17} cm^2 [22]; in particular Lin shows that the lifetime of time-resolved PL for novel oxygen vacancy defect is shortened to 26–3.6 ns level and cross section is about above value [23]. This was demonstrated by the conductance method measurements in previous research [18]. We guess that the SiO/SiO_2 superlattice way has less oxygen content and less oxygen-related radiative defects, compared with other fabrication ways, such as Si-ion implantation or PECVD-grown Si rich SiO_x film, because SiO will take phase separation to break Si–O band and form stable SiO_2 dielectric film and Si nanocluster, so in the corresponding PL spectra we only observe light intensity around near-IR range, other than what was observed at Lin's paper having defect PL at 415, 420, and 520 nm, respectively [24].

Here we could see clear different cross sections of defect-related deep level and Si NC's own deep level within dielectric matrix. The capture cross section is an important parameter for memory operation; a reduced capture cross section and Coulomb blockade will result in lower programming speed and saturation V_T. The larger capture cross sections of Si NCs not only benefit nonvolatile memory operation but also play a key role as a sensitizer in the E_r doped silicon dioxide containing Si NC system.

4. Conclusions

In summary, using DLTS, we were able to observe thermal emission from Si NC around 300 K for certain rate windows. From our estimates for some intrinsic parameters of the DLTS curve, such as capture cross section σ at 10^{-13} cm^2 level and activation energy E_t at about 0.6 eV for our size-controlled Si NC inside MOS structure, we concluded that these data are consistent with the properties of Si NCs which were measured by optical methods, such as photoluminescence Auger saturation [20]. These results could be a clue that the trapping mechanism in MOS systems containing Si NCs is related to the quantum levels of the Si quantum dots at around 300 K. This trapping mechanism also is suitable for other types of quantum dots embedded in the dielectric matrix as a system. DLTS supplied information other than obtained as high frequency *C-V* measurement on other electrical characterizations.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Authors' Contribution

Dr. Tiezheng Lv and Dr. Lili Zhao have equal contribution to this paper.

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