A paralleland series network structure was introduced into the design of the high-voltage single-chip (HV-SC) light-emitting diode to inhibit the effect of current crowding and to improve the yield. Using such a design, a 6.6×5 mm\(^2\) large area LED chip of 24 parallel stages was demonstrated with 3 W light output power (LOP) at the current of 500 mA. The forward voltage was measured to be 83 V with the same current injection, corresponding to 3.5 V for a single stage. The LED chip's average thermal resistance was identified to be 0.28 K/W by using infrared thermography analysis.

1. Introduction

The compound semiconductor GaN is a promising material for blue-green light-emitting diodes (LEDs) and construction of white light sources. LEDs have numerous applications [1, 2]; thus they have attracted considerable attention. Commercialized LEDs are now being used in many areas such as general illumination [3], signaling, and back lighting in liquid crystal displays [4]. However, high-power LEDs used in projector, fluorescence microscopy, and general lighting still require much of research effort.

There are several methods proposed to improve LED's performance based on two aspects. One is to enhance the quantum efficiency of GaN materials such as insertion of an AlN interlayer [5], low temperature GaN [6] for stress reduction, patterned sapphire substrates (PSSs) [7], epitaxial lateral overgrowth (ELOG) [8], and some other modified ELOG techniques [9]. Another is to improve the LED's efficiency droop, such as suppression of Auger recombination [10], polarization matched GaN [11], and insertion of electron blocking layer (EBL) [12]. As a common sense, the most direct approach to improve the optical power is to enlarge the chip's size. Alternating-current light-emitting diodes (AC-LEDs) [13] and high-voltage LEDs (HV-LEDs) [14] with serial connection structure were demonstrated to overcome low light extraction efficiency (LEE), poor current spreading, and serious luminous efficiency droop. However, AC-LEDs waste half of the active area and HV-LEDs are out of work if one of the LED cells becomes open circuit. Furthermore, an even larger area LED needs a special design to make sure that the LED chip has a high product yield. In particular, with the design in this work, the cost of the package for traditional HV-LEDs and AC-LEDs used as module can be reduced. And it will lead to a more compact lighting system for applications.

Recently, we fabricated a high-voltage single-chip large area (6.6 × 5 mm\(^2\)) green LED with 3 W light output power. In this paper, the electrical and optical properties of this green LED are presented. The 2-dimensional junction temperature distribution was also analyzed.
overcome the current crowding effect. As shown in Figure 1, the HV-SC LED chip consists of 24 parallel stages connected in series, and each stage has 24 small LED cells in parallel connection. The size of a small LED cell is 200 × 200 μm².

In this work, the InGaN/GaN LED wafer was acquired commercially from Xiangneng Hualei Optoelectronic Co. Ltd. with a wavelength of 520 nm. After the cleaning of GaN epilayer, a SiO₂ hard mask layer for isolation region etching and mesa etching was deposited on the p-type GaN layer using plasma-enhanced chemical vapor deposition (PECVD, Oxford System 100). After the SiO₂ mask was patterned, the isolation etching and mesa etching were carried out, respectively, by an inductively coupled plasma (ICP) system (Oxford ICP 180). A sidewall slope of approximately 45° was selected to form on the GaN epilayer for smooth coverage of interconnect metal. A dielectric layer of 200 nm SiO₂ was then deposited, and the RIE dry etching was carried out to open the dielectric window. After that, an indium tin oxide (ITO) film was deposited and wet-etched to form n-contact. An Al back reflector was sputtered on the back of the sapphire substrate after polishing down to 150 μm. The chip was mounted on an Al based heat sink by the soldering, and a hemispherical borosilicate glass lens with 13 mm diameters was covered on the chip by KER2500 AB silicone.

### 3. Results and Discussion

Figure 2 shows the typical I-V characteristics of the fabricated HV-SC LED evaluated by Keithley 4200. The measured forward voltage is 83 V, corresponding to 3.5 V for each parallel stage at 500 mA. A reverse leakage current of 8 nA is measured at −120 V, confirming the advantage of suppressing reverse leakage current in the series connected HV LED chips compared with the single parallel stage, whose reverse current is several microamperes at −5 V.

The optical properties of a HV-SC LED were measured by Everfine HAAS 2000 spectrometer with a large integrating sphere of 1.5 m inner diameter. A fan of −1 W was set at the back of the device for cooling. Figure 3 presents a luminous photo of the LED driven at 10 mA, and the LOP and external quantum efficiency (EQE) varying with injection current. As shown in Figure 3(b), the green light output power was measured to be 3 W at 500 mA, and the EQE was calculated to be 12.6%, which is 44.2% lower than its peak value of 22.6% at 35 mA. The light output power provided by the wafer suppliers was about 60 mW at the current of 350 mA for the chip size of 30 × 30 mil². The 9% EQE of the HV-SC LED agreed with the reference value of 8.9% calculated by the parameters for the wafers, at the same current density, without lens.

Infrared thermography analysis using QFI InfraScope II was also carried out to display the junction temperature distribution and calculate the average junction temperature. The HV-SC LED chip was mounted on a thermostatic plate with a constant temperature of 23°C by thermal conductive silica gel.

Figure 4 shows the 2D junction temperature distribution on the chip area highlighted by the red dashed line, as indicated in Figure 1. Due to the heat crowding effect, the junction temperature at the center is higher than that at the periphery. The temperature profile along the red line from bottom to top in Figure 1 is plotted in Figure 5. The temperature at the center (Tc) is about 36.8°C, while the temperature at the edge (T₀) is about 30.7°C.

To evaluate the heat dissipation capacity of this large area LED chip, the average thermal resistance (Rᵢx_Average) and the peak thermal resistance (Rᵢx_Peak) should be considered. They can be calculated by the following equation (see [15]):

\[
R_{IX} = \frac{T_J - T_a}{P_H},
\]

where Rᵢx, T_J, T_a, and P_H are the thermal resistance, the junction temperature, the ambient temperature, and the heat dissipation power, respectively. T_J was 33.8°C and 36.8°C for Rᵢx_Average and Rᵢx_Peak, respectively. So, Rᵢx_Average and Rᵢx_Peak were evaluated to be 0.28 K/W and 0.36 K/W, corresponding to
Figure 3: (a) The luminous photo of a HV-SC LED with optical lens driven at 10 mA and (b) the LOP and external quantum efficiency (EQE) of the HV-SC LED.

Figure 4: 2D junction temperature distribution in the red dashed line highlighted area in Figure 1.

Figure 5: The chip's temperature and fitting curve along the red line from bottom to top in Figure 1.

So the junction temperature spatial distribution leads to the forward current density spatial distribution. For a junction temperature distribution as shown in Figure 5, the current density at the center of the chip \( J_c \) should be higher than that at the edge \( J_e \), implying a current crowding effect. It should be noted that the small LED cells along the red line, as shown in Figure 1, are connected in parallel. The ratio of \( J_c/J_e \) represents the extent of the current crowding. In practice, when this ratio \( \leq e \) (Euler's number), the device is considered appropriately designed [3].

According to (3), the ratio of \( J_c/J_e \) can be expressed as

\[
\frac{J_c}{J_e} = \left( \frac{T_c}{T_e} \right)^{3+\gamma/2} \frac{\exp \left( q (V - I_c R_s - V_i) / n_{\text{ideal}} k T_c \right)}{\exp \left( q (V - I_e R_s - V_i) / n_{\text{ideal}} k T_e \right)},
\]

where \( T_c \) and \( T_e \) were found to be 36.8°C and 30.7°C, respectively, in Figure 5. \( V_i \) is estimated to be 3.4 V in \( \text{In}_{0.3} \text{Ga}_{0.7} \text{N} / \text{GaN} \) QWs [17] and \( \gamma \) is regarded as 2 to evaluate the maximum value of the \( J_c/J_e \) ratio. As a result, the ratio of \( J_c/J_e \) was estimated less than 1.029, which is much less than \( e \) (~2.72), indicating no obvious current crowding effect, thus validating the effectiveness of the chip design.

According to (2), for the heat flow through the plate with the constant cross-sectional area, the average thermal resistance can also be calculated by

\[
R_T = \frac{1}{\kappa} \cdot \frac{L}{A},
\]

where \( R_T \) is the average thermal resistance, \( \kappa \) is the thermal conductivity, \( L \) is the chip’s thickness, and \( A \) is the area. The average thermal resistance of the HV-SC chip was calculated to be 0.26 K/W, 0.02 K/W higher than the calculated result because of the heat crowding effect and the additional thermal resistances of the silica gel and the heat sink.

It is well known that the forward current density of an LED strongly depends on the junction temperature, as shown in the following equation (see [16]):

\[
J \propto T^{3+\gamma/2} \exp \left( \frac{q (V - I R_s - V_i)}{n_{\text{ideal}} k T} \right).
\]
4. Conclusion

In this study, we introduced a parallel and series network structure into the design of a large area high-power LED chip, which suppresses the effect of current crowding and enhances the fabrication yield of the LED chip. We also successfully demonstrated a 6.6 × 5 mm² large area HV-SC green LED array of 24 parallel stages. With a driven current at 500 mA, the forward voltage was measured to be 83 V, 3.5 V for each stage, and 3 W light output power with an EQE of 12.6%. Based on the infrared thermography analysis, the measured average thermal resistance was 0.28 K/W and the self-heating induced current crowding is negligible. Such a high-power, high-voltage LED device has a great potential in RGB solid state lighting.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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