

## Research Article

# Investigation of In Situ Boron-Doping in SiGe Source/Drain Layer Growth for PMOS Devices

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Embedded SiGe (eSiGe) source/drain (S/D) was studied to enhance PMOS performance. Detailed investigations concerning the effect of GeH<sub>4</sub> and B<sub>2</sub>H<sub>6</sub> gas flow rate on the resultant Boron-doping of the SiGe layer (on a 40 nm patterned wafer) were carried out. Various SiGeB epitaxial growth experiments were realized under systematically varying experimental conditions. Key structural and chemical characteristics of the SiGeB layers were investigated using Secondary Ion Mass Spectroscopy (SIMS), nanobeam diffraction mode (NBD), and Transmission Electron Microscopy (TEM) itself. Furthermore,  $I_{on}/I_{off}$  performances of 40 nm PMOS transistors are also measured by the Parametric Test Systems for the semiconductor industry. The results indicate that the ratio between GeH<sub>4</sub> and B<sub>2</sub>H<sub>6</sub> gas flow rates influences not only the Ge and Boron content of the SiGeB layer, but also the PMOS channel strain and the morphology of the eSiGe S/D regions which directly affect PMOS performance. In addition, the mechanism of Boron-doping during SiGe layer growth on the pattern wafer is briefly discussed. The results and discussion presented within this paper are expected to contribute to the optimization of eSiGe stressor, aimed for advanced CMOS devices.

## 1. Introduction

Implementation of embedded SiGe (eSiGe) as source/drain (S/D) has emerged as an attractive strategy for boosting device performance in PMOS transistors to technology nodes like 40 nm logic node and beyond. This is primarily connected with the ability of eSiGe to strain engineering of the PMOS channel [1]. eSiGe essentially works by enhancing hole mobility in the PMOS channel, by inducing a uniaxial compressive stress that arises out of the lattice mismatch between the substrate (Si) and the eSiGe layer. In the last decade, optimization of the misfit strain, by increasing Ge concentration in eSiGe, has met enormous success [2–5]. Simultaneously, in situ Boron-doping during SiGe epitaxial growth has also been widely researched, mainly due to its inducement of low sheet resistance in the S/D regions [6–9]. On the other hand, reports have also suggested that Boron-doping can actually bring out strain relaxation in the channel, termed as the *strain compensation effect* [10]. Boron-doping essentially reduces lattice mismatch between the Si and the SiGe layer, since Boron has a smaller atomic

radius as compared to that of Si. Though there is a lot of literature on SiGeB growth, few works relate to SiGeB growth on the pattern wafer. Hence there is a need to conduct a rigorous investigation into the growth factors surrounding Boron-doped SiGe on the pattern wafer, with a focus on key structural and chemical characteristics. This paper studies the effect of GeH<sub>4</sub> and B<sub>2</sub>H<sub>6</sub> gas flow rate on Boron-doping of SiGe film, deposited on a 40 nm patterned wafer. It includes investigating Ge and Boron content in a SiGeB film, along with observation of channel strain and morphology of the S/D regions. Moreover, the  $I_{on}/I_{off}$  performances of 40 nm PMOS transistors were analyzed. In addition, the mechanism of Boron-doping during SiGe growth is briefly discussed.

## 2. Experiments

Figure 1 shows a schematic diagram, depicting the S/D regions of the fabricated 40 nm PMOS transistors. Different planar PMOS devices were fabricated on a bulk silicon substrate (diameter: 300 mm), according to the following

TABLE 1: Key characteristics of the fabricated Boron-doped SiGe bulk samples.

	Sample number				
	#1	#2	#3	#4	#5
GeH <sub>4</sub> flow rate (sccm)	520	400	360	400	400
B <sub>2</sub> H <sub>6</sub> flow rate (sccm)	60	60	60	70	40
GeH <sub>4</sub> /B <sub>2</sub> H <sub>6</sub> flow rate ratio ( $R$ )	8.67	6.67	6.00	5.71	10.00
Channel strain $\langle 2, -2, 0 \rangle$	-0.88%	-1.42%	-0.80%	-0.60%	-1.50%
SiGe bulk Dep rate (nm/min)	20.6	13.2	8.04	17.9	7.9
Ge content in bulk	35%	33%	29%	29%	35%
Boron content in bulk (cm <sup>-3</sup> )	1.60E + 20	1.60E + 20	2.00E + 20	2.00E + 20	1.30E + 20

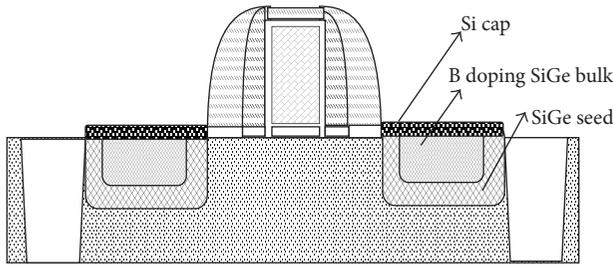


FIGURE 1: Schematic diagram of SiGe S/D area in PFET.

procedure: at first, the channel implantation was performed before the formation of the gate dielectric and the gate electrode. Secondly, the dopants for the lightly doped drain (LDD) were implanted. After that, a 50 nm U-shape trench was etched and a triple-layer epitaxial S/D structure, consisting of a SiGe seed layer (20 nm), a Boron-doped SiGe bulk layer (30 nm), and a Si cap layer (20 nm), was deposited via consecutive selective-epitaxy steps. The epitaxial layers were grown in an AMAT Centura reduced-pressure chemical vapor deposition (RP-CVD) reactor, at growth temperature and pressure of 600°C and 10 torr, respectively. Dichlorosilane (SiH<sub>2</sub>Cl<sub>2</sub>) was used as a gas source for Si, whereas 10% germane (GeH<sub>4</sub>) and 1% diborane (B<sub>2</sub>H<sub>6</sub>) were used as gas sources for Ge and Boron, respectively (with H<sub>2</sub> acting as a carrier gas). HCl was used as the etchant to provide the necessary selectivity during the SiGe deposition process. We have performed different experiments by exploiting a wide range of GeH<sub>4</sub> and B<sub>2</sub>H<sub>6</sub> gas flow rates during the growth of the Boron-doped bulk layers, while keeping all the other process parameters constant. On the other hand, PMOS transistors with eSiGe S/D were formed on the device wafers using the same SiGe epitaxial conditions as mentioned above.

Immediately following the growth of the triple layered epitaxial process, Ge and Boron contents of the SiGeB layer were directly analyzed using a Secondary Ion Mass Spectrometry setup (SIMS; Camera 4F). The PMOS channel strain was measured using the nanobeam diffraction mode (NBD, FEI Tecnai G2 F20) within a Transmission Electron Microscopy (TEM) setup. eSiGe S/D morphologies were further analyzed by TEM (JEOL JEM-2100F). Besides, after the device wafers were fabricated, the universal curves

( $I_{\text{dsat}}$  versus  $I_{\text{off}}$ ) were measured by the Parametric Test Systems for the semiconductor industry (Agilent, 4082F).

### 3. Results and Discussions

Table 1 lists the key growth parameters for different Boron-doped SiGe bulk layer samples, fabricated using different GeH<sub>4</sub> and B<sub>2</sub>H<sub>6</sub> gas flow rates. Also, the estimated Ge and Boron concentrations are listed, along with the SiGeB growth rates, as calculated from the SIMS data. It was found that as GeH<sub>4</sub> flow rate increased while B<sub>2</sub>H<sub>6</sub> flow rate was kept constant, the Ge content of the SiGeB film increased while Boron concentration decreased. In addition, the growth rate of SiGeB layer was promoted (sample #1~#3). On the other hand, as B<sub>2</sub>H<sub>6</sub> flow rate increased while GeH<sub>4</sub> flow rate was fixed, the Boron concentration of the SiGeB layer apparently increased, while Ge content decreased (sample #2, #4, and #5). Besides, the growth rate of SiGeB improved. These observations are in agreement with a similar work reported in literature [11].

The NBD mode in TEM has emerged as a powerful technique for measuring strain with a nanoscale resolution [12]. The mechanism of NBD along with the related estimation method has been clearly established in literature [13]. Strain along the  $\langle 2, -2, 0 \rangle$  channel direction was measured by NBD. The nanoscale NBD probe measured the strain values along a cross section beginning from the gate oxide to the unstrained Si substrate (red arrow; Figure 2(a)), utilizing a line scan mode. The negative strain values refer to a compressive strain, which is what actually enhances the PMOS mobility. Figures 2(b) and 2(c) show the strain curves of the SiGeB film with different GeH<sub>4</sub> and B<sub>2</sub>H<sub>6</sub> gas flow rate, respectively. Apparently, the channel shows maximal compressive strain, which is generally 0–10 nm below the gate oxide (red circles; Figures 2(b) and 2(c)) in contrast to the unstrained Si substrate (strain = 0) in all the samples. In order to further understand the influence of gas flow rates on the SiGeB film growth, ratio  $R$  is defined as the ratio of the flow rate of GeH<sub>4</sub> to that of B<sub>2</sub>H<sub>6</sub>. From NBD result of the 5 studied samples (Table 1 and Figure 2), it was shown that as the value of  $R$  increased, the channel strain in all the samples was monotonously enhanced, with sample #1 being an exception. Based on the fact that Boron induces *strain compensation effect*, it can be argued that higher Boron concentration in SiGe layer will decrease the compressive strain in the channel.

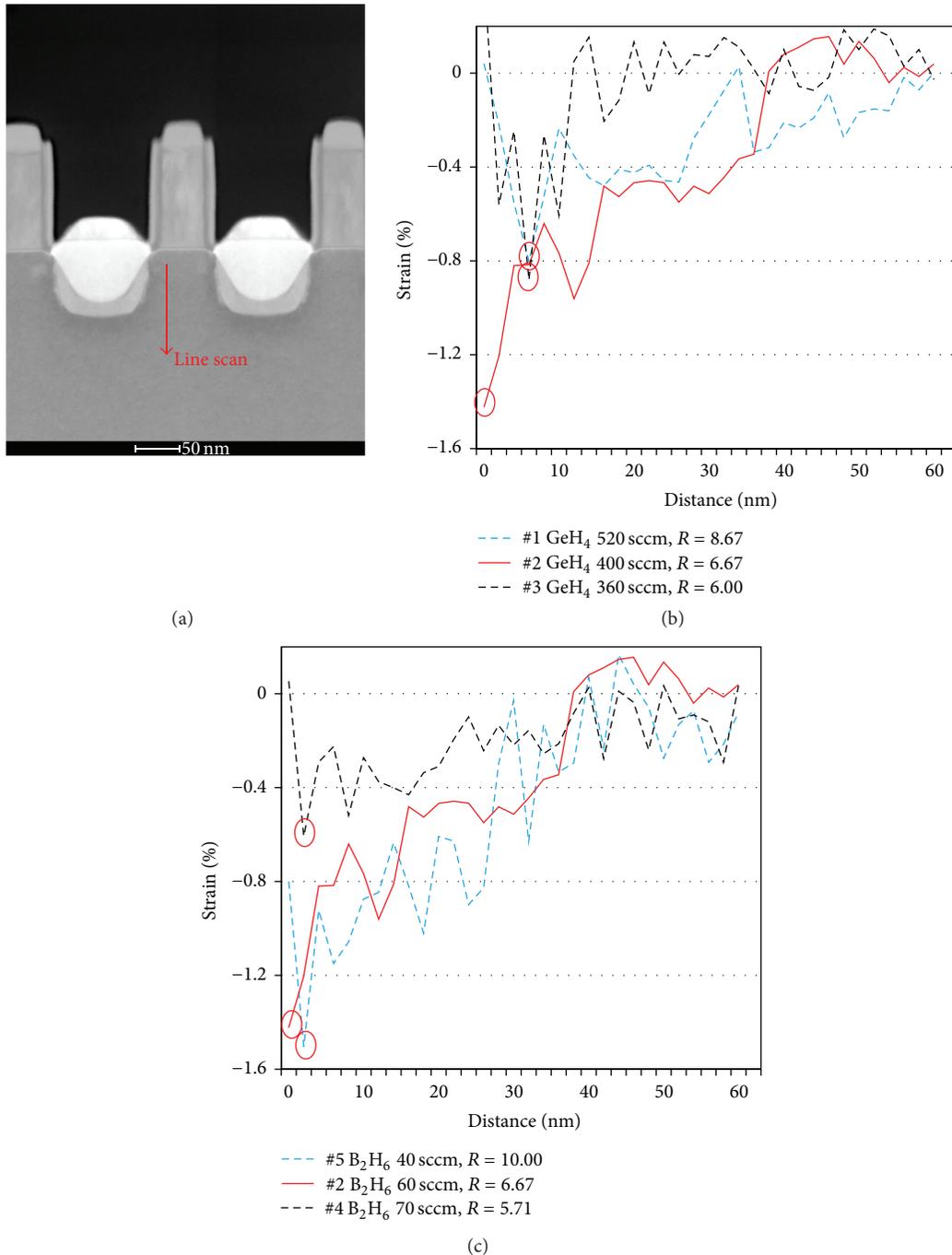


FIGURE 2: (a) TEM morphology along the cross section of sample #2 ( $R = 6.67$ ). (b) Strain curves along the  $\langle 2, -2, 0 \rangle$  channel direction for samples with varying GeH<sub>4</sub> flow rates. (c) Strain curves along the  $\langle 2, -2, 0 \rangle$  channel direction for samples with varying B<sub>2</sub>H<sub>6</sub> flow rate.

Therefore, increasing  $R$ , which corresponds to the increment in the content of Ge over Boron in the SiGeB layer, leads to improvement in the channel strain. A possible reason for the anomalous reduction in channel strain for sample #1 is the extremely high SiGeB growth rate associated with it. High growth rates can result into defects such as stacking fault or threading dislocations in the SiGeB film. As a consequence of this, the compressive strain in the channel could be partly relaxed, lowering the effective channel strain. Furthermore,

TEM image of sample #1 was shown in Figure 3. Obvious threading dislocations appeared in the SiGeB film, which confirmed our previous speculation.

Increasing  $R$  seems to be increasing the PMOS channel strain, which could be associated with the absence of any strain relaxation. However, besides this, the morphology of the eSiGe S/D regions also has to be considered for the SiGeB growth on the pattern wafer. Figures 2(a) and 4 show the morphology of the eSiGe S/D regions for sample #1, #2, and

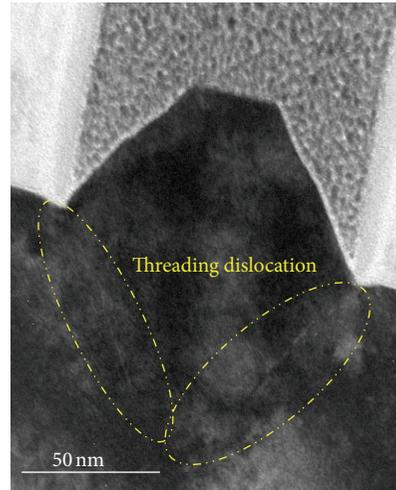


FIGURE 3: TEM morphology of sample #1 (threading dislocation appeared in the SiGeB film).

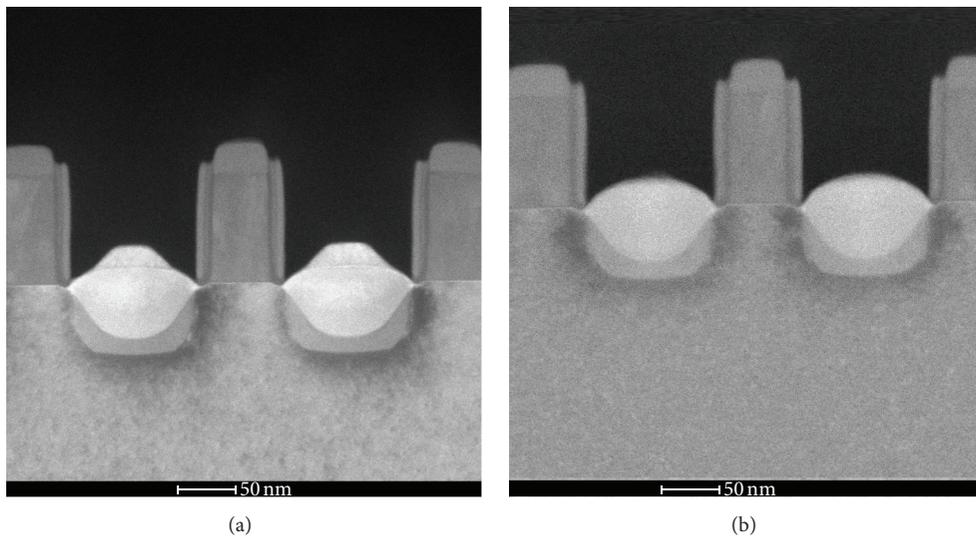


FIGURE 4: TEM image of the cross section of sample (a) #1 ( $R = 8.67$ ) and (b) #5 ( $R = 10.00$ ).

#5, respectively. Obviously, the Si capping layer can fully cover the SiGeB bulk layer for  $R = 6.67$  (Figure 2(a)). It was found that when the value of  $R$  increases ( $R = 8.67$  and  $R = 10$  for sample #1 and #5, resp.), the Si cap coverage of the SiGeB bulk layer becomes accumulatively sparse. When  $R = 8.67$  (sample #1), the edges of the SiGeB layer were not covered by the Si capping. In case of  $R = 10.00$  (sample #5), Si capping on the SiGeB bulk layer entirely disappears. It has been reported that a Si capping layer above the SiGeB bulk layer, which acts as a precursor for postsilicide formation, can actually improve S/D sheet resistance [14]. In the absence of this Si capping layer, the nickel germanosilicate, formed by consuming the SiGeB bulk layer during the silicide formation process, could induce higher S/D sheet resistance and strain relaxation in the SiGeB layer. The root cause of the poor covering of Si capping layer can be explained in terms of the difference existing between the lattice constant of SiGe and Si. When

the value of  $R$  is high, the higher Ge content leads to a higher dispersion in the lattice constants of SiGeB and Si. Thus, Si epitaxial growth on the SiGe surface, especially on the (110) facet, is rendered relatively difficult as compared to that on the identical Si surface. In order to improve the Si epitaxial growth on the SiGeB layer, the nucleation activation energy of Si capping deposition has to be enhanced by employing strategies like higher growth temperature, and so forth.

Additionally, the transistors performances were compared with and without Si capping on the SiGeB S/D regions (sample #2 and #5 epitaxial condition, resp.). The  $I_{\text{dsat}}$  currents were extracted under  $I_{\text{off}} = 100$  nA from the universal curves ( $I_{\text{dsat}}$  versus  $I_{\text{off}}$  plot) of 40 nm PMOS transistors (as shown in Figure 5).  $I_{\text{dsat}}$  current was increased from  $418 \mu\text{A}/\mu\text{m}$  to  $486 \mu\text{A}/\mu\text{m}$ . A 16.2% performance improvement was achieved, attributed to lower S/D sheet resistance of the PMOS transistor with Si capping. Lower S/D resistance

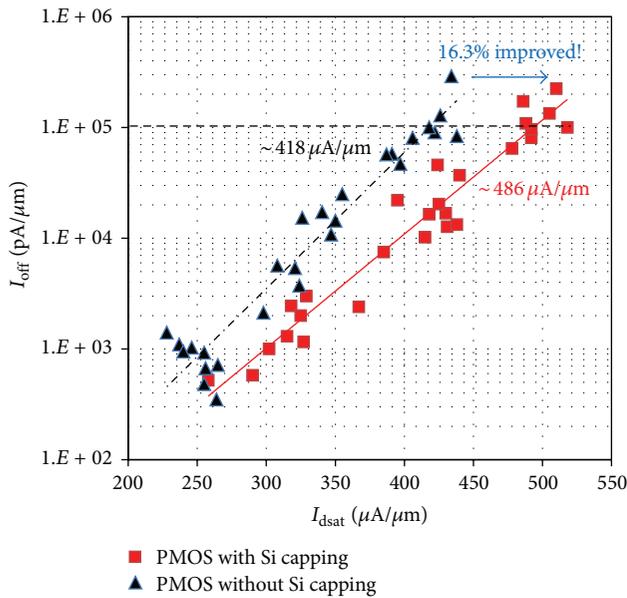


FIGURE 5: Universal curves ( $I_{\text{dsat}}$  versus  $I_{\text{off}}$  plot) for 40 nm PMOS transistors with and without Si capping on SiGe bulk.

indicates the on-resistance of a PMOS transistor ( $R_{\text{on}}$ ), which leads to the enhancement of  $I_{\text{dsat}}$  when  $V_{\text{ds}}$  is fixed. The above explanation illuminated the significance of good morphology of eSiGe S/D regions.

In a word, it should be noticed that the growth mechanism of SiGeB on the pattern wafer is more complicated compared to that on the blanket wafer, since the structural and chemical characteristics of the SiGeB are sensitive to the growth parameters. According to Section 3, ratio  $R$  should be considered as a key parameter instead of the individual  $\text{GeH}_4$  and  $\text{B}_2\text{H}_6$  flow rates. A moderate value of  $R$  can result into large channel strain and a good morphology of the eSiGe S/D regions, which ultimately eliminates any strain relaxation and also suppresses sheet resistance in the S/D areas. As a result, improved effective PMOS performance can be acquired. As the presented study, sample #2, which has moderate  $R$  (6.67), shows remarkable channel strain ( $-1.42\%$ ) along with a good Si capping coverage.

#### 4. Conclusions

In summary, the parameter  $R$  (the ratio of the gas flow rates of  $\text{GeH}_4$  and  $\text{B}_2\text{H}_6$ ) was demonstrated to have a crucial influence on the channel strain and S/D region morphologies of a PMOS. This ultimately affects the effective device performance of a 40 nm PMOS transistor. It was established that a moderate  $R$  value has to be chosen in order to obtain large enough compressive channel strain, along with a good morphology in the S/D areas. In addition, the S/D sheet resistance and strain relaxation issues which were addressed in this work could be considered for integration into the PMOS fabrication process. An exhaustive understanding of the growth mechanism of the Boron-doped SiGe layer on the pattern wafer was also presented. The conclusions might

serve as a useful reference for improving the eSiGe stressor performance, which could eventually lead to optimizations for advanced CMOS devices.

#### Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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