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Review Article

Incorporation of Ge on High *K* Dielectric Material for Different Fabrication Technologies (HBT, CMOS) and Their Impact on Electrical Characteristics of the Device

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The paper is composed of distinct reviews on various fabrication technologies of the CMOS family and the characterization of MOS capacitors. The initial part of the article essentially presents a systemic review on an already conducted work on different fabrication technologies such as Si MOSFET, SiGe HBT, and InP HBT. Device and circuit-level performance for broadband and tuned millimetre-wave applications is discussed in detail relative to the underlying CMOS technologies. The comparison is made for various performance metrics for 180 nm, 130 nm, and 90 nm n-MOSFET devices for SiGe and InP HBTs. In the latter part of the study, a comprehensive review on a previously conducted research on electrical and physical characterization of metal-oxide-semiconductor (MOS) capacitors fabricated on a 2.5 μm epitaxial germanium layer grown on (100) silicon substrate is undertaken. The focus and crux of the study is the influence of germanium surface preparation on MOS electrical characteristics. It is observed that predielectric (HfO) deposition annealing in NH_3 ambience results in the performance upgradation in critical and key parameters such as equivalent oxide thickness and the gate leakage current.

1. Introduction

The dielectric constant or dielectric strength (k) is an important parameter in the design of an electronic device especially in the perspective of CMOS fabrication technology. It has technological implications. The device which has been of scientific interest due to its inherent properties of scaling, high capacitance, and stronger electric field is in the integration of high K and metal gate on top of the substrate and is known as the metal-oxide-semiconductor (MOS) device. By establishing the value of dielectric constant "k" (Capcha), charge storing capability can be determined and subsequently the capacitance (C) for the device.

Shown in Figure 1 is the high K+ metal gate structure modelled as a parallel plate capacitor. It is used as an alternative to standard poly-Si/SiO_2 structure.

The structure is assembled in a way that metal is the top layer followed by the oxide layer and finally the semiconductor layer [1]. Hence, the name MOS is realised. It is to be noted that the oxide layer is replaced by a dielectric while the metal gate is replaced by the polysilicon in recent time.

The capacitance formed by the metal gate and the semiconductor with the dielectric in between the two is given by

$$C = \frac{\epsilon_0 k A}{d}, \tag{1}$$

where C is the capacitance between the metal gate and the semiconductor substrate, k is the dielectric constant or relative permittivity of the dielectric medium, ϵ_0 is the

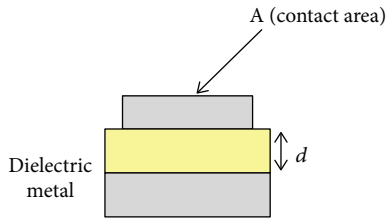

Figure 1: High K+ metal gate [1].

permittivity of free space, and d is the thickness of the dielectric medium between the plates.

Dielectric constant "k" is the defining parameter in determining the capacitance in the above structure as the area of cross section (A) and thickness (d) of the structure cannot be manipulated so the only option is to change the value of k. For a stronger electric field, the value of k value must be high owing to proportionality.

To determine the standard for a high k and low k dielectric, the dielectric value of SiO_2 is referenced which is 3.9. So, we get two categories, shown in Table 1.

However, there are some applications where both high k electric and low k dielectric materials are required for proper functionality.

2. Need of a High K Dielectric

The scientific and technical reasons for the use of high K dielectrics in the Si-CMOS industry are its high capacitance, equivalent oxide thickness (EOT), high permittivity, and greater control over the conduction channel between source and drain. In order to maintain the gate capacitance sufficiently large, high k dielectric materials are utilised. The metal gate is used in conjunction with high k materials. Since in MOS devices, because of scaling of channel length (L) the gate area (A) is reduced in order to maintain the high value of capacitance in the face of ever-reducing gate thickness, a high k dielectric is used. There is a limit to scaling in the nm regime; gate oxide becomes so thin and it will stop acting as an insulator because the phenomena of tunnelling take place, resulting in leakages. In advanced CMOS/MOS IC design technology, dielectrics with values of $k > 3.9$ are used.

3. Literature Review

In the pursuit of enhanced materials with conducive properties, research was continued and discovery of new material was made. The researchers found that germanium on silicon possessed better conductivity properties and performance as compared to isolated silicon and germanium. The integration of germanium with a high K material is not a limitation because of the compatibility of germanium with high k material [2]. For the future advancement of gate stacks of MOSFETs, germanium is required to be optimized for seamless integration with the high K dielectric. In [3], the results of P-MOSFET (fully depleted) are discussed and extended for GeOI with a 200 mm wafer. It was shown in [4] that the substrate was fabricated on the wafer by using state-of-the-art smart-cut technology resulting into germanium on silicon or GOS. In [5], a detailed study was carried on high K/metal (HfO_2/TiN) gate stacks for GOS electrical properties. The effects on the electrical characteristics when the germanium surface is deposited on MOS are quiet pronounced. The leakage current is also taken into consideration for the device.

Table 1: Dielectric category [1].

K value	Dielectric
<3.9	Low
>3.9	High

For the last few years, interest in the millimetre wave has been increasing, and conclusion has been made in the light of an increase in the number of research publications. As this field is sparked by the automotive radar and because of the radar market, the interest in the mm wave has increased [6].

Research work on the performance of a 0.13 mm SiGe and BiCMOS technology has been presented in [7] along with the implementation of the circuit in broadband in BiCMOS technology. In [8], the comparison of the three technologies, namely, Si MOSFET, InP HBT, and SiGe, has been made. In [9], the study on the transistor design and application considerations is made for 200 GHz SiGe HBTs.

One of the MOSCAP-based silicon photonic modulators is a device named silicon insulator silicon capacitor (SISCAP) [10], which is a device that consists of a gate oxide layer, SOI layer of n-type, and poly-Si layer p-type. A single-mode optical waveguide is formed by overlapping SOI layers and poly-Si with optical mode-centred gate oxide. The main advantage of SISCAP is that its gate oxide provides higher charge densities. An efficient MOSCAP-based silicon modulator and CMOS drivers for optical transmitters are discussed in [10].

The interest in the field of photonics based on silicon is on the rise because of diverse optical communication applications. Some of the attributes of such devices are that they are less power-intensive, they have cheaper cost, and they occupy lesser area.

With the CMOS scaling regime together with the advancement in advanced electronic fabrication protocols and advent of nanotechnology, nanostructures with attributes of short-channel effects surpassed the Si CMOS conventional devices in terms of performance and efficiency [11] (Figure 2).

In [12, 13], the benefits of using silicide as a source and drain region are emphasized; it signifies the benefits of using silicide such as low parasitic capacitance, ease of fabrication, and low thermal response.

In [14, 15], it is shown that silicide is compatible to be used as a high k dielectric material because of its high temperature compatibility since silicide is compatible to be used as a high k dielectric and metal gate stacks as till the temperature of 700°C.

In [16], a drawback of employing silicide is highlighted which is due to the drop of potential on the drain side. The device performance is affected in case of low voltage at the

drain. In order to resolve this defect, a solution is proposed which involves the use of those silicates whose Schottky barrier is low, for instance, the use of erbium silicide [17].

If we look into the leakage current of conventional devices related to CMOS and MOSFET in comparison to the Schottky barrier, it is observed that the MOSFET leakage current is higher in comparison to CMOS devices [17, 18].

In designing the high k dielectric oxide layer in the gate stack, the thickness of the gate oxide is very important because the gate voltage controls the current injection [19]. In the MOSFET (Schottky tunnelling source) mode of operation, the tunnelling barrier is controlled by channel and the source silicide.

4. Sample Preparation

From the paper, MOS capacitors were fabricated on germanium grown epitaxially (2.5 μm) on p-type 200 mm (100) Si wafers using a full CMOS process flow. The germanium films were grown directly onto Si (100) using a reduced pressure chemical vapour deposition technique. The thick Ge layers were grown using germanium and low-temperature annealing (400/750°C) process owing to the difference in their mechanical properties such as thermal expansion of Ge and Si resulting in an assymetrical structure of the device.. The threading dislocation density can be as low as $6 * 10^6\,\text{cm}^{-2}$ for annealed 2.5 μm Ge layers. Outward diffusion phenomena are also observed. The surface of Ge thick layers is smooth with the RMS roughness of the order of 1 nm for 2.5 μm thick Ge layers (Figure 3).

For the first time, we report the electrical and physical characterization of metal-oxide-semiconductor (MOS) capacitors fabricated on 2.5/spl mu/m epitaxial germanium layers grown on (100) silicon. These capacitors were made using HfO/sub 2/as the dielectric and TiN as the metal gate electrode. We have studied the influence of Ge surface preparation on MOS electrical characteristics. It is demonstrated that a surface anneal step in a NH/sub 3/ambient before the HfO/sub 2/deposition results in significant improvements in both equivalent oxide thickness (EOT) and the gate leakage current. We show that it is possible to achieve Ge/GeON/HfO/sub 2//TiN gate stacks with an EOT of 0.7 nm and a leakage current of 0.84 A/cm/sup 2/at −2 V gate bias. The better transport properties of Ge and these performances show the interest of Ge and GeOI for the ITRS advanced nodes.

Table 2 shows the samples and their surface preparation with germanium (Ge) with time of cleaning and atmospheric pressure.

4.1. Electrical Results. The C-V hysteresis study [5] was carried out at 300 K with a frequency sweep of 10 kHz up to 900 kHz. These analyses revealed that epitaxial Ge was a p-type material. Figure 4 shows the measured C-V curves on samples SN1-2-3 and SX (area = $20^*20\,\mu\text{m}^2$, sweeping from inversion to accumulation regions). WSP samples conform to nonreproducible results, which endorses the need for a Ge surface preparation manoeuvre. The results for the WSP samples can be attributed to the unstable

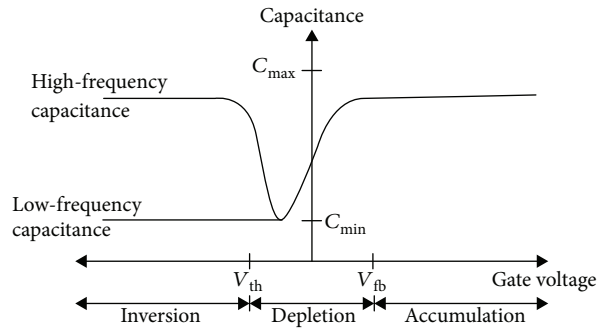

Figure 2: C-V curve for MOSCAP.

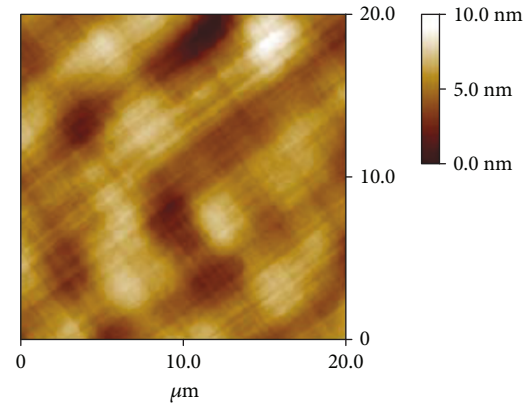

Figure 3: (20*20) μm tapping mode AFM image of the surface of a 2.5 μm thick Ge layer grown on Si (001) that has subsequently submerged, in situ annealing under H2 image sides.

Table 2: Surface treatment performed prior to HfO_2 deposition [5].

Sample	Surface preparation
SN1	Ge cleaning + 2 min – 0.3 Torr
SN2	Ge cleaning + 2 min – 17 Torr
SN3	Ge cleaning + 10 min – 17 Torr
SC	Ge cleaning + 1.5 nm Si capping + chemical oxidation
WSP	Ge cleaning (without surface preparation)

GeO_x layer sandwiched between Ge and HfO_2. Samples SN2 and SN3 exhibit good C-V curves compared to the WSP sample. SN1 exhibits a different behaviour which may be attributed to an incomplete nitridation of the GeO native layer. For the samples with Si capping and chemical oxidation (SC), the C-V curves show two plateaus in the accumulation region; this effect could be due to the presence of the two semiconductors (Si and Ge) leading to a two-step accumulation process.

Capacitance vs. voltage (CV) behaviour is observed for the different samples as shown in Figure 4.

By using the permittivity (relative) of SiO_2, the equivalent oxide thickness (EOT) was calculated at a frequency of 900 kHz corresponding to the accumulation capacitance.

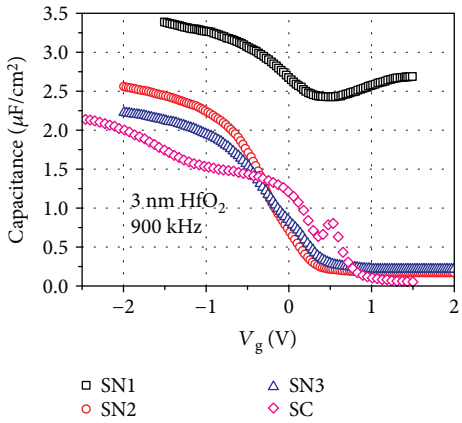

Figure 4: C-V measurement for SN1–4 at 900 kHz [5].

The EOT of the interfacial layer (SiO_2) is estimated to be around 6–7 Å. For the nitrided samples, the EOTs of the interfacial layers are smaller (down to 2 Å for SN1). The dielectric constant (k) and EOT were estimated from the graph of Figure 5. The dielectric constant (k) and EOT value vary by increasing the nitridation time (SN2), the EOT value increases if the partial pressure (NH3) and nitridation time are increased, and the GeO_xN_y layer is affected.

In order to examine the GeO_xN_y Interface XPS investigations have been accomplished on the nitrided samples. Figure 6 shows the GeO_xN_y 3D study (XPS) performed on samples of nitride. The inset peak at 397.7 eV is in line with germanium oxynitride and shows the presence of nitrogen at the Ge/HfO_2 interface. The result is in agreement with [20].

4.1.1. Gate Stack Leakage. The gate current leakage densities have been measured for samples SN1-2-3, SC and WSP samples, as shown in Figure 7.

The WSP samples show high and widespread leakage values as compared to SN1 and SC samples.

In Figure 8, the variation of the current density (J_g) as a function of the gate bias voltage for sample SN_{1-4} graph for different thicknesses of HfO_2 and gate bias is shown.

Gate stack leakage behaviour is observed and plotted for samples SN1–3 relative to a standard non-nitrided sample. To compare the results for different surface treatments, the gate leakage current densities at $V_g = -2$ V are plotted as a function of the EOT values (Figure 9). This plot shows the behaviour of the SC samples and HfO_2/Si which is almost identical in line with the C-V hysteresis.

For the nitrided samples, the SN1 sample seemingly possesses the most appropriate leakage/EOT trade-off ($J_g = 0.84$ A/cm^2 at $V_g = -2$ V for EOT = 0.7 nm). For the gate stacks with 1 nm EOT, the leakage current density of HfO_2 on Ge is 40–50 times smaller than for HfO_2 on Si. These attributes demonstrate that Ge/GeON/HfO_2 is a favourable candidate for the scaling regime.

4.1.2. Characterization of the Ge Material and the Interface Traps. With the help of observations of the C-V curve, we came to know the gate stack interface and Ge material traps.

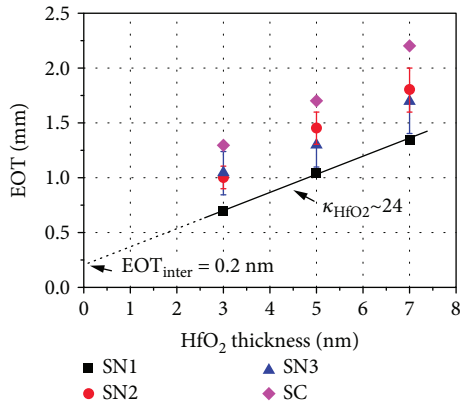

Figure 5: Equivalent oxide thickness for sample SN1–4 after quantum mechanical correction of the gate stack on Ge vs. the physical thickness of the deposited HfO_2 [5].

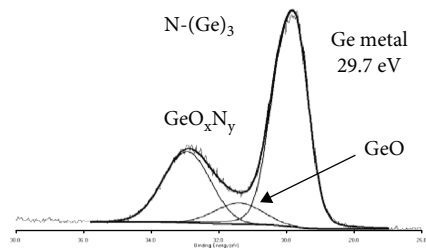

Figure 6: Ge XPS spectra for sample SN1 [5].

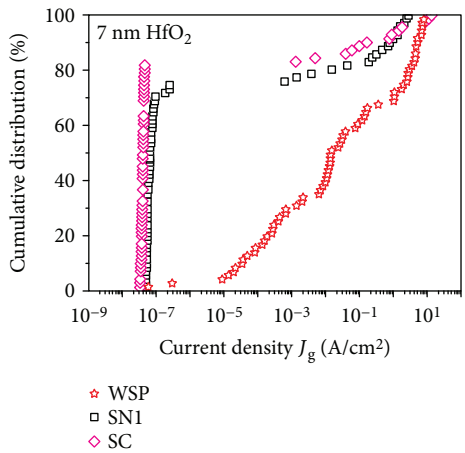

Figure 7: Cumulative distribution of gate leakage current density vs. current density for WSP, SN1, and SC [5].

Frequency scan was done for testing the device design. The frequency range from 1 kHz up to 900 kHz was employed for the C-V curve of the SN2 sample along with 7 nm thickness of dielectric HfO_2.

In order to extract the parameters, the C-V curve plays a very vital role, so to account for the carrier quantification in germanium, C-V simulation is performed. After the analysis, it became clear that frequency plays a very important role in ascertain capacitance.

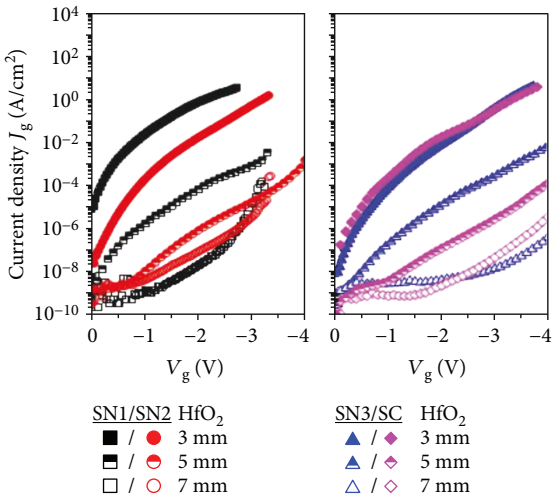

Figure 8: Current density vs. gate bias (V_g) [5].

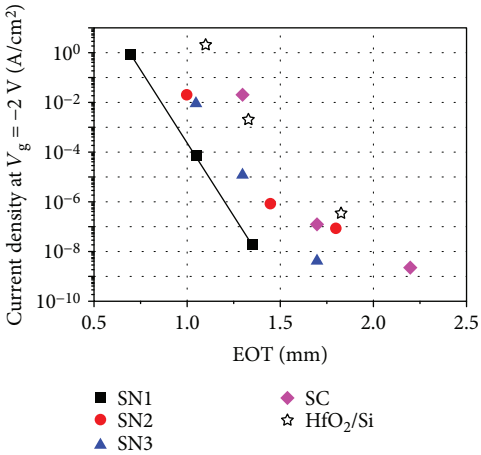

Figure 9: Leakage current densities vs. EOT for SN1–4 and reference HfO$_2$/Si [5].

It is deduced from the results of simulation that lower frequencies tend to lead to high capacitance whereas high frequency tends to lead to lead to low capacitance of the gate stack. The frequency is considered high when it is of the order of 400 kHz. The change in the reversal regime between Si and Ge is essentially credited to the lesser lifetime of smaller carriers in Ge which hinders the generation recombination procedures in this material. Due to the high density of defaults in the Ge film and higher carrier density (10^{13} cm^{-3}), the response time is lower (Figure 10).

4.1.3. Method of Extracting/Determining the Dit. The interface state density Dit over the band gap was extracted by modelling the experimental C-V curve at 400 kHz (solid line) for a sample of GeON with 7 nm thick HfO$_2$ in Figure 11.

In the lower portion of the band gap, the mean density of Dit is about $6 * 10^{12}$ cm^2 (near EV). In the vicinity of E, the Dit level is lower. However, the extraction method used now is comparatively imprecise to estimate Dit. On

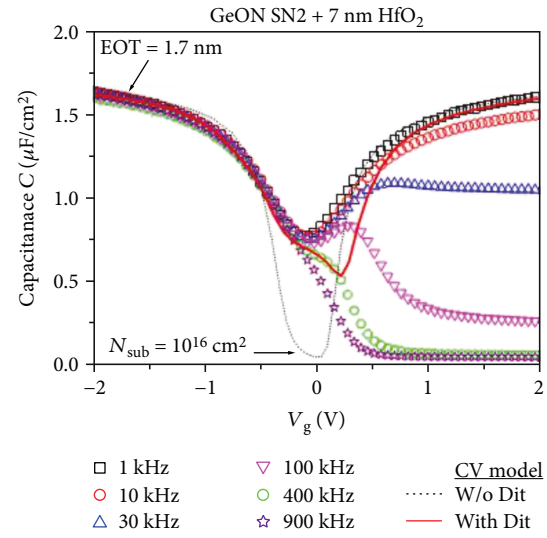

Figure 10: C-V curve for SN2 at the 1 kHz–900 kHz frequency range [5].

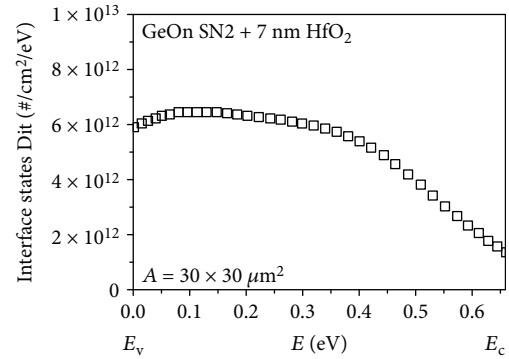

Figure 11: Interface state density vs. E for sample SN2 at 400 kHz and 7 nm HfO$_2$ [5].

SOI wafer, the SISCAP device was fabricated using 0.13 μm technology.

(1) C-V Hysteresis for SISCAP. The simulated and measured CV curves are compared for the SISCAP structure. The measured and simulated values are almost the same. A benefit of the SISCAP device is that it can be functioned in accumulation which delivers high charge densities on either side of the gate oxide. With this high charge density region centred within the optical mode, a large perturbation overlap integral [4] is achieved resulting in an efficient modulator that has a $V_\pi L_\pi < 2\,\text{V} \cdot \text{mm}^{-1}$ at a wavelength of 1310 nm (Figure 12).

4.1.4. Comparison of SiGe BiCMOS and RF CMOS Fabrication Technologies. A novel BiCMOS design variant incorporates a novel structure of the common source MOS and HBT structures having inherent properties of large slew rate of the HBT and low input resistance of the gate resulting in a faster switching speed than that of either MOS and HBT

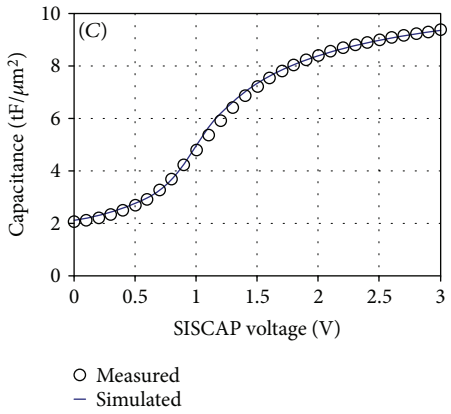

Figure 12: C-V curve for SISCAP [10].

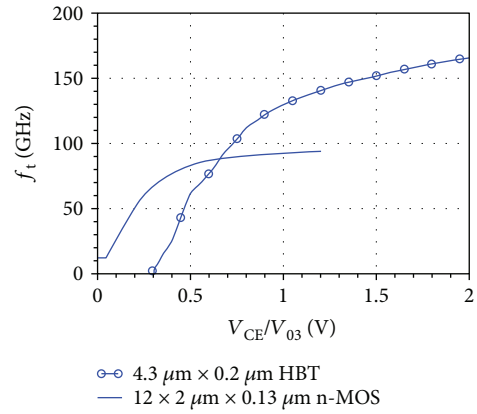

Figure 13: Ratio of collector to drain voltage with frequency curve [8]. Drain/collector voltage dependence of f_T (frequency) in 130 nm n-MOSFET and SiGe HBT.

devices as in Figure 13. Owing to the features of low threshold voltage for MOSFET and higher f_T key features of RF, CMOS fabrication technology has many advantages over SiGe, since BiCMOS has higher values of f_T and f_{MAX}. Due to lesser sensitivity to parasitic capacitance, SiGe BiCMOS has an advantage over the RF CMOS. High-temperature problems have been addressed in RF CMOS technology.

4.1.5. Comparison of Si CMOS, SiGe BiCMOS, and InP HBT Technologies. In Figure 13, the curve representing may be added to make sense. The comparison of HBT and 3D n-MOS device is presented. It can be seen that HBT devices have a higher drain-to-source-voltage ratio and have a higher slope as compared to n-MOS devices after 0.3 volts.

In Figure 14, a comparison is drawn for an inductor with a value of 150 pH for InP (indium phosphide) and Si substrate. At 50 GHz, the value of the Q factor is 15 for both InP and Si samples. For silicon implementation, a 75% smaller footprint is resulted; as for InP and Si, the width of the stripe is 2 mm.

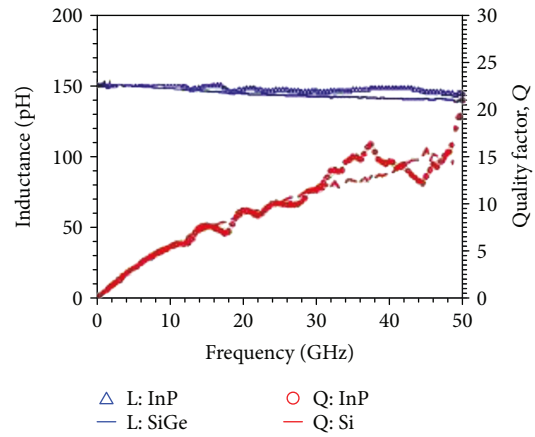

Figure 14: Inductance, quality factor, and frequency curve [8].

5. Results and Findings

This review study has several key and important results and findings to offer to the research literature. The NH_3 surface preparation on the high K metal gate structure has a direct impact on the electrical performance of the device. It is demonstrated that a surface anneal step for the special gate stack structure comprising of NH_3/sub 3/ambient HfO_x/sub 2 post-dielectric deposition results in significant improvements in both the equivalent oxide thickness (EOT) and the gate leakage current. It is also shown that it is possible to achieve Ge/GeON/HfO/sub 2//TiN gate stacks with an EOT of 0.7 nm with a leakage current of 0.84 A/cm/sup 2/at −2 V gate bias. The device and circuit performance for broadband and tuned millimetre-wave applications is also studied. Circuit implementations for CMOS, SiGe-HBT, SiGe BiCMOS, and InP-HBT 30–80 Gb/s high-speed circuit in the production of 130 nm SiGe BiCMOS and InP HBT technologies are compared and analysed. We have presented an efficient MOS capacitor-based silicon modulator. A special MZI configuration exhibits a 9 dB extinction ratio at a data rate of 28 Gbps at a 1 V output of a low-power CMOS inverter driver IC. This paper also presents an overview of high-K Si MOSFET, SiGE, HBT, and InP HBT technologies. The EOT of the interfacial layer (SiO_2) vs. thickness is also presented.

6. Conclusion

This paper encompasses the review of two key studies. In the first half of the study, the characterization of special CMOS-based device structure ($Ge/HfO_2/TiN$) capacitors on epitaxial GOS wafers is undertaken. The impact analysis of Ge surface preparation on dielectric deposition is analysed on the electrical characteristics. It was found that NH_3 treatment causes improvement in the EOT and the gate leakage current.

Further, the prime focus is to study the high K dielectric material. The contrast of the high k dielectric with the low K dielectric is also studied. The need for the use of a high k

dielectric is also justified within the paper. Five different samples were surface prepared with germanium on top of silicon. A thorough analysis on germanium on silicon samples is made such as C-V analysis, interface state density, EOT vs thickness of HfO_2, XPS, current density, inductance , and quality factor vs frequency in order to review all the possible parameters to examine the device. The comparison among the fabrication technologies such as SiGe, BiCMOS, and RF CMOS is also drawn.

The purpose of the study is to rigorously and holistically compare and contrast the various implementations of CMOS technology for frequency response and consequently for faster miniature electronic circuits for applications in communication systems. The aim is to set the direction of study among various technologies such as SiGe and InP HBTs to suggest to scientists and design engineers to choose the most appropriate technology for future implementation. Moreover, a CMOS-based device, namely, MOSCAP employing a high K dielectric (HfO) and metal gate (TiN), is characterised for leakage current and EOT. Moreover, germanium incorporation results in better transport properties, thus paving the way for following the ITRS roadmap.

Conflicts of Interest

No conflict of interest is declared from authors.

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