Research Article

Comprehensive Study of Kinetics of Processes Competing during PECVD Ultrathin Silicon Layer High-Temperature Annealing

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Received 2 July 2019; Revised 9 October 2019; Accepted 20 November 2019; Published 3 December 2019

Guest Editor: Francesca A. Scaramuzzo

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Application of low-temperature PECVD is a very tempting option for formation of ultrathin silicon layers for nanoelectronic and nanophotonic applications, as followed by annealing of this layer, regardless if executed as individual process performed in controlled ambient or during following high-temperature processes, allows for phase and content changes in the silicon layer. Understanding complex changes that can take place during such process, which depend on its temperature, conditions (e.g., oxygen availability), and timeframe, is a fundamental requirement for conscious application of such technology. It is worth realizing that nanodevices with their unprecedented variety of structures and devices require many different fabrication technologies. Hence, depending on the application in mind, different results of ultrathin silicon layer annealing may appear advantageous. During high-temperature processing (e.g., annealing) of PECVD ultrathin silicon layer, three competing effects have to be taken into account. These are amorphous silicon recrystallization and oxidation of amorphous and crystalline (as-deposited or just recrystallized from as-deposited amorphous phase) silicon (both of which by nature exhibit different kinetics). So far, most of attention has been paid to silicon recrystallization, which was justified by the fact that under experimental conditions studied (silicon multilayers) oxidation was certainly of less importance. In certain applications, the required device structure consists of single (and not multiple) ultrathin silicon layer, and thus, oxidation effects certainly have to be included into considerations. Understanding dynamics and very complex relations between these individual effects is thus mandatory for using consciously this technique and achieving needed properties of the layer. It has to be stated clearly that although the achieved results, presented in this study, refer to the silicon layers fabricated under certain conditions (particular type of PECVD reactor and process parameters), they can, however, be easily extrapolated for similar cases too. The presented below results are, to our knowledge, the first successful attempt to address these issues.

1. Introduction

Silicon nanocrystals have been investigated very intensively for more than two decades. Many potential applications have been considered and many methods of their formation studied. For very broad (216 references) and recent review of these issues, see [1].

In many applications, we find double oxide barrier structure (ultrathin layer stack—oxide/silicon/oxide). Depending on application, different requirements on the physical structure and properties of silicon ultrathin layer in this stack can be requested. The most intriguing case is

the possibility of obtaining silicon nanocrystals (nanodots) in the dielectric (oxide) matrix, which can be achieved by very carefully achieved combination of recrystallization and oxidation processes. As both of these processes require high temperature, they can take place at the same time, simultaneously, providing appropriate conditions are satisfied. It is worth realizing that the main difference between the conditions needed for them is the availability of oxygen, which is indispensable for the oxidation process, while not needed for recrystallization.

In reality, oxygen-free conditions can only be obtained in high-temperature annealing process in case of complete lack

FIGURE 1: Schema of the (a) used process flow and the (b) fabricated structure.

of oxygen source in the reactor, i.e., no oxygen in supplied gas nor oxygen is released (e.g., outdiffused) from any layer that the annealed structure consists of. While the former condition is relatively easy to provide, the latter one is not (as it will be shown in this paper).

So far, many studies on amorphous silicon recrystallization ignored silicon oxidation and its potential effect on high-temperature recrystallization process (e.g., [2–4]). This approach was justified in some of these works by the fact that in the multilayer structure (some tens of ultrathin silicon layers located in between silicon oxide layers) with high-temperature stoichiometric thermal oxide used in these investigations, the probability of releasing oxygen from the oxide layers was very low. At the same time, most of the silicon layers in the stack were far beyond diffusion length of oxygen from ambient gas during high-temperature annealing. Hence, measured by photoluminescence, Raman or XRD signals averaged across the whole stack could not identify changes in SiO_2 content.

In the studied case of single ultrathin silicon layer behavior, where quantitative data were needed, spectroscopic ellipsometry was used for the investigation of changes in phase and thickness of ultrathin PECVD silicon layer.

This detailed study is believed to provide grounds for practical use of annealing and/or oxidation of PECVD ultrathin silicon layers to fabricate different nanoelectronic and nanophotonic devices.

2. Experimental

2.1. Sample Preparation and Technology. In the experiments, Si (100) 5–9 Ωcm boron-doped wafers were used as substrates. In order to achieve atomically flat silicon surface after standard RCA-based (HF-last) cleaning, the wafers underwent so-called “sacrificial oxidation” followed by selective oxide etch (as shown in Figure 1). This allowed to achieve atomic flat silicon and defect-free monocrystalline surface (confirmed previously by TEM observations).

Basing on previous results presented in [5], which have proved that the recrystallization process is practically not influenced by direct contact of PECVD layer with monocrystalline silicon substrate, and on a spectroscopic ellipsometry study presented in [6] proving that an ultrathin silicon PECVD layer can be successfully analyzed on Si substrate,

in this work, the ultrathin silicon was PECVD deposited directly onto the monocrystalline silicon wafer.

For the PECVD processing, the Oxford Plasma Technology 80+ system was used. The silicon PECVD process optimized for low deposition rates as reported previously in [5, 7, 8] has been used. Deposition of silicon PECVD layers was performed using SiH_4 (2%): He diluted in 5 N purity argon (150 sccm and 50 sccm, respectively); the deposition temperature is 350°C and the R.F. power is 25 W.

Within this study, two types of samples were fabricated. They differed by thickness of PECVD Si layer only (the same deposition parameters were used except for deposition time) and will be referred to hereafter as “thin” and “thick” (as-deposited layer thicknesses were 53 Å and 84 Å, respectively). These two types of samples with differing thicknesses of Si PECVD layer appeared to be indispensable, as will become clear in Section 3 of this paper, for analysis of reasons of oxide growth saturation during high-temperature annealing.

High-temperature annealing was performed in typical semiconductor high-temperature furnace in quartz tube. Argon of 5 N (99.999%) purity was used for this purpose. In order to have fair comparison of results of annealing, the wafers were divided into quarters for annealing. The annealing conditions and times were chosen based on the previous experiments and were set to 700°C , 800°C , 900°C , and 1000°C and 1, 2, 3, and 5 minutes, respectively.

2.2. Characterization Method of the Obtained Structures and Results of Annealing. The results of structure manufacturing were then examined by spectroscopic ellipsometry study. This method was already proved (e.g., in [5–11]) to be very sensitive and reliable, while fast and nondestructive.

For spectroscopic ellipsometric studies UVISEL-NIR by Jobin-Yvon and supplied with this equipment modelling software has been used. It allows performing ellipsometric measurements within wide range of wavelengths, i.e., from 190 nm to 880 nm, if necessary under different angles of beam incidence. As a rule, measurements and then fitting were performed in the whole allowed by the tool wavelength spectrum. The enclosed to this tool materials’ data base and several optical models to choose from allow for nondestructive and very sophisticated characterization of

FIGURE 2: Schemas of optical models used for analysis of spectroscopic ellipsometry data: (a) for the as-deposited single PECVD Si layer parameter determination and (b) for evaluation of structure properties after annealing process. In order to differentiate the two silicon oxides, the oxide phase in the silicon layer will be referred to as “SiO₂ in PECVD Si,” while continuous oxide layer as “SiO₂ on top”.

TABLE 1: Thickness and phase composition of as-deposited “thin” and “thick” PECVD layers.

	“Thin” layer		“Thick” layer	
	Composition (%)	Phase thickness (Å)	Composition (%)	Phase thickness (Å)
a-Si	49	26	68	57
c-Si	30	16	15	13
SiO ₂	21	11	17	14
Total for PECVD silicon layer	100	53	100	84

single and multiple layers. When used carefully, it allows not only to determine individual layer thickness (even in the multiple layer stack) but also (with some limitations) to study phase compositions of the layers. For more information on these models, see [12]. Formally, content of up to three phases or compounds within a single layer is possible to be evaluated from this optical model. These features have been fully explored in this study. The validity of this approach has been already proved and discussed in more details in [6].

In order to discuss and compare the behavior of each of individual phases in PECVD silicon layer during the studied high-temperature processes, the concept of “phase layer thickness” will be used hereafter. This concept has already been introduced and discussed in our previous works (e.g., in [5, 6, 8]). The multiphase PECVD silicon layer is described in optical models used in this study by its physical thickness and its composition expressed in percentage of the layer. The used hereafter terms “phase thickness” (a-Si phase thickness, c-Si phase thickness, or SiO₂ phase thickness) are, thus, obtained by multiplying overall physical thickness of the layer by composition percentage of the particular phase. As a result of this, the overall PECVD Si layer thickness (as evaluated from ellipsometric measurements using the assumed optical model) is equal to the sum of these “phase layer thicknesses.” The advantage of this approach is that using these parameters one can independently follow possible changes in both, in physical layer thickness and in its composition.

It should be stressed, however, that phase thickness concept neither assumes nor provides information on location of particular phases constituting the layer (as has already been discussed in [8]).

Each of the produced samples has been measured in at least 3 points in order to avoid that some local behavior artefact may be misinterpreted as a characteristic feature of the tested sample. Providing the difference in results of analysis performed in each of all the measured points was acceptably small, the average values were then calculated and used for the analysis and discussion. In few occasions only, where the data scatter on the sample was considered unacceptably high, the statistics of the measurements was improved by measuring at more individual locations.

Such an approach is justified by the fact that spectroscopic ellipsometer spot size is by far greater than that of the expected nanocrystals. This means that this measurement method is, by nature, providing information on average character over the spot area in the sample.

3. Results and Discussion

3.1. Characterization of As-Deposited PECVD Si Layers. The ellipsometric analysis of the as-deposited PECVD Si films was performed using an optical model shown schematically in Figure 2(a). In this model, three phases are expected in this single layer, namely, amorphous silicon phase (a-Si), nanocrystalline silicon phase (c-Si), and silicon oxide phase (SiO₂). It allows to evaluate the initial content of the layer and hence allows to follow changes in phase composition of this layer resulting from the studied annealing processes.

The obtained composition of the as-deposited “thin” and “thick” PECVD layers is shown in Table 1.

It is interesting to realize that although the main contribution to the as-deposited PECVD layer thickness (volume) comes (as expected) from a-Si, there already exist also nanocrystalline silicon (c-Si) and silicon oxide (SiO₂) phases. The

difference in thickness between the “thin” and “thick” layers is primarily due to the difference in amorphous phase content, while c-Si and SiO₂ phases change only a little. Another intriguing fact is that c-Si seems to decrease with PECVD time (is thinner for thick layer). This behavior is in agreement with observations obtained for high-temperature annealing which will be discussed below. While the presence of both phases of silicon is obvious, the origin of the SiO₂ phase is, at the first glance, not.

Although no oxygen is used in PECVD of silicon layer, one has to remember that humidity is very difficult to pump down in vacuum reactor chambers, so (unless load-lock system is used) its presence in the reaction chamber has to be taken into account. On the other hand, bare silicon surface is exceptionally reactive when exposed to ambient atmosphere and natural oxide grows on such a surface in a matter of minutes. Hence, it is reasonable to attribute the detected in as-deposited layer SiO₂ phase to thin natural oxide spontaneously grown on silicon wafer surface after wafer cleaning procedure prior to PECVD process and some SiO₂ particles resulting from reaction of deposited Si with oxygen leftovers present in the reaction chamber during PECVD.

It should be stressed that fittings of the optical model presented in Figure 2(a) to experimentally obtained spectroscopic ellipsometry data were very good (RMS ≤ 0.1 (RMS (Root Mean Square) deviation error in this case is representing the accuracy of fitting theoretical optical model to the real results of ellipsometric measurements, hence confidence level to evaluate this method parameter of the optical model (whether it is thickness, thickness and/or optical properties, or thickness and/or composition).) for the whole measured spectrum), thus should be considered as reliable.

During high-temperature annealing, especially in high purity gases (in our case Ar 5N better than 99.999% was used), it is expected that (depending on temperature and time) only annealing process leading to reduction of defect density in the as-deposited silicon layer (PECVD Si) or this layer recrystallization, resulting in the formation of silicon nanocrystals, takes place. In extreme situation, there potentially exists a possibility of complete recrystallization of as-deposited silicon layer, i.e., formation of a single crystal (monocrystalline) layer across the wafer. The situation differs significantly if there is oxygen available during the annealing process and whether its source is limited or unlimited. Under such conditions, we can expect competing (with annealing) process of oxidation. Consequently, depending on the amount of oxygen available for oxidation, we can expect either continuous, unlimited growth of silicon oxide phase or its saturation due to consumption of all available oxygen in the system.

For this reason, in the studies on the results of annealing experiments (similarly as in [5]), a slightly different optical model of the structure for spectroscopic ellipsometry data analysis was used. It differs by additional oxide layer placed on top of the silicon layer (defined exactly as for as-deposited silicon PECVD layer) and is shown schematically in Figure 2(b). In order to distinguish in the discussion below the oxides, the additional one will be hereafter referred to as

FIGURE 3: Schema of effects competing during high-temperature processes for PECVD silicon ultrathin layer containing structures.

“SiO₂ on top,” while the one present in the silicon layer as “SiO₂ in PECVD Si.”

3.2. Silicon Oxidation. As this has been already mentioned above, there already exists SiO₂ phase in the as-deposited silicon layer. Further changes in oxide phase content strongly depend on the additional availability of oxidant species during high-temperature annealing processes. Few more potential sources of oxygen that can fuel silicon oxidation can be named. Summarizing, we could expect them to be as follows:

1. Natural silicon oxide layer located between the silicon monocrystalline substrate and PECVD Si
2. Water vapor adsorbed on sample surfaces before their loading into a high-temperature furnace
3. Water vapor adsorbed on reactor walls during its loading/unloading and, thus, present during PECVD Si (this can be prevented by using loadlock system in PECVD reactor)
4. Diffusion through the wall of quartz tube in the high-temperature furnace used for annealing (which can, potentially, be prevented fully only by double wall quartz tube system and is strongly quartz tube temperature history dependent)

Under these circumstances during high-temperature annealing, along with the processes mentioned above (defect annealing, recrystallization), we also have to take into account the process of oxidation of amorphous silicon a-Si (represented in Figure 3 as “oxidation#1”). We also have to consider another oxidation path, which consumes nanocrystalline silicon c-Si (represented in Figure 3 as “oxidation#2”). It should be underlined that these two processes can potentially have different kinetics, due to difference in crystalline structure of silicon consumed for thermal oxidation. It also has to be remembered that kinetics of both processes is highly dependent on availability of free silicon (either a-Si or c-Si for “oxidation#1” and “oxidation#2,” respectively) and of free oxygen. The specificity of the structures under consideration is that providing all silicon from the PECVD Si layer is already consumed, oxidation can continue further

by consumption of silicon from monocrystalline substrate. In order to be able to take into account this effect, two series of samples were fabricated, i.e., with “thin” PECVD Si and “thick” PECVD Si.

The complexity of results of high-temperature annealing of PECVD Si layer can be schematically presented as shown in Figure 3.

Consequently, in order to understand the experimentally obtained results of annealing of structure of interest, we have to compare the kinetics of all three processes potentially involved. It should be realized that in many potential applications the ultimate goal of processing would be formation of silicon nanocrystal (nanodot) matrix suspended within the oxide volume. Depending on their relative rate, this final aim may or may not be possible to achieve by annealing or annealing/oxidation process. Hence, even more important is careful analysis of these competing processes.

The following part of this paper describes the experiments and analysis of the results aimed at fulfilling this requirement.

3.3. Silicon Recrystallization. Recrystallization of amorphous silicon thin layers in high-temperature treatments formed by various methods has already been reported before (e.g., [1–5, 12–18]).

In the preceding study experiments, we have experimentally verified a wide range of annealing temperatures and times, i.e., temperatures from 350°C up to 1100°C and times from few minutes to a quarter of an hour. The obtained results have already been published in [8]. Basing on the results in this study, values of these parameters have been narrowed to temperature range between 700°C and 1000°C and limited annealing time to 5 minutes only for current experiments. In order to remove from the studied system difficult to control source of oxygen while not affecting recrystallization process (as it was already determined in [5]), in the current study, no SiO₂ layers were fabricated below and top of the PECVD silicon layer.

Using two types of samples, “thin” and “thick,” was also advantageous from the perspective of study of recrystallization effects. They allowed us to verify if recrystallization behavior is dependent (within examined range) on the initial thickness and volume of amorphous silicon layer.

3.4. Oxidation and Recrystallization Kinetics: Temperature Dependencies. The obtained results are presented in Figures 4 and 5. Comparing the results obtained for “thin” and “thick” PECVD Si film annealing, one can realize that although there are some differences between them, some universal characteristic features can also be noticed. In fact, we can realize that the “thick” case copies the behavior of all the annealed layers under study of the “thin” one, but in a different timeframe. It is interesting to realize that some things seem to happen much slower for the “thin” than for the “thick” case. This has already been reported in numerous papers in respect to crystallization process and attributed to difference in stress in the layers (e.g., [3, 13, 14]). In this study, this refers not only to the qualitative behavior of silicon phases but also to oxides. In both cases, we can see that

the lowest annealing temperature (700°C) is too low to get recrystallization effects within the PECVD Si film (see Figures 4(a) and 5(a)). This is in agreement with the results of studies presented before for various methods of layer deposition (e.g., [13]). On the contrary, during the first minute, the originally observed crystalline phase of this layer (c-Si) disappears (completely for “thick” and almost completely for “thin” case). It is intriguing to realize that this trend is similar to the one observed for low-temperature annealing (350°C) that takes place *in situ* during PECVD itself. As already reported above, as-deposited “thick” silicon layers contained less (percentage-wise) c-Si phase content than the “thin” one (deposited shorter, hence exposed shorter to raised deposition temperature).

Interestingly, the silicon oxide phase within the PECVD Si (“SiO₂ in PECVD Si”) layer remains almost constant during annealing, while oxide on the top of the structure grows. The oxide growth is slow and tends to saturate for annealing times longer than 3 minutes. This can be explained either by typical for this temperature range behavior of kinetics of silicon oxidation (see [15]) or exhausted already (at this moment) source of free oxygen needed to continue the oxidation process.

For 800°C, we still can see the initial period (first minute) during which c-Si disappears (see Figures 4(b) and 5(b)). In this case, however, from this moment noticeable (for “thin” case) and almost complete (for “thick” case) recrystallization of silicon phase occurs. The kinetics of this process differs significantly depending on the original thickness of the silicon layer. For the “thick” one, recrystallization rate is very high, much higher than that for the “thin.” Within a minute (between 1 and 2 minutes of annealing), it reaches its final state (for which more than 90% of free silicon is nanocrystalline). This is not the case for the “thin” silicon layer, for which recrystallization is relatively slow and it takes 5 minutes to achieve approximately 75% of c-Si phase content in free silicon. This observation can be considered as supporting report of Zacharias and Streitenberger [19] in which they have shown that crystallization temperature is strongly dependent on initial a-Si layer thickness and it abruptly increases with decreasing silicon layer thickness. It should be noticed, however, that according to [19] the crystallization temperatures for Si layer of similar thickness to the ones in our study, i.e., approximately 5 nm and 8 nm (corresponding to “thin” and “thick” cases), are approximately 1050°C and 1000°C, respectively, thus are significantly higher than those observed in our study.

Considering the influence of internal stress in a-Si layers on recrystallization behavior (among others, temperature), which has been shown and discussed by Zacharias and Streitenberger in [19], one could draw then indirect conclusion that PECVD a-Si layers fabricated in our study exhibit far less internal stress than those studied by Zacharias et al. It should be kept in mind, however, that while in [19] a-Si thermal recrystallization was performed using multilayer stacks in which each of the a-Si layers was located in between two SiO₂ (plasma oxidized) layers, in our study, a-Si was deposited directly on monocrystalline silicon substrate with potentially only natural oxide at its both interfaces. Also, the

FIGURE 4: Individual layer and phase reaction to annealing in pure argon at (a) 700°C, (b) 800°C, (c) 900°C, and (d) 1000°C of “thin” PECVD Si layer. PECVD Si layer consists of a-Si, c-Si, and SiO₂ in PECVD Si phases. SiO₂ on top is determined as a separate layer.

method of a-Si layer formation was different in [19], as magnetron sputtering (presumably with no external heating during deposition) was used for this purpose in this work.

As can be seen in Figures 4(b) and 5(b), in this temperature, oxide formation is also slow and in both cases oxide thickness saturation can be observed. In fact, oxide thicknesses are very similar for both groups of samples.

The recrystallization process behaves differently for 900°C. In both cases (“thin” and “thick,” see Figures 4(c) and 5(c), respectively), we do not observe any more amorphization of the initial c-Si phase (reported above for the beginning of annealing at lower temperatures). Instead, we can see that in this temperature both “thick” and “thin” silicon layers get practically completely recrystallized during this first minute of annealing. As regards oxide formation, in this temper-

ature, oxide thickness is similar in both cases. This is not surprising as although recrystallized silicon phase is decreasing during the annealing after the first minute, even for “thin” silicon layer some c-Si are left and can potentially undergo oxidation providing there is still some free oxygen available in the system. The oxide growth is slightly higher than for 800°C, which is consistent with oxidation process kinetics temperature dependence. More detailed discussion on the oxidation issues are to be found below.

In 1000°C, alike in 900°C, recrystallization of amorphous silicon for both “thick” and “thin” cases is completed within the first minute of annealing (see Figures 4(d) and 5(d)). We can, however, observe very high consumption rate of silicon (after the first minute) by oxidation, which at 1000°C is very fast indeed. In fact, for the “thin” case, free silicon is

FIGURE 5: Individual layer and phase reaction to annealing in pure argon at (a) 700°C, (b) 800°C, (c) 900°C, and (d) 1000°C of “thick” PECVD Si layer. PECVD Si layer consists of a-Si, c-Si, and SiO₂ in PECVD Si phases. SiO₂ on top is determined as a separate layer.

consumed almost completely during the first 2 minutes, while for the “thick” layer case this takes only one minute longer (at 3 minutes).

It is interesting to realize that for all temperatures lower or equal to 900°C, the oxide growth is attributed by optical model to the continuous “SiO₂ on top” layer, while “SiO₂ in PECVD Si” holds almost completely stable within the whole range of examined annealing times. This is no more true for 1000°C for which (in both cases) “SiO₂ on top” is at some moment of annealing “replaced” by “SiO₂ in PECVD Si.” For the “thin” case, this happens in between the first and second minutes of annealing, while for the “thick” case sometime between the third and fifth minutes of annealing.

In order to try to understand better the effects leading to the results described above, one should draw attention to few more facts.

For more in-depth analysis of oxidation process, a different representation of the obtained experimental data is advantageous. For this purpose, it is better to consider total oxide thickness (“SiO₂ on top” plus “SiO₂ in PECVD Si”) and total free silicon (a-Si plus c-Si) in the studied systems. The obtained time dependencies for all studied temperatures and both “thin” and “thick” cases are shown in Figure 6.

From Figure 6(a), it becomes clear that for 800°C and below, for both “thin” and “thick” cases free silicon behaves similarly. We observe saturation of its consumption by oxidation and it remains even for the longest annealing times used in the experiment. The situation for 900°C, however, depends on the initial thickness of the annealed layer. For the “thin” case, free silicon disappears almost completely, while for the “thick” case a lot of it remains still available in the layer. We can see that the rate of silicon consumption

FIGURE 6: Changes during high-temperature annealing for two types of samples with “thin” PECVD Si layer (dashed lined and empty symbols) and with “thick” PECVD Si layer (full lines and symbols) of (a) total free silicon (a-Si+c-Si) and (b) total oxide thickness (“SiO₂ on top”+“SiO₂ within PECVD Si”).

in both cases seems almost independent on initial silicon thickness. For annealing at 1000°C, the rate of silicon consumption by oxidation differs at first glance dramatically. Careful look allows, however, to realize that the kinetics of free silicon consumption at the beginning stages of annealing is similar (compare the “thin” case up to 1 min and the “thick” case up to 2 minutes), while the main difference is that it takes at least one more minute to consume free silicon in the “thick” PECVD Si layer. In fact, practically all the free silicon is consumed within 2 minutes of annealing for “thin” and 3 minutes for “thick” cases at this temperature. If oxidation kinetics would be controlled by silicon availability, the oxide growth should completely stop after 2 min for “thin” and after 3 min for “thick” PECVD Si layer annealing. In Figure 6(b), we can see that this is not the case. Oxide growth does take place in this time regime and its rates are very similar (see also Figure 7). This leads clearly to a conclusion that oxidation kinetics is controlled by oxygen and not by silicon availability. Once free silicon originating from PECVD Si layer is not available any more for the oxidation process, silicon from the silicon substrate layer is consumed. This effect cannot be recognized in by ellipsometric measurements and available optical models.

Looking at the presented kinetics of oxide formation in Figure 6(b), one can realize that the starting point for “thin” and “thick” layers differs by few Angstroms. Taking this into account, results in oxidation rate (see Figure 7) for annealing temperatures up to 900°C of both “thick” and “thin” cases are being practically the same (with the exception of one point at 3 minutes for “thick” one, which will be discussed in more details below). Interesting effect occurs for 1000°C, where at the beginning of annealing oxidation rates differ significantly, with gradual slowdown in time for “thick” layers and abrupt for “thin” ones. Still, both oxidation rates meet at the end of

FIGURE 7: Oxidation rates (calculated from data shown in Figure 6(b), attributed to the center of each of time slots) during high-temperature annealing for the two types of samples, with “thick” and “thin” PECVD Si layers (full symbols/solid lines and open symbols/dashed lines, respectively).

the examined annealing time range, i.e., between 3 and 5 minutes. This can potentially be a consequence of the observation referred already above (see also Figure 6(a)) that at 1000°C free silicon is consumed in the “thin” layer already by the end of the second minute of annealing, while for the “thick” layer it takes one more minute (no free silicon is practically available after the third minute of annealing). Hence,

FIGURE 8: Total oxide thickness (“SiO₂ on top”+“SiO₂ within PECVD Si”) changes during high-temperature annealing for the two types of samples: with “thin” PECVD Si layer (full lines and open symbols) and for standard RTO (data from [20]) (full symbols).

at this temperature, we can divide the examined annealing time range into three stages:

- (1) Oxidation consumes only free silicon from the PECVD Si layer (this takes place during the first minute of annealing for “thin” layers and 2 minutes for “thick” ones)
- (2) Transition period, during which free silicon from the PECVD Si film does not provide enough silicon for oxidation (this takes place during the next 1-2 minutes range for “thin” and 2-3 minutes range for “thick” (see Figure 6(a)))
- (3) Oxidation can take place only by consuming monocrystalline silicon substrate (takes place from the 2nd minute for “thin” and the 3rd minute onwards for “thick” layers)

All the presented discussion on oxidation kinetics has not so far referred to the problem of limitation of availability of oxygen during the annealing process. In order to address this issue, it is suggested to compare experimentally observed oxide growth during annealing with kinetics of oxidation performed with unlimited supply of oxygen (Rapid Thermal Oxidation (RTO) [20]). The comparison for two temperatures, namely, 900°C and 1000°C, and the “thin” case is shown in Figure 8. It can be clearly seen that oxidation rates behave significantly different for both temperatures compared.

For 1000°C, oxide growth during the first two minutes is almost identical for rapid thermal oxidation (RTO) and oxidation during PECVD silicon layer annealing. Only afterwards, oxidation rate during RTO exceeds that for

annealing. Taking into consideration that for the “thin” case for annealing times longer than 2 minutes, oxidation takes place by consumption of monocrystalline silicon substrate (see discussion above), exactly as in the case for RTO, this difference can only be attributed to the limitation of oxygen in the reaction chamber of annealing furnace. In consequence, this observation fully supports the conclusion presented in this study that oxidation rate is controlled by the deficiency of free oxygen in the system. It has to be realized then that depending on the nature of oxygen source in the experimental system oxidation may continue or can ultimately stop. The moment it happens, as well as the degree of oxygen limitation (hence also oxidation rate) is strictly individual, as according to our discussion above, the potential sources of oxygen in the system can vary significantly between different procedures and equipment used in particular laboratories.

For 900°C, the situation is different. The overall oxide thickness (sum of “SiO₂ on top” and “SiO₂ in PECVD Si”) resulting from the annealing in this temperature is much higher than that achieved during RTO (see Figure 7). At first glance, this seems to be nonsense. How can the actual oxidation rate be higher than the thermal oxidation rate under standard conditions (i.e., with unlimited silicon and oxygen supply) at the same temperature? This effect can be explained by the following fact. Standard thermal oxidation takes place at the already formed oxide-silicon substrate interface due to oxygen supplied from the ambient atmosphere to this plane by means of numerous mechanisms (highly dependent on the current thickness of the oxide layer, see [21]). Thus, in typical process, we have a chemical reaction that takes place primarily at a certain plane. In our case, on the contrary to the typical situation, we have oxygen atoms not only in the ambient atmosphere but some of them are already incorporated in the PECVD Si layer volume. Hence, oxidation in the studied case does not take place at a single “reaction plane,” but in the whole volume of PECVD Si layer. This way, oxide growth higher than that for the typical process is possible and justified. This hypothesis can be also supported by an observation that as oxidation time increases and according to our mentioned above observations, availability of free oxygen becomes reduced, the difference between oxidation behavior of PECVD Si and RTO process becomes smaller and it seems reasonable to expect that will become negligible for longer annealing times.

It also has to be pointed out that for both “thick” and “thin” cases for 900°C, “SiO₂ in top” prevails “SiO₂ in PECVD Si,” while for annealing times longer than 2 minutes at 1000°C it is the other way round. One has to realize that these two types of oxides are not the same in at least two ways. While “SiO₂ on top” is assumed to be a continuous layer on top of the sample, “SiO₂ in PECVD Si” may not be. From the optical model point of view, it is one of the phases present in the layer on top of silicon substrate and covered by continuous “SiO₂ on top.” Once “SiO₂ in PECVD Si” prevails free silicon content (sum of the other two phases in this layer, i.e., a-Si+c-Si), it becomes reasonable to assume that the remaining silicon is located in this layer in one of the two forms shown schematically on Figure 9. Under these

FIGURE 9: Schematic view of two potential interpretations of complex composition in PECVD Si layer: (a) continuous crystalline silicon “sublayer” and (b) matrix of silicon nanocrystals, both within the oxidized PECVD Si layer.

circumstances, one can potentially have either very thin, continuous crystalline silicon layer (Figure 9(a)) or silicon nanocrystals surrounded by silicon oxide (Figure 9(b)). These two forms cannot be distinguished by means of ellipsometry due to averaging effect resulting from size of ellipsometric spot (of the order of hundred micrometers) compared to a size of silicon nanocrystals (of the order of nanometers). If we realize that for 1000°C both “thick” and “thin” cases exhibit only few Angstroms of c-Si phase left, then oxide matrix with some intrusions of silicon nanocrystals seems to be by far a more probable option. For 900°C, however, there is a significant difference between the “thin” and “thick” cases. The “thin” case reminds situation observed for 1000°C, with only few Angstroms of silicon remaining after the first minute of annealing. For the “thick” case, however, even for 5 minutes annealing, there remains most of the initial silicon phase thickness. This can be explained by considerable oxidation kinetics slow down for annealing times above 2 minutes observed in Figure 6(b) (or Figure 7). As a consequence, it seems justified to claim that in temperatures around 900°C, we can independently control recrystallization and oxidation process by means of annealing time. Choosing appropriate initial silicon PECVD layer thickness provides opportunity to control nanocrystal size under these conditions. Further optimization is needed to establish precise dependencies between these parameters. It is important to realize that due to stress dependency of crystallization behavior, any change in PECVD silicon deposition process which may change the internal stress in this layer will inevitably influence the temperature and time dependence of the optimum annealing conditions.

4. Summary

The comprehensive study presented above allowed to obtain important observations and draw from them numerous conclusions that are potentially of great interest for considerations on methods of fabrication of different types of structures and devices for electronic and photonic applications.

Within this study, it has been proved once again how valuable spectroscopic ellipsometry-based analysis can be for providing information on structure and phase composition of complex ultrathin layers and studies on their variability and changes during processing. Using consequently the same optical model along the annealing process analysis provided unique opportunity of straightforward following complex processes taking place during this high-temperature annealing.

The obtained results proved that the proposed dual path between free silicon and silicon oxide phase (path via recrystallization and then oxidation in parallel to direct oxidation

of amorphous phase of silicon) allows to represent, analyze, and explain complex events that take place during high-temperature annealing of primarily amorphous PECVD silicon layer.

Providing ultrapure neutral gas (e.g., 5 N purity) for high-temperature processing does not ensure oxygen-free ambient atmosphere during it. There exist numerous sources (limited and unlimited in time) that have to be taken into consideration when analyzing results of the high-temperature process, especially in nanoscale. This is particularly true for silicon due to exceptionally quick growth of natural oxide even at room temperature.

The oxygen present within the ultrathin layer can change significantly the behavior and kinetics of the events taking place during high-temperature processing. In this study, it has led, for example, to oxidation rates higher than that for standard oxidation (with unlimited supply of oxygen).

The discussed results in this paper proved very high dependence of both oxidation and recrystallization process on temperature. From the perspective of recrystallization process, 700°C is too low to observe this effect, while 1000°C is too high (recrystallized silicon is almost instantly consumed by oxidation).

The process of silicon recrystallization in lower temperatures studied (i.e., 700°C and 800°C) is preceded by the decomposition of silicon crystals regardless of the initial thickness, while for temperatures above (i.e., 900°C and 1000°C) amorphization process cannot be noticed. Nanocrystalline silicon phase replaces amorphous silicon very quickly (regardless of the initial deposited layer thickness) and its content decreases in time due to the oxidation process.

Recrystallization rate and its temperature dependence are also strongly affected by the method and formation conditions (deposition parameters) used for silicon layer fabrication, which can be explained by different internal stress in the layer.

Similar to recrystallization, for oxidation, lower temperatures (i.e., 700°C and 800°C) are not sufficient to consume free-silicon phase in the deposited layer. On the contrary, annealing at 1000°C leads very quickly to complete consumption of free-silicon phase in the layer.

From the perspective of potential applications, the most interesting are temperatures around 900°C, for which, depending on the initial silicon layer thickness, one can achieve either completely recrystallized silicon phase in the form of nanocrystals (alternatively atomic thin silicon layer) suspended within the oxide.

Oxidation process, after certain time, becomes controlled (limited) additionally by oxygen availability in the reactor

and in the deposited silicon layer. This makes it sensitive to the methods of silicon layer deposition and preprocessing (chemistries and their sequence).

Choosing appropriate initial thickness, annealing temperature, and time while controlling oxygen supply sources (also on the level of silicon substrate preprocessing and deposition method and its conditions) should allow achieving repetitive results of otherwise very difficult to obtain structures.

It has to be underlined that this requires individual optimization process, as the kinetics of nanocrystalline phase oxidation at some moment begins to depend on the used methods of silicon layer deposition and preprocessing steps.

It also seems justified to conclude that PECVD Si ultrathin layers manufactured for the purpose of this study exhibit much smaller internal strain than the ones fabricated by magnetron sputtering method. This, in turn, results in lower crystallization temperature favoring this process vs. oxidation and in consequence increasing the technological window for separation of recrystallization from oxidation in temperature and time domains.

Data Availability

The data are collected and archived at the Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, as a part of documentation of results achieved during two research projects, funded via National Grants by the National Science Centre-DEC-2011/03/B/ST702595 (UMO-2011/03/B/ST7/02595) and funded by the National Centre for Research and Development (NCBiR) under grant no. V4-Jap/3/2016 ("NaMSeN") in the course of "V4-Japan Advanced Materials Joint Call," as well as during diploma work of Kamil Ber.

Disclosure

This paper is developed from the conference abstract presented on the 2016 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

This work was partly funded via National Grants by the National Science Centre-DEC-2011/03/B/ST702595 (UMO-2011/03/B/ST7/02595) and partly by the National Centre for Research and Development (NCBiR) under grant no. V4-Jap/3/2016 ("NaMSeN") in the course of "V4-Japan Advanced Materials Joint Call." The authors acknowledge all the valuable feedbacks received at the conference.

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