

## Research Article

# Improved Carbon Nanotube Field Effect Transistor for Designing a Hearing Aid Filtering Application

**K. Mohana Sundaram** <sup>1</sup>, **P. Prakash**,<sup>2</sup> **D. Karthikeyan**,<sup>3</sup> and **Wubishet Degife Mammo** <sup>4</sup>

<sup>1</sup>Department of EEE, KPR Institute of Engineering and Technology, Coimbatore 641402, India

<sup>2</sup>Department of ECE, Madha Engineering College, Chennai 600070, India

<sup>3</sup>Department of EEE, SRM Institute of Science and Technology, Kattankulathur, Chennai 603203, India

<sup>4</sup>Mechanical Engineering Department, Wollo University, Kombolcha Institute of Technology, Kombolcha, South Wollo, 208 Amhara, Ethiopia

Correspondence should be addressed to K. Mohana Sundaram; mohanasundaram.k@kpriet.ac.in and Wubishet Degife Mammo; wubishetdegife7@gmail.com

Received 8 September 2021; Revised 9 October 2021; Accepted 18 October 2021; Published 31 October 2021

Academic Editor: Lakshmiathy R

Copyright © 2021 K. Mohana Sundaram et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Designing a hearing aid device is one of the challenging applications recently, since it is useful for the people with hearing loss. For this purpose, various circuit designing procedures such as MOSFET and carbon nanotube field effect transistor (CNTFET) are introduced in the existing works. But it mainly lacks the following drawbacks: increased leakage current, not highly efficient, and increased area and power consumption. In order to mitigate these issues, this paper is aimed at designing an improved CNTFET (ECNFET) for hearing aid filtering application. The major objectives of the proposed work are leakage current minimization and the improvements in transconductance and mobility. At first, the layout is designed with 10 layers based on the specific dimensionalities, and different materials are placed in each and every layer. It includes gold, silicon, silicon dioxide, bismuth telluride, and carbon tube. Then, the parameters such as band gap, electron concentration, hole concentration, electron mobility, hole mobility, and insulator breakage voltage are verified to determine the efficiency of the layout. If all the parameters are satisfied, the characteristics such as voltage current, leakage current, mobility, and transconductance are validated. If all measures are satisfied, the library is created for the designed ECNFET layout by using the Comsol tool. Furthermore, the operational amplifier is designed based on the generated library function. After amplification, the hearing aid filter is designed with the use of the proposed ECNFET layout. The experimental validation of the proposed work and comparison with the existing method based on the measures of area consumption, power consumption, speed, and frequency range confirm the effectiveness of ECNTFET in filtering applications.

## 1. Introduction

In today's world, approximately 10% of people suffer due to the hearing loss in which a small amount people use hearing aid devices. The result of wearing this device is highly efficient with minimum noise and distortion. Moreover, a variety of digital signal processing algorithms is required to design the hearing aid device. Traditionally, some of the existing research works are aimed at developing a hearing aid filter by using the VLSI circuit designing technology. But it poses several challenges like increased power and area

consumption, when compared to other portable devices. So, the layouts such as MOSFET and CNTFET [1] are developed to design this filtering application. The MOSFET is an integrated circuit that is capable of both voltage gain and signal power gain, in which the MOS capacitor is the main part, and then, the application of gate voltages changes the semiconductor operation from p-type to n-type. Furthermore, it functions based on the deflection mode and the enhancement mode [2]. But it has the major constraints such as process variations, short channel effect, and high leakage current issues. Thus, a CNTFET [3] is developed that is the next

generation of MOSFET [4], which uses the carbon nanotube between the source and drain. The major reasons for designing CNTFET are reduced size, high-performance channel material, and mobility enhancement. Normally, the CNT is considered as a rolled-up sheet of graphene, in which the electrical properties are dependent on the chirality of the distortion direction [5]. In CNTFET, the core of integrated circuit is implemented in a single chip that contains four terminal units, namely, source, drain, gate, and body as shown in Figure 1. A CNTFET relates to a FET that uses single or multiple carbon nanotubes as channel being a substitute for bulk silicon found in the conventional MOSFET [6]. Here, the power supply is provided to the source and drain; then the triggering is enabled for the gate. If it is high, the layout goes to on state; otherwise, it goes to off state.

**1.1. Problem Definition.** The procedure of CNTFET [7, 8] is the same as that of MOSFET, in which the source terminal supplies the electrons and it is collected by the drain terminal. The CNTFET is the most widely used technology for the past decades [9]. The dimensional criticality in the silicon material reduced the utilization level for the transistor fabrication [10]. Hence, the research studies focused on the identification of alternatives to improve the density and recital of electronic information system [11]. The gate terminal controls the current intensity [12]. If the transistor is in off stage, there is no gate voltage is supplied [13]. However, it also has some major limitations [14] such as increased area consumption and power consumption, reduced speed and frequency range, and increased leakage current [15]. So, it is highly important to determine whether the hearing aid device is good for the hearing loss patients [16]. To mitigate the issues, this article explores the development of a novel hearing aid filtering application by implementing the CNTFET layout.

**1.2. Objectives.** The objectives modelled from the problem identification are listed as follows:

- (i) To reduce the leakage current
- (ii) To increase the transconductance
- (iii) To increase the electron mobility
- (iv) For these objectives, an enhanced CNTFET (ECNFET) layout is designed and implemented in the hearing aid filtering application
- (v) The novelty behind the proposed work lies in following cases:
  - (i) The design of CNTFET-based hearing aid filter in 2 nm technology with the thickness of 0.6 m
  - (ii) The minimization in layer thickness and the design technology reduce the leakage current compared to the existing models
  - (iii) The reduction of thickness of the layering initiates the thin material design and increases the operational speed simultaneously

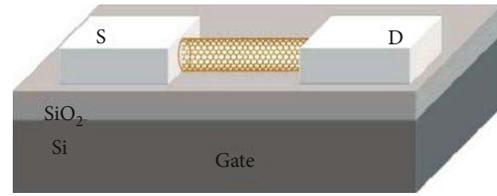


FIGURE 1: Source, drain, and gate of ECNFET layout.

**1.3. Organization.** The article is structured as follows: the existing filtering applications and field effect transistor layouts with its advantages and disadvantages are surveyed in Section 2. The detailed description about the proposed ECNFET-hearing aid filtering application is presented in Section 3. The measured results of both available and proposed filtering applications are evaluated in Section 4. Section 5 provides the overall summary and the future enhancement.

## 2. Associated Works

The existing available FET layout designs used for hearing aid filters are surveyed with their advantages and disadvantages here. The compensation of hearing loss utilizes the device, namely, hearing-aid system, which contains several processes such as amplification, noise removal, suppressing the feedback, and automatic program switching. The amplification of sounds and transferring such sounds to the human ear are the major operations of hearing-aid system. The adjustments of speech signals were performed through the filter bank-based algorithms. Wei and Wang [17] proposed an adjustable filter bank to achieve wave composition based on hearing loss. The changes in 4-bit control signal provide the adjustments in number of subbands and their location. The size optimizing of filter used in hearing-aid system turned the research studies to make the fast-efficient filter with low-power consumption. Kotha et al. [18] discussed the 4:2 compressors for finite impulse response (FIR) design. The realization gate level-17 order filter was illustrated by using Hardware Description Language (HDL). The UMC-90 technology was used to implement the architectures with the integration of Cadence compiler. Recently, the revolution in wireless communications systems changes the people lifestyle and leads to the numerous smart device utilization. Based on the application areas such as environmental monitoring and healthcare monitoring, the frequency ranges were defined. Trivedi et al. [19] pointed out the maximum frequency range for the hearing aid is 6 kHz. Under different biasing conditions, the power dissipation among the components was investigated with the sub-threshold operation. In some cases, the degree of hearing loss was worse against the time variations. For the severe hearing loss, the acoustic-based amplification was insufficient to restore the satisfactory result [20]. Based on these operational constraints, the design of hearing aid filter was the next stage of research FET-based models which was employed to design several models. Under the temperature variations, power and delay consumed by the operating

phases were high and hence, the reduction mechanisms were required.

Nguyen et al. [21] developed a new sensing system, namely, Low cost In-ear Bioelectrical Sensing (LIBS) for providing a solution to healthcare applications. It automatically captured the signal from the ear canal based on the process of data acquisition and signal separation. Also, a Nonnegative Matrix Factorization (NMF) method was introduced to decompose the signal for separation. Yogeshwaran et al. [22] investigated the drain current and delay of the hearing aid device. Here, the relationship between these measures was validated based on the features of ON and OFF. Kuo et al. [23] implemented an ANSI S1.11 filter for designing a digital hearing aid device. The intention of this application was to cancel the echo, reduce the noise, and enhance the speech. The stages involved in this design were filter bank architecture formation, low power optimization, computation reordering, clock gating, and operand isolation. Guo et al. [24] implemented an acoustic feedback cancellation approach for eliminating the probe noise in a hearing aid filter. The intention of this paper was to reduce the convergence rate with the use of probe noise enhancement filters. Here, two different probe noise-based approaches were evaluated for analyzing the suitable approach with increased convergence rate and reduced steady-state error. However, this design strategy failed to reduce the computational complexity.

Kalathil and Elias [25] designed a nonuniform cosine-modulated filter, and the aim of this application was to fulfill the requirements of hearing-impaired people with the use of uniform filter and transition filter. The merits observed from this paper were increased flexibility, reduced complexity, and improved performance. Pandey and Matthews [26] implemented a Spectral Gain Shaping Method (SGSM) for hearing loss compensation with dynamic range compression and noise suppression. Also, the unwanted effects of the long and broadband path delays were reduced with the use of hearing aid signal processing algorithms. Moreover, the spectral gain shaping capability of the hearing aid system was analyzed for reducing the delay. Ngo et al. [27] designed an improved prediction error filter for modelling the acoustic feedback and estimating the feedback signal in a hearing aid system. Here, the correlation between the near-end signal and loudspeaker signal was identified with the use of Prediction Error Method (PEM). Moreover, an energy-based voiced and unvoiced detection was performed by using the Zero Crossing Rate (ZCR) feature. Pandey and Mathews [28] employed an adaptive filtering technique to enhance the sound quality of hearing aid device. The aim of this paper was to increase the hearing aid gain and to reduce the perceptual distortion. Here, the amplification process was controlled and the frequency components were automatically identified. The use of CNTFET sensors in biomedical applications is growing at a rapid pace [29–31].

### 3. Suggested Method

The clear description about the proposed hearing aid filtering application using ECFET layout is provided here. The

design of a hearing aid filter with an enhanced CNTFET layout is the major objective of this paper. In this design, the single-walled nanotube is used for providing high current conductivity. It mainly focused to reduce the leakage current and increase the transconductance and electron mobility. For these purposes, an ECFET layout is designed based on the dimensionalities of length, width, height, CNT thickness, CNT length, and CNT diameter. After designing the circuit, the required materials such as gold, silicon, silicon oxide, bismuth telluride, and carbon are used. Then, the parameters such as band gap, electron concentration, hole concentration, electron mobility, hole mobility, and insulator breakage voltage are considered.

After verifying these parameters, the characteristics such as voltage current, mobility, leakage current, and transconductance of the layout are validated. If the characteristics are satisfied, the library is created by using the Comsol tool. Furthermore, the operation amplifier is designed by using the ECFET layout for increasing the efficiency of filtering application. Finally, the hearing aid filter is designed by implementing this ECFET layout. To demonstrate the superiority of the suggested application, the evaluation parameters such as area, power, frequency, and speed are considered during the evaluation. ECFET flow is shown in Figure 2.

*3.1. Physical Design Based on the Dimensionality Analysis.* At first, the ECFET layout is designed based on the specific dimension of each layer. It contains 10 layers, in which different materials are placed in each layer. Layers 1 and 3 are termed as intralayers, and layer 2 is termed as interlayer. Then, layer 5 acts as a source, layer 8 acts as gate, and layer 10 acts as a drain. Also, layers 4, 7, and 9 act as either p-substrates or n-substrates; finally, the CNT is placed in layer 6. The layout design is represented in Figure 3, in which the dimensionalities are determined based on rules of circuit designing. The rules specified that the entire layout should contain the minimum width of  $2\lambda$  and height of  $1.5\lambda$ , if the layout design does not follow these rules, it is termed as a worst case design. In the proposed design, the height of the ECFET is  $1\lambda$  and the width is  $2\lambda$ . Also, each and every layer should follow some dimensionalities for a good design. The intralayers (i.e., D1 and D3) have the height of 0.2 nm and width of 2 nm, because these dimensions provide an increased doping concentration. Also, it has a minimum opening for allowing the current conductance from electrons to holes and holes to electrons. Then, the inter layer (i.e., D2) has the height of 0.2 nm and width of 2 nm, because it offers an increased conductance and peak doping concentration. The p-type and n-type substrates (i.e., D4, D9, and D7) have the height of 0.2 nm and width of 0.7 nm, because it controls the materials based on the resistance. Moreover, the source, drain, and gate layers (i.e., D5, D8, and D10) have the height of 0.1 nm and width of 0.4 nm, because they offer a high-level implant and energy. Finally, the CNT that is placed in D6 has the height of 0.1 nm, width of 0.6 nm, and diameter of 0.6 nm, which is placed between the source and drain for increasing the conductivity.

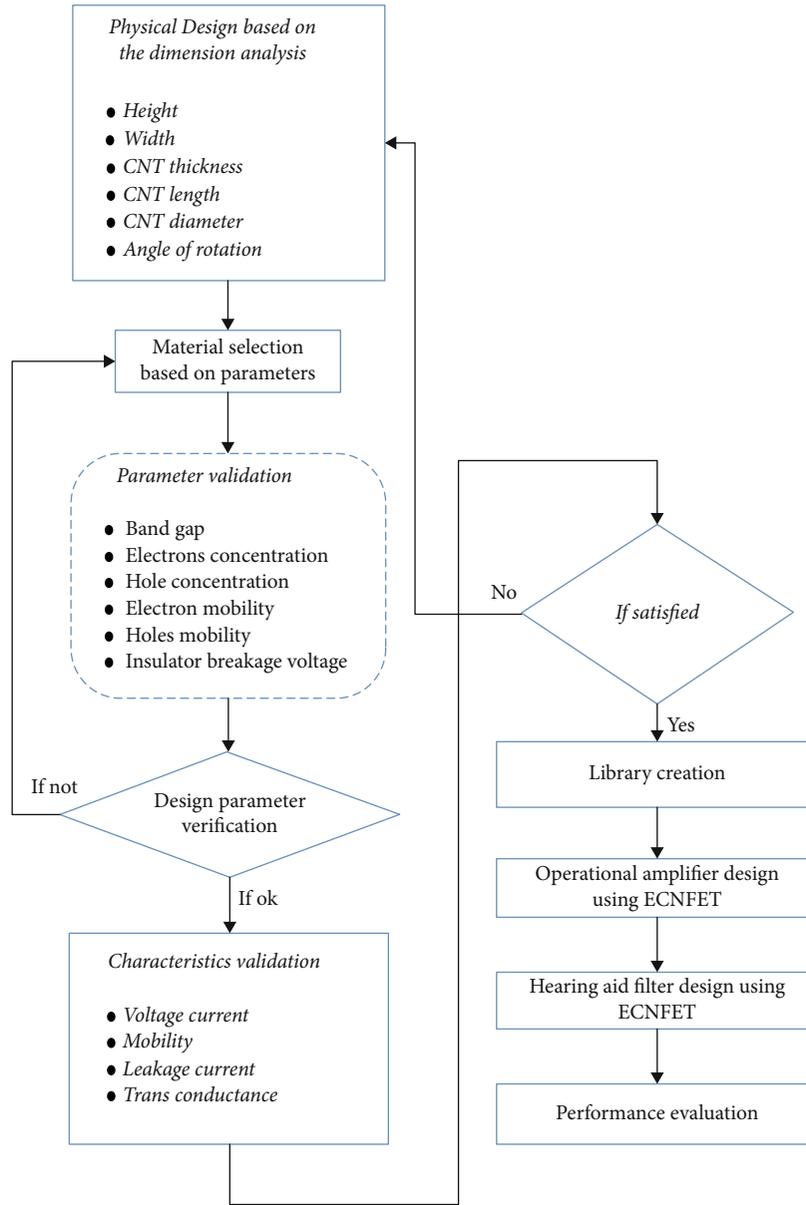


FIGURE 2: Flow of the ECFET-based hearing aid filtering.

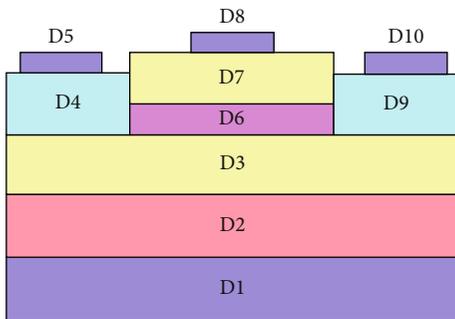


FIGURE 3: Layout design with different materials.

3.2. *Material Selection.* After designing the layout, different materials are placed in each and every layer, which includes gold, silicon, quartz, bismuth telluride, and carbon nanotube. The main reasons of using gold are it increases the conductivity of semiconductor and accuracy and improves the movement of electrons to holes and holes to electrons. This material is placed in the layers of D1, D5, D8, and D10. The silicon is considered the second-best material that is placed in D2, which provides little flow electricity when it acts as a semiconductor. Then, the silicon dioxide is placed in D3 and D7, which provides an increased dielectric strength and acts as an excellent insulator. Also, it can function even in high temperature. Bismuth telluride is placed in D4 and D9, which provides low lattice thermal conductivity. Moreover, it acts as a power generation device and is used in both p-type and n-type substrates. Finally, the single-walled thin

CNT is placed in D6, which reduces the diameter size by using the single graphite sheet. Due to this, the size of transistor component is reduced to 2 nm.

**3.3. Parameter Verification.** After selecting the materials, the parameters such as band gap, electron concentration, hole concentration, electron mobility, hole mobility, and insulator breakage voltage are validated [32]. As for band gap, the energy band gap of the circuit is highly depending on the materials that are used for circuit designing.

The materials or insulators having the energy gap of 1 eV are termed as semiconductors. It is calculated as follows:

$$E_g = E_c - E_v, \quad (1)$$

$$E_g = 1.210 - 3.60 \times 10^{-4} \times T \text{ eV}, \quad (2)$$

where  $T$  indicates the temperature, eV indicates the electron volts,  $E_g$  represents the energy band gap,  $E_c$  is the conduction band, and  $E_v$  is the valence band.

**3.3.1. Electron Concentration.** The electron concentration is defined as the concentration of electrons in the conduction band. Here, the intrinsic concentration is calculated for both n-type and p-type transistors, which is shown below:

$$n_i = N_c e^{((E_F - E_c)/kT)}, \quad (3)$$

where  $N_c = (2\pi m_e kT/h^2)^{3/2}$ .

**3.3.2. Hole Concentration.** The hole concentration is defined as the concentration of electrons in the valence band, which is calculated as follows:

$$p_i = N_v e^{((E_v - E_F)/kT)}, \quad (4)$$

where  $N_v = 2(2\pi m_h kT/h^2)^{3/2}$ , where  $N_c$  is effective density of states in the conduction band,  $N_v$  is effective densities of states in the valence band,  $k$  is Boltzmann constant,  $T$  is temperature,  $E_F$  is Fermi energy,  $E_v$  is valence band level,  $E_c$  is conduction band level,  $m_h$  is effective mass of a hole,  $m_e$  is effective mass of an electron, and  $h$  is Planck constant  $6.624 \times 10^{-34}$  Js.

**3.3.3. Electron Mobility.** The movement of electrons through a semiconductor or metal is characterized by using the electron mobility. It is estimated as follows:

$$v_d = \mu E. \quad (5)$$

**3.3.4. Hole Mobility.** Typically, there is an analogous quantity for holes in a semiconductor, which is generally lower than the electron mobility. It is estimated as follows:

$$v_d = \mu H, \quad (6)$$

where  $\mu$  represents the mobility,  $E$  is the electric field,  $H$  represents the holes, and  $v_d$  is the drift velocity.

**3.3.5. Insulator Breakage Voltage.** This should be minimum, because it causes some portion of an insulator as an electrically conductive. It is calculated as follows:

$$V_{\text{breakdown}} = B \times p \times \frac{d}{(C + \ln(p \times d))}, \quad (7)$$

where  $p$  is pressure of the gas,  $d$  represents the distance between two conducting plates, and  $B$  and  $C$  are the constants that are determined based on the experiments. Based on these parameters, the effectiveness of the layout is determined; if these measures are fully satisfied, the characteristics of the layout are validated.

**3.4. Characteristic Validation.** After verifying the measures, the major characteristics of the layout is validated; this includes voltage current, mobility, leakage current, and transconductance. The controlling of voltage and flow of current between the source and drain through the proposed ECFET model reduced leakage current [33].

**3.4.1. Voltage Current.** It is defined as the amount of current taken for the movement of electrons to holes and holes to electrons. It is calculated as follows:

$$I = \mu W c_i \times \frac{(V_{GS} - V_T)V}{L}, \quad (8)$$

where  $\mu$  is the mobility and  $I$  indicate the current.

**3.4.2. Transconductance.** The transconductance is also called as mutual conductance, in which the electrical characteristics are related to the output current through the device and the input voltage across the device. Also, the conductance is represented as the reciprocal of the resistance.

$$g_m = \frac{dI_d}{dV_{GS}} \Big|_{V_{DS}}, \quad (9)$$

where  $g_m$  is transconductance,  $I_d$  is drain current,  $V_{GS}$  is gate source voltage, and  $V_{DS}$  is drain source voltage.

**3.4.3. Leakage Current.** It is an important conduction of PN junction diode, in which the width of the depletion region is increased, when a diode is reverse biased. This condition is required to restrict the current carrier accumulation. The depletion region acts as an insulator, if the majority of current carriers are primarily negated. It is calculated as follows:

$$I = I_0 e^{-Ee/2kT}. \quad (10)$$

$I_0$  is the initial current,  $E$  defines the electrons, and  $e$  is the permittivity. Here and mainly, the leakage current reduction is concentrated, because it leads to the band-to-band tunnelling leakage.

**3.5. ECFET Layout Design and Library Creation.** After triggering, the transistors are enabled by using the analytic doping model, in which the P, N, and P are substrates in the P-type transistor, and the N, P, and N are substrates in

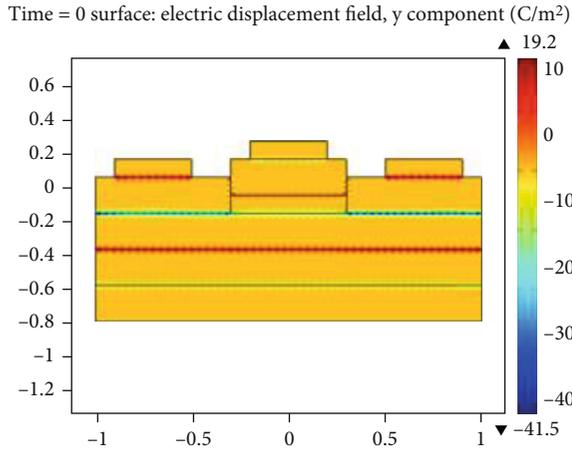


FIGURE 4: ECNFET layout design.

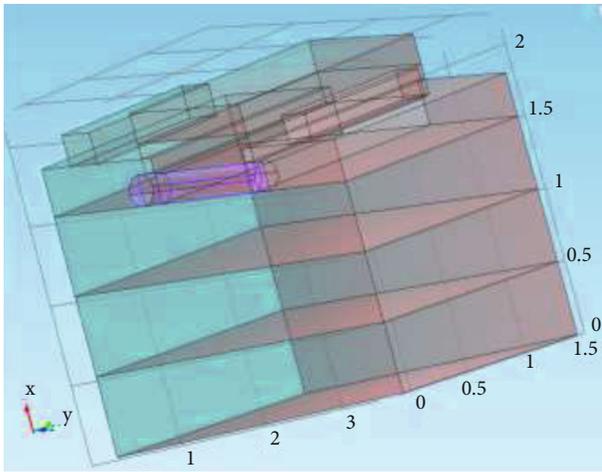


FIGURE 5: 3D representation of ECNFET.

the N-type transistor. In this layout, the semiconductor is placed in between the source and drain under the oxide layer domain. Furthermore, the application of positive and negative voltages on gate terminal switches the operation between n-type and p-type transistors. Here, the holes across the oxide layer are pushed downward to the substrate, when the positive gate voltage is applied. Then, the bound negative charges populate the deflection region with the acceptor atoms. The current flows freely once the voltage is applied between the drain and source; then, the electrons in the channel are controlled by the gate voltage. The hole channel is made under the oxide, when the negative voltage is supplied. The designed ECNFET layout is shown in Figure 4, and its 3D representation is shown in Figure 5. After that, the library is generated for both p-type and n-type transistors by using the Comsol tool. Then, the generated libraries are given to the input of filtering for noise removal.

**3.6. Operational Amplifier Design.** The ECNFET is a kind of semiconductor device that is mainly used to amplify the signals in the electronic devices. Figure 6 shows the opera-

tional amplifier [34] with the 7 ECNFETs which are used as a p-type transistor, and 5 ECNFETs are used as an n-type transistor. Also, one capacitor is used to avoid the current loss, which is  $0.1 \mu\text{f}$ . This layout gets the low-level frequency as input and provides an improved frequency as output. In this design, the  $V_d$  is taken as  $10 \text{ mw}$  and  $V_g$  is taken as  $2 \text{ v}$ .

The op-amp design using the proposed ECNFET operates at the constant common mode voltage close to source voltage. The input to the op-amp stage is simplified with the Miller-compensated simplified voltage supply. The proposed op-amp comprises the cascaded Miller-compensated stage and output stage to minimize the power intake. The input and output waveforms with frequency variations are illustrated in Figure 7.

With the linear increase of frequencies from  $2 \text{ kHz}$  to  $10 \text{ kHz}$ , the voltage variations are graphically depicted in Figure 7. The stable operating point for the voltage and current is observed after the frequency range  $2 \text{ kHz}$ .

The major benefits of the ECNFET-hearing aid filter shown in Figure 8 are as follows:

It helps to increase the speed of transistor.

It avoids the current loss by designing the capacitor with  $0.1 \mu\text{f}$ .

It efficiently reduces the noise by designing the hearing aid using the ECNFET layout.

The output voltage waveform variations with respect to the time period clearly demonstrate the operation of filter design using the ECNFET model. It is shown in Figure 9.

For the minimum time period ( $50 \text{ ns}$ ), the output voltage is in maximum state. When the simulation period is linearly increased from the minimum to maximum value ( $500 \text{ ns}$ ), the voltage value is decreased to low value due to the reduction in drain current under the constant drain-to-source voltage.

## 4. Performance Analysis

The results of both existing and proposed hearing aid filtering applications are measured and equated depending on the measures of leakage current, mobility, transconductance, voltage current, voltage current, area consumption, power consumption, speed, and frequency. The software tools used to implement the proposed work are Comsol 5.0, Electric 9.07, and H-spice J2014. The operating phases of the proposed CNTFET-based hearing aid filter design are layout design, library creation for electric properties, and the performance evaluation. Initially, Comsol 5.0 is used to design the layout with the material specification. In general, there are five materials employed to design the CNTFET such as gold, silicon, graphite, carbon, and  $\text{SiO}_2$ . But, gold and  $\text{SiO}_2$  are used for our proposed work. Then, the electrical properties are defined as the library which is performed by the software electric tool. The layout is considered as the base for the electric property's declaration. Once the layout and electric properties are completed, the numerical variations of current, voltage, and the mobility for the design are investigated to state the effectiveness of the proposed work. This is achieved

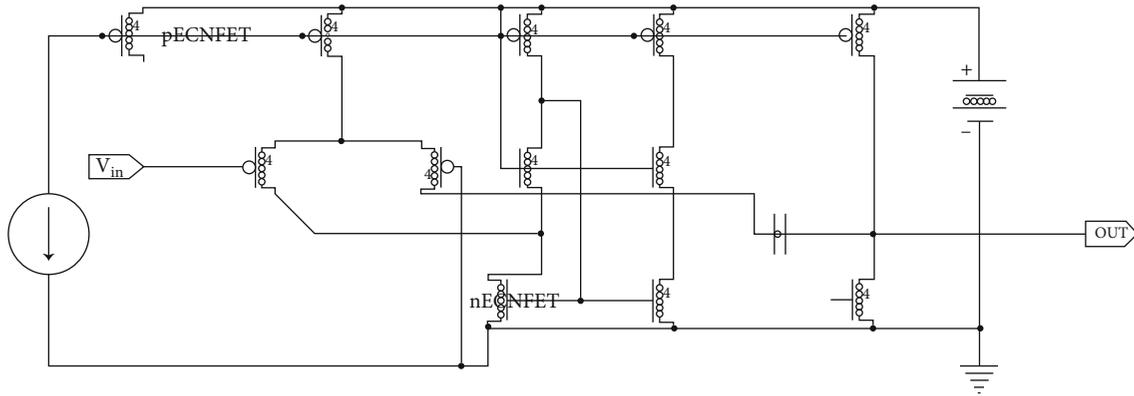


FIGURE 6: Design of operational amplifier.

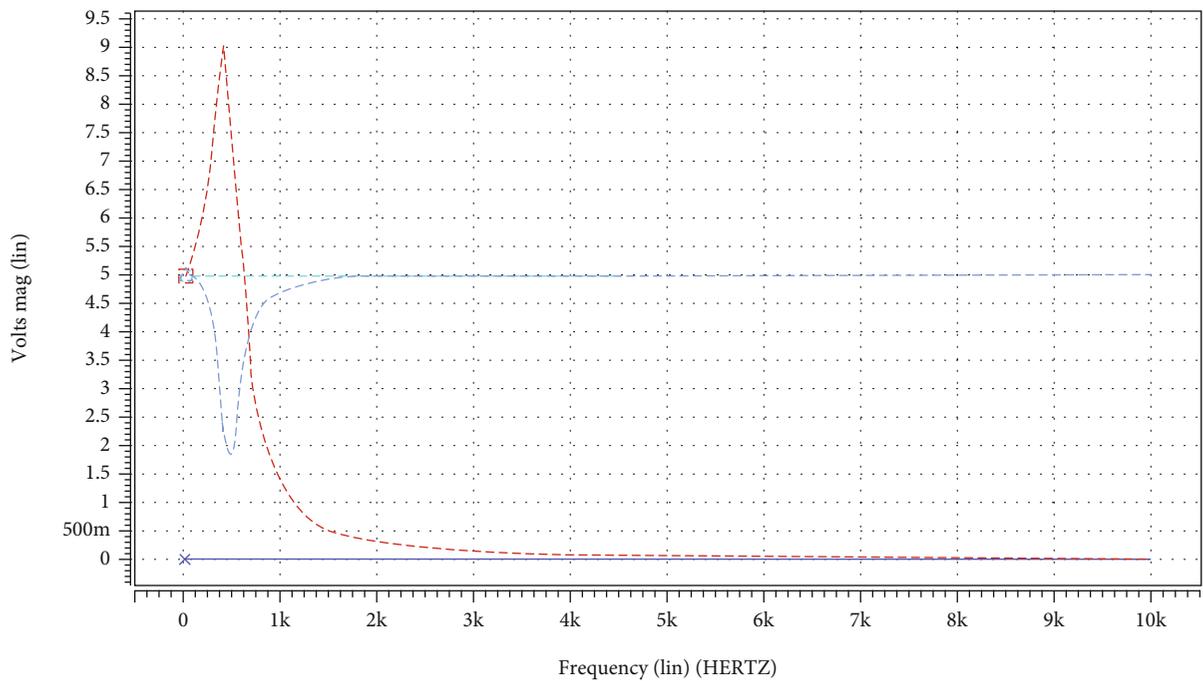


FIGURE 7: Output voltage analysis.

by using the H-spice simulation tool. Hence, the integration of three software tools is the major requirement for our proposed work.

**4.1. Leakage Current.** Figure 10 graphically illustrates the leakage current of the proposed ECNFET design with respect to the gate voltage. The leakage current can flow between the source and drain, which is linearly increased with the increase of the gate voltage by minimum leakage current in nanoamps (nA) [33]. In the proposed application, the overall leakage current is reduced to 0.02 nA by using the ECNFET layout.

Figure 11 represents the drain current variations for the proposed ECNFET. With respect to gate-to-source voltage, there is a linear increase of gate-to-source voltage. The graphical variations of drain current show that it increased to 1.65 mA by using the ECNFET layout. On the basis of

the threshold and saturation, the overall peak value of the current is estimated.

**4.2. Mobility.** The mobility defines the movement of electrons and holes from n-substrate to p-substrate, in which the electron conductivity and electron charge carrier are increased, when compared to the holes. The mobility of the proposed ECNFET layout is shown in Figure 12. The linear increase in gate voltage from 0 to 2 V increases the mobility values linearly.

**4.3. Transconductance.** Typically, the transconductance of ECNFET is based on the current of output device and the voltage of input device. Figure 13 shows the transconductance of the ECNFET design. From the evaluation, it is observed that the transconductance is improved with respect to the varying gate source voltage and is evaluated in terms of  $V_{GS}$ .

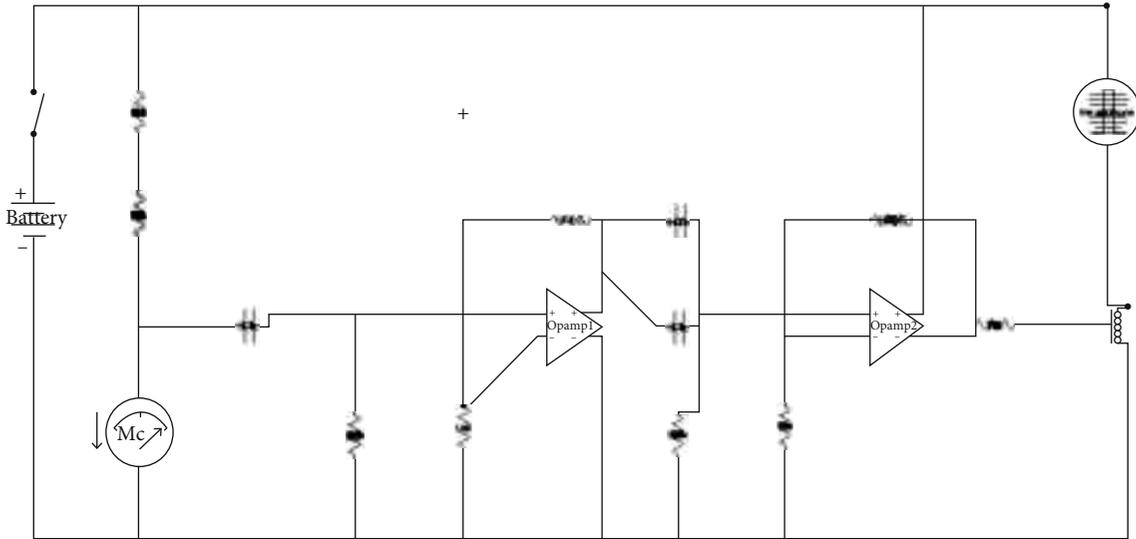


FIGURE 8: Hearing and filtering application.

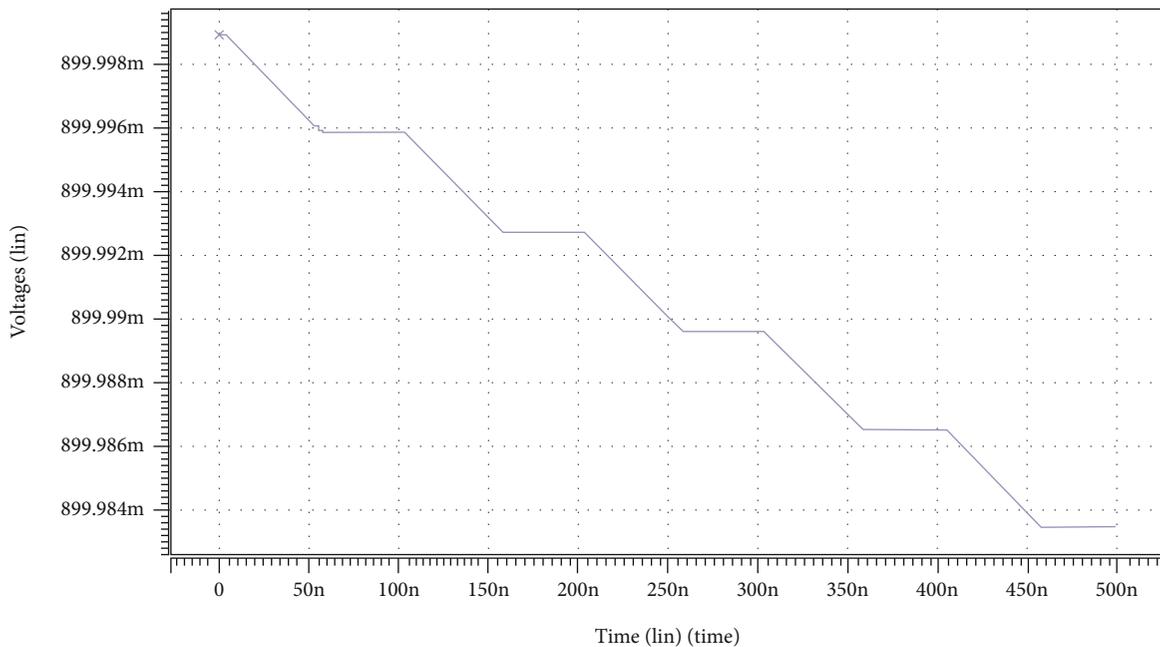


FIGURE 9: Filter output.

4.4. *Area, Power, Frequency, and Speed.* Table 1 provides the area consumption, power intake, frequency, and speed of both the existing CNTFET-based filtering design and the proposed ECNFET layout-based filtering design. Here, the amount of area and power required to design the layout is drastically reduced with the increase in the frequency range and speed. In this design, the best materials are used in this circuit design, which reduces the area and power consumption. Also, the operational amplifier improves the frequency range by amplifying the ECNFET layout. Moreover, the hearing aid filter improves the overall efficiency and speed of the system. Based upon the results, it is found that the

suggested ECNFET-based hearing aid filtering design provides the better performance, in comparison to the available filtering design.

4.5. *Comparative Analysis.* Table 2 shows the threshold voltage of existing CNTFET and proposed ECNFET layouts based on varying temperatures. Due to the less heat dissipation mechanism, the heating effect of ECNFET is lower than that of CNTFET, in which the highest value appears in both source and drain, because the heat is nonuniformly distributed. Here, the threshold voltage is calculated with respect to various temperature values, which evaluates the optimized

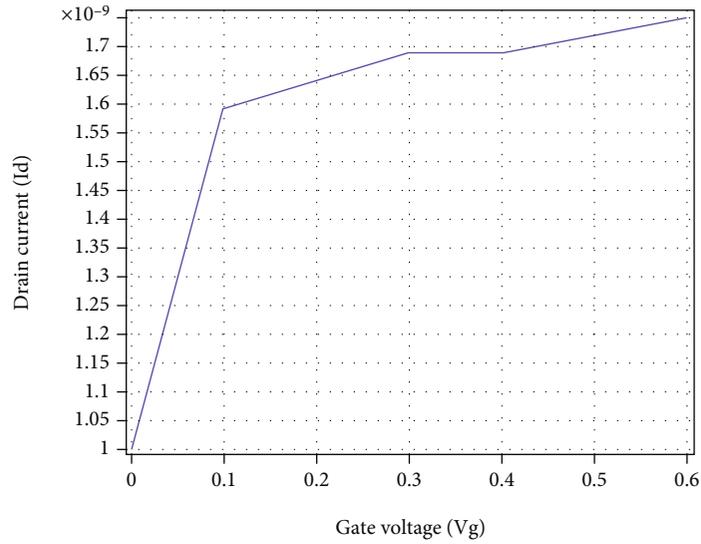


FIGURE 10: Leakage current.

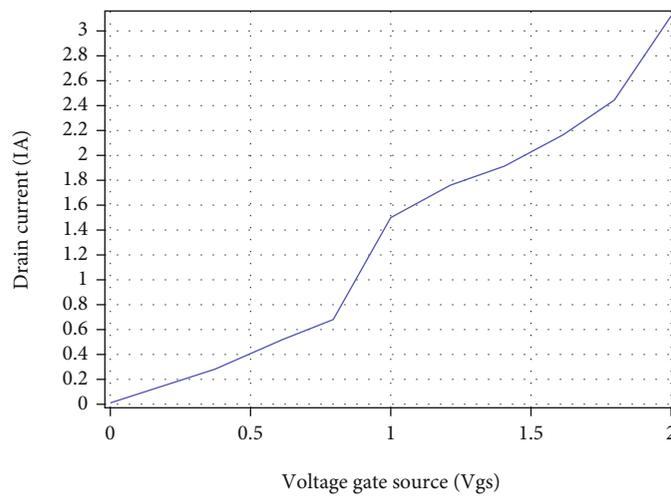


FIGURE 11: Voltage current.

usage of voltage by the proposed layout. Moreover, different temperatures from 27°C to 227°C are taken to analyze the threshold voltage. For minimum temperature values (27°C), the threshold voltage values for CNTFET and ECNFET are 0.210 and 0.205 V, respectively. Similarly, they are 0.164 and 0.160 V for maximum temperature values 227°C, respectively. The comparative analysis between the proposed ECNFET with the CNTFET shows that the proposed model reduces the threshold voltage values by 2.38 and 2.44%, respectively.

Table 3 compares the threshold voltage of CNTFET and ECNFET with respect to gold and silicon dioxide materials. The threshold voltage variations on CNTFET and ECNFET corresponding to gold and SiO<sub>2</sub> are illustrated in Table 3. In this analysis, various materials are used for estimating the threshold voltage, because each layer has separate voltage. So, selecting an appropriate material for each layer is an

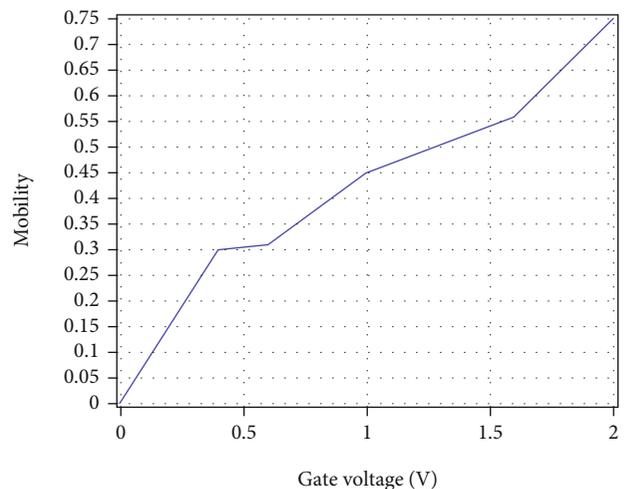


FIGURE 12: Mobility graph.

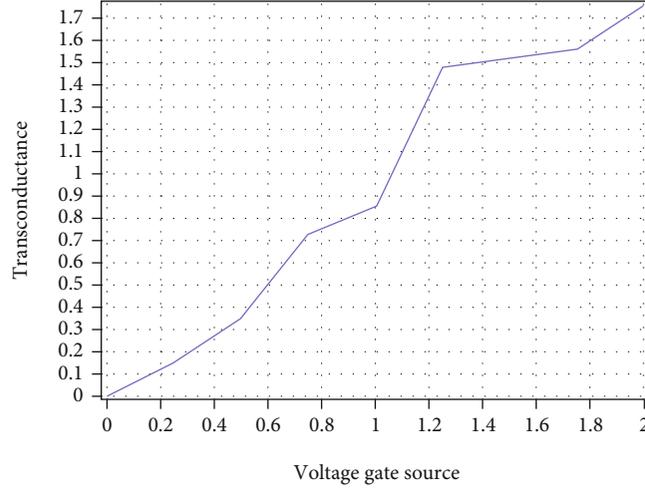


FIGURE 13: Transconductance analysis.

TABLE 1: Performance analysis of ECNFET.

Measures	Existing CNTFET filter	Proposed ECNFET hearing aid filter
Area [35]	151 components	134 components
Power [36]	58.96 $\mu$ W	26.03 $\mu$ W
Frequency	$1.9 \times 10^3$ Hz	$2 \times 10^3$ Hz
Speed [37]	$2.8 \times 10^9$ m/s	$4 \times 10^{11}$ m/s
Delay [37]	$7.4e^{-12}$	$6.63e^{-14}$

TABLE 2: Threshold voltage with respect to temperature.

Temperature ( $^{\circ}$ C)	Threshold voltage (V)	
	CNTFET	ECNFET
27	0.210	0.205
47	0.210	0.205
67	0.210	0.204
87	0.210	0.204
107	0.202	0.198
127	0.198	0.197
147	0.194	0.193
167	0.191	0.186
187	0.187	0.182
207	0.180	0.174
227	0.164	0.160

TABLE 3: Threshold voltage with respect to different materials.

Materials	Threshold voltage (V)	
	CNTFET	ECNFET
Gold	0.210	0.205
Silicon dioxide (SiO <sub>2</sub> )	0.240	0.235

important process. For gold material, the threshold voltage values for CNTFET and ECNFET are 0.210 and 0.205 V, respectively. Similarly, they are 0.240 and 0.230 V for SiO<sub>2</sub>. The proposed design reduces the voltage values by 2.38 and 4.17%, respectively.

Table 4 compares the drain voltage of the existing CNFET and proposed ECNFET with respect to varying dielectric constants and drain current. The necessity of the drain voltage is decreased for a specific drain current in an ECNFET device. Here, the electric constant is varied for estimating the current value; based on this, the current consumption of the proposed ECNFET layout is calculated. Also, the voltage consumption is highly depending on the current consumption or resistance, so the current consumption must be reduced. Here, the current consumption is reduced with the increase of electric constant.

The reduction of gate layer thickness of 0.6 nm in the proposed layout design reduces the drain voltage further compared to CNTFET models. For the high value of drain current (80  $\mu$ A) and dielectric constant (19), the drain voltage for CNTFET and ECNFET is 0.40 and 0.39 V, respectively. The comparative analysis between the proposed ECNFET with the existing CNTFET models shows that the proposed ECNFET provides the 2.5% reduction compared to the CNTFET model, respectively.

#### 4.5.1. Limitations of CNTFET

- (i) When modelling CNTFETs, a consistent model that is suitable for both analogue and digital applications and capable of mass production must be developed
- (ii) The fault tolerance of CNTFET circuits should be investigated
- (iii) Scalability of CNTFETs should be thoroughly investigated
- (iv) It is necessary to discover new materials for the synthesis and integration of CNTFETs

TABLE 4: Comparative analysis based on dielectric constant and drain voltage.

Dielectric constant	Drain current							
	20 ( $\mu\text{A}$ )		40 ( $\mu\text{A}$ )		60 ( $\mu\text{A}$ )		80 ( $\mu\text{A}$ )	
	CNTFET	ECNFET	CNTFET	ECNFET	CNTFET	ECNFET	CNTFET	ECNFET
3.9	0.30	0.29	0.56	0.54	0.84	0.83	—	0.74
9.0	0.15	0.14	0.28	0.28	0.44	0.40	0.56	0.53
15.6	0.11	0.10	0.22	0.20	0.33	0.31	0.44	0.41
19.0	0.12	0.11	0.18	0.17	0.30	0.27	0.40	0.39

## 5. Conclusions

This paper designs a new hearing aid filtering application by using an ECNFET layout. Here, five different materials such as gold, silicon, silicon dioxide, bismuth telluride, and single-walled carbon nanotube are placed in the layers, which are selected based on their specific advantages. After selecting these materials, the parameters such as band gap, electron concentration, hole concentration, electron mobility, hole mobility, and insulator breakage voltage are validated. If all the parameters are satisfied, the characteristics of the layout are validated for proving the effectiveness of the proposed design. It includes voltage current, transconductance, mobility, and leakage current, which are all satisfied; the library is created for the corresponding ECNFET layout by using the Comsol tool. After that, the operational amplifier is designed based on the generated library function, which is used to improve the level of frequency. Finally, the hearing aid filter is implemented with the use of ECNFET layout that improves the accuracy of filter by efficiently reducing the noise. The experimental results evaluate the performance of this application based on different performance measures such as area consumption, power consumption, frequency range, and speed. The proposed ECNFET-hearing aid filter provides the better performance in drain voltage, current, threshold voltage, and mobility compared to the existing layout designs.

The proposed ECNFET layout can be used to some other applications such as head phone, telephone, and biomedical devices in the future. The parameter estimation of CNTFET could be investigated further using other cutting-edge intelligent optimization algorithms. The most recent materials may be incorporated into the design of a CNTFET in order to identify the one that will yield the longest life of the CNTFET as well as the best performance.

## Data Availability

The data used to support the findings of this study are included within the article. Should further data or information be required, these are available from the corresponding author upon request.

## Disclosure

This study was performed as a part of the Employment of Kombolcha Institute of Technology, Wollo University, Kombolcha, Amhara, Ethiopia.

## Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

## Acknowledgments

The authors thank the KPR Institute of Engineering and Technology, Coimbatore, for providing characterization supports to complete this research work.

## References

- [1] H. Gautam and P. Bindra, "Structure and a detailed analysis of various simulation results of CNTFET: a review," *International Journal of Scientific Engineering and Technology*, vol. 4, no. 2, pp. 32–35, 2015.
- [2] S. Yogeshwaran, L. Natrayan, S. Rajaraman, S. Parthasarathi, and S. Nestro, "Experimental investigation on mechanical properties of epoxy/graphene/fish scale and fermented spinach hybrid bio composite by hand lay-up technique," *Materials Today: Proceedings*, vol. 37, no. 2, pp. 1578–1583, 2021.
- [3] A. G. N. Raeini, Z. Kordrostami, and M. Javaheri, "High on/off current ratio in SB-CNTFET based on tuning the gate insulator parameters for different ambient temperatures," in *Nano/Micro Engineered and Molecular Systems (NEMS), 2015 IEEE 10th International Conference on, 2015*, pp. 630–634, Xi'an, China, 2015.
- [4] S. K. Sinha and S. Chaudhury, "Impact of oxide thickness on gate capacitance—a comprehensive analysis on MOSFET, nanowire FET, and CNTFET devices," *IEEE Transactions on Nanotechnology*, vol. 12, no. 6, pp. 958–964, 2013.
- [5] M. S. Ansari and S. Tripathi, "Carbon nanotubes as FET channel: analog design optimization considering CNT parameter variability," in *IOP Conference Series: Materials Science and Engineering*, p. 012167, India, 2017.
- [6] P. Prakash, K. Mohana Sundaram, and M. Anto Bennet, "A review on carbon nanotube field effect transistors (CNTFETs) for ultra-low power applications," *Renewable and Sustainable Energy Reviews*, vol. 89, pp. 194–203, 2018.
- [7] B. N. Kumar, A. K. Singh, C. Prabhu, C. Venkataseshiaiah, and G. C. Sheng, "Compact analytical model for one dimensional carbon nanotube field effect transistor (CNTFET)," *ECS Solid State Letters*, vol. 4, no. 6, pp. M12–M14, 2015.
- [8] K. Hemalatha, C. James, L. Natrayan, and V. Swamynadh, "Analysis of RCC T-beam and prestressed concrete box girder bridges super structure under different span conditions," *Materials Today: Proceedings*, vol. 37, no. 2, pp. 1507–1516, 2021.

- [9] S. G. Shirazi and S. Mirzakhuchaki, "High on/off current ratio in ballistic CNTFETs based on tuning the gate insulator parameters for different ambient temperatures," *Applied Physics A*, vol. 113, no. 2, pp. 447–457, 2013.
- [10] N. Ghaderi and M. Alidadi-Shamsabadi, "A novel ultra high speed and low power phase detector using carbon nanotube field effect transistors," in *Electrical and Electronics Engineering (ELECO), 2017 10th International Conference on*, pp. 467–471, Bursa, Turkey, 2017.
- [11] W. Makni, I. Barrage, H. Samet, M. Masmoudi, and M. Najari, "Low noise high frequency CNTFET amplifier," in *Design & Technology of Integrated Systems in Nanoscale Era (DTIS), 2013 8th International Conference on*, pp. 45–49, Abu Dhabi, United Arab, 2013.
- [12] M. Moghaddam, M. H. Moaiyeri, and M. Eshghi, "Design and evaluation of an efficient Schmitt trigger-based hardened latch in CNTFET technology," *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 1, pp. 267–277, 2017.
- [13] S.-A. Imam, N. Kalam, and S. Abdullah, "Comparative analysis of control coefficients on the performance of CNTFET under different parameters," *International Journal of Nanoscience*, vol. 15, no. 3, p. 1640005, 2016.
- [14] S. K. Sinha and S. Chaudhury, "Comparative study of leakage power in CNTFET over MOSFET device," *Journal of Semiconductors*, vol. 35, no. 11, p. 114002, 2014.
- [15] A. K. Dadori, K. Khare, T. Gupta, and R. Singh, "Leakage power reduction technique by using multigate FinFET in DSM technology," in *Proceedings of International Conference on Communication and Networks, 2017*, pp. 233–244, Ahmedabad, India, 2017.
- [16] M. Sandeep Kauthsa Sharma, S. Umadevi, Y. Sai Sampath et al., "Mechanical behavior of silica fume concrete filled with steel tubular composite column," *Advances in Materials Science and Engineering*, vol. 2021, Article ID 3632991, 9 pages, 2021.
- [17] Y. Wei and Y. Wang, "Design of low complexity adjustable filter bank for personalized hearing aid solutions," *IEEE/ACM Trans Audio Speech Lang Process*, vol. 23, no. 5, pp. 923–931, 2015.
- [18] S. R. Kotha, D. Bilaye, U. Jain, and S. S. Kumar, "An approach for efficient FIR filter design for hearing aid application," in *VLSI Design and Test, 18th International Symposium on, 2014*, pp. 1–5, IEEE, 2014.
- [19] A. R. Trivedi, S. Carlo, and S. Mukhopadhyay, "Exploring tunnel-FET for ultra low power analog applications: a case study on operational transconductance amplifier," *Proceedings of the 50th annual design automation conference, 2013*, , IEEE, p. 109, 2013.
- [20] V. Paranthaman, K. Shanmuga Sundaram, and L. Natrayan, "Influence of SiC particles on mechanical and microstructural properties of modified interlock friction stir weld lap joint for automotive grade aluminium alloy," *Silicon*, vol. 4, pp. 1–11, 2021.
- [21] A. Nguyen, Z. Raghebi, F. Banaei-kashani, A. C. Halbower, and T. Vu, "LIBS: a low-cost in-ear bioelectrical sensing solution for healthcare applications," in *Proceedings of the Eighth Wireless of the Students, by the Students, and for the Students Workshop*, pp. 33–35, New York, NY, USA, 2016.
- [22] S. Yogeshwaran, L. Natrayan, G. Udhayakumar, G. Godwin, and L. Yuvaraj, "Effect of waste tyre particles reinforcement on mechanical properties of jute and abaca fiber- epoxy hybrid composites with pre-treatment," *Materials Today: Proceedings*, vol. 37, no. 2, pp. 1377–1380, 2021.
- [23] Y.-T. Kuo, T.-J. Lin, Y.-T. Li, and C.-W. Liu, "Design and implementation of low-power ANSI S1. 11 filter bank for digital hearing aids," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, pp. 1684–1696, 2010.
- [24] M. Guo, S. H. Jensen, and J. Jensen, "Novel acoustic feedback cancellation approaches in hearing aid applications using probe noise and probe noise enhancement," *IEEE Transactions on Audio, Speech and Language Processing*, vol. 20, no. 9, pp. 2549–2563, 2012.
- [25] S. Kalathil and E. Elias, "Efficient design of non-uniform cosine modulated filter banks for digital hearing aids," *AEU International Journal of Electronics and Communications*, vol. 69, no. 9, pp. 1314–1320, 2015.
- [26] A. Pandey and V. J. Mathews, "Low-delay signal processing for digital hearing aids," *IEEE Transactions on Audio, Speech and Language Processing*, vol. 19, no. 4, pp. 699–710, 2011.
- [27] K. Ngo, T. Van Waterschoot, M. G. Christensen, M. Moonen, and S. H. Jensen, "Improved prediction error filters for adaptive feedback cancellation in hearing aids," *Signal Processing*, vol. 93, no. 11, pp. 3062–3075, 2013.
- [28] A. Pandey and V. J. Mathews, "Improving adaptive feedback cancellation in digital hearing aids through offending frequency suppression," in *Acoustics Speech and Signal Processing (ICASSP), 2010 IEEE International Conference on, 2010*, pp. 173–176, Dallas, TX, USA, 2010.
- [29] S. S. Alabsi, A. Y. Ahmed, J. O. Dennis, M. H. M. Khir, and A. S. Algamili, "A review of carbon nanotubes field effect-based biosensors," *IEEE Access*, vol. 8, pp. 69509–69521, 2020.
- [30] V. D. Bezzon, T. L. Montanheiro, B. R. de Menezes et al., "Carbon nanostructure-based sensors: a brief review on recent advances," *Advances in Materials Science and Engineering*, vol. 2019, 21 pages, 2019.
- [31] B. K. Santhoshi, K. Mohanasundaram, and L. A. Kumar, "ANN-based dynamic control and energy management of inverter and battery in a grid-tied hybrid renewable power system fed through switched Z-source converter," *Electrical Engineering*, vol. 103, pp. 2285–2301, 2021.
- [32] W. Shockley, "Electrons and holes in semiconductors," vol. 471, p. 237, 1952.
- [33] Q. Gong, *Fabrication and Characterization of Carbon Nanotube Random Network Transistors*, Universität München, 2015.
- [34] L. Marques, C. Galup-Montoro, and M. Schneider, "A switched-MOSFET filter for application in hearing aid devices," in *Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on*, pp. 77–80, Sydney, NSW, Australia, 2001.
- [35] M. Bahadori, M. Kamal, A. Afzali-Kusha, and M. Pedram, "High-speed and energy-efficient carry skip adder operating under a wide range of supply voltage levels," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 2, pp. 421–433, 2016.
- [36] P. Bhattacharyya, B. Kundu, S. Ghosh, V. Kumar, and A. Dandapat, "Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 10, pp. 2001–2008, 2015.
- [37] R. P. Somnini, B. Madhavi, and K. L. Kishore, "Low leakage CNTFET SRAM cells," *Procedia Computer Science*, vol. 57, pp. 1049–1056, 2015.