

Research Article

Novel Design for Quantum Dots Cellular Automata to Obtain Fault-Tolerant Majority Gate

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Received 29 November 2011; Revised 4 January 2012; Accepted 10 January 2012

Academic Editor: Arturo I. Martinez

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Quantum-dot Cellular Automata (QCA) is one of the most attractive technologies for computing at nanoscale. The principle element in QCA is majority gate. In this paper, fault-tolerance properties of the majority gate is analyzed. This component is suitable for designing fault-tolerant QCA circuits. We analyze fault-tolerance properties of three-input majority gate in terms of misalignment, missing, and dislocation cells. In order to verify the functionality of the proposed component some physical proofs using kink energy (the difference in electrostatic energy between the two polarization states) and computer simulations using QCA Designer tool are provided. Our results clearly demonstrate that the redundant version of the majority gate is more robust than the standard style for this gate.

1. Introduction

Current CMOS technology is going to approach a scaling limitation in deep nanometer technologies. The CMOS technology in nanoscales experienced some problems due to increase in amounts of variation in every aspect of a nanometer design. Quantum-dot cellular automata (QCA) is one of the promising new technologies for future generation ICs that overcome the limitation of CMOS [1–3]. The fundamental unit of QCA-based design is majority gate; hence, efficient construction of QCA circuits using majority gates has attracted a lot of attention [4–9].

Since every QCA circuit can be implemented by using only majority and inverter gates, inverter becomes another important component in constructing QCA circuits. Hence, efficiently constructing an inverter in QCA is of great importance [10–12].

Fault-tolerant design of QCA logic circuits is absolutely necessary for characterization of defective behavior of QCA circuits. In recent years the fault-tolerance properties of QCA circuits has been demonstrated by many researchers [13–17].

As already mentioned, the basic building block of QCA circuit is majority gate; majority logic is a way of implementing digital operations in a manner different from that of Boolean logic. The logic process of majority logic is more sophisticated than that of Boolean logic; consequently, majority logic is more powerful for implementing a given digital function with a smaller number of logic gates [18, 19].

This paper investigates a new design for fault-tolerant majority gate. By applying this new proposed scheme for fault-tolerant majority gate, we can obtain high degree of robustness in terms of misalignment, missing, and dislocation cells. The presented method is justified based on physical proofs as well as simulation results. In comparison to other existing implementations, this majority gate demonstrates significant improvement in terms of area, complexity, and robustness.

One of the most important component in any arithmetic and digital circuits in QCA and VLSI is full adder [4–7, 20–24]. A fault-tolerant QCA full adder can be implemented using the new fault-tolerant majority gate. Improving the

robustness of the majority gate cells leads to efficient designing of many arithmetic circuits.

2. Materials and Methods

2.1. Background. Quantum cellular automata is a new device architecture, which is proposed by Lent and Tougaw [25]. A quantum cell can be viewed as a set of four charge containers or dots, positioned at the corner of a square. The cell contains two extra mobile electrons, which can quantum mechanically tunnel between dots but not cells. The electrons are forced to the corner positions by Columbic repulsion. This two possible polarization states represent logic “0” and “1,” as shown in Figure 1(a) [2].

As shown in Figure 1(b), an ordinary QCA gate implementing the majority function is as follows: assuming three inputs labeled A, B, and C, the logic function of majority gate is $M(A, B, C) = AB + AC + BC$. As illustrated in Figure 1(b) each QCA majority gate requires only five cells. In Figure 1(c) a QCA inverter is shown which simply returns the opposite value that was put in.

2.2. Faults of QCA Circuits. Three major categories of faults can occur during the assembly of a QCA circuit. First, faults may occur when quantum cells are shifted from their intended locations which are called “misalignment” cells. Sometimes misalignment cells have no effect on functionality of a QCA circuit, and also sometimes a misalignment cell may have a polarity opposite what it should. A second type of faults occurs when the quantum cell itself is “missing” resulting in the cell becoming defective. If the gap between ideal cells is large enough, it would have no influence on its neighbors and it can cause a circuit to cease functioning well. A third type of faults occurs when quantum cells are rotated relative to the other cells in the array which is called “dislocation” cells. Also, in this case, the circuit may cease to function (Figure 2).

Based on the researches which have been performed to date, some fault-tolerant QCA circuits have been designed and tested [14–16]. But, these circuits are not robust enough to operate correctly when faced with faults. In next section, we have attempted to make a novel fault-tolerant majority gate using physical relation, in such a manner that it can continue to operate correctly in the event of the above-mentioned faults.

2.3. Novel Design for Fault-Tolerant Majority Gate. Majority is a voter. In our new structure, a fault-tolerant majority gate can be implemented as shown in Figure 3. In this scheme we have three inputs labeled A, B, and C and the output cell is shown by *out*. In addition there are nine middle cells labeled 1, 2, 3, 4, 5, 6, 7, 8, and 9. Polarization of input cells is fixed and middle cells and output cell are free to change.

As it is clear in Figure 3, a new fault-tolerant majority gate only needs 13 cells and by considering some physical relations it is implemented.

Regarding the physical proofs, assume that all cells are similar and the length of each one is a ($a = 18$ nm) and there is a space of x ($x = 2$ nm) between each two neighbors.

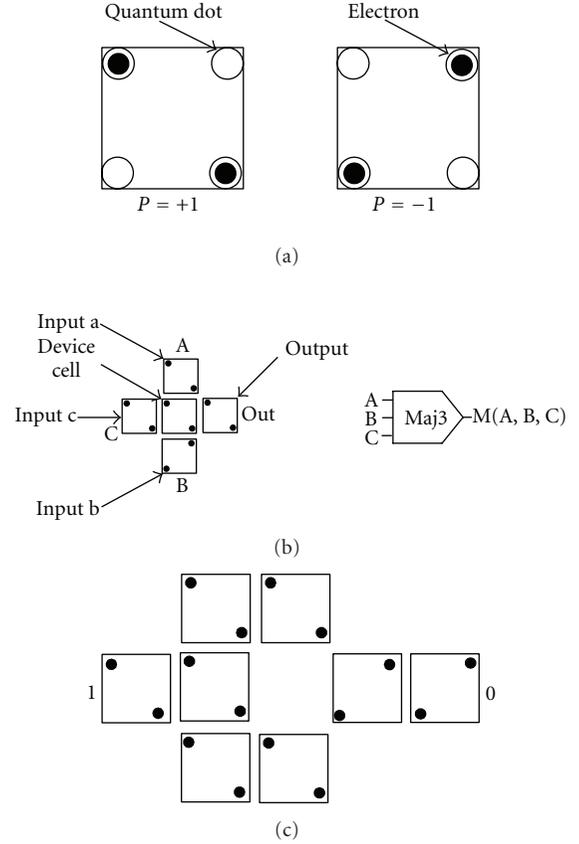


FIGURE 1: (a) Basic QCA cell and binary encoding, (b) a QCA majority gate, (c) a QCA inverter.

In all figures, rectangles show a QCA cell and the circles inside show the electrons within that cell. It should be noted that in order to achieve more stability, electrons of QCA cell are arranged in such a manner that reaches minimum kink energy.

The kink energy between two electron charges is calculated using (1a). In this equation, U is kink energy, k is fixed colon, q_1 and q_2 are electric charges, and r is the distance between two electric charges. By putting the values of k and q , we obtain (1b). U_T is the summation of kink energies that is calculated from (2) [4, 26–28]

$$U \frac{kq_1q_2}{r}, \quad (1a)$$

$$\begin{aligned} kq_1q_2 &= 9 * 10^9 * (1.6)^2 * 10^{-38} \\ &= 23.04 * 10^{-29} = A = cte, \end{aligned} \quad (1b)$$

$$U_T = \sum_{i=1}^2 U_i. \quad (2)$$

2.4. Physical Proof. The proposed fault-tolerant majority gate has nine different middle cells, so we should check all the faults that may occur in middle cells to verify the correctness of this scheme. Here, only one of the faults (missing cell 5)

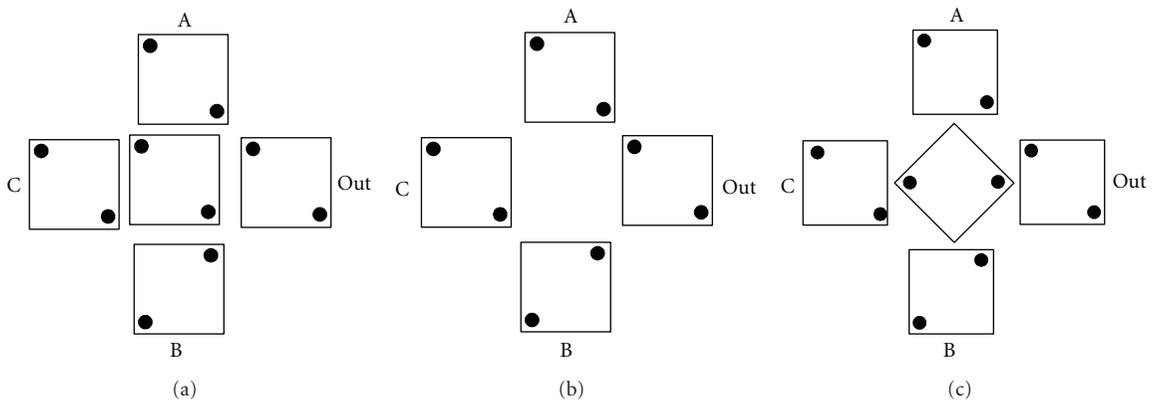


FIGURE 2: Faults of majority gate, (a) misalignment cell, (b) missing cell, and (c) dislocation cell.

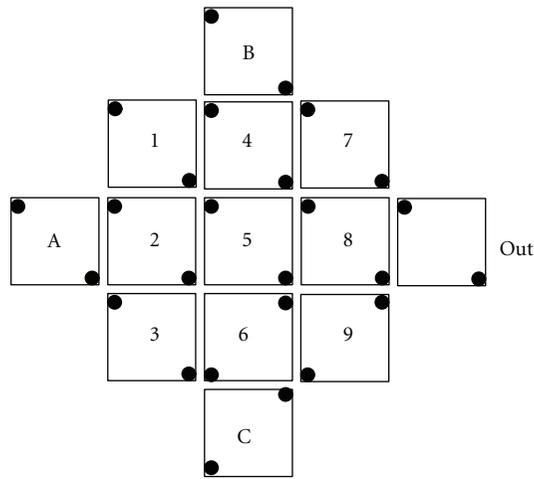


FIGURE 3: Proposed fault-tolerant majority gate.

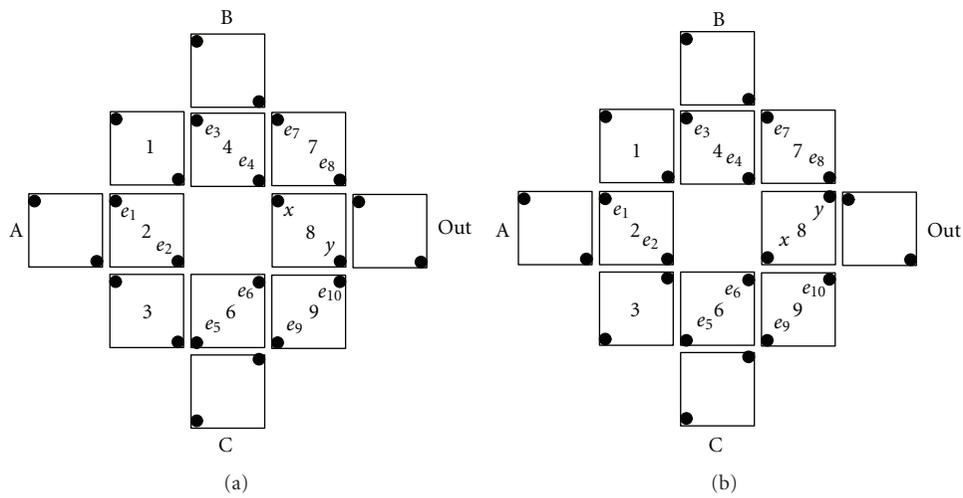


FIGURE 4: (a) The one value in cell 8, (b) the zero value in cell 8.

is proved and the others can be proved as well. The assumed value of input cells are $A = B = 1, C = 0$.

First, we calculate the kink energy existing between each electron ($e_1, e_2, e_3, e_4, e_5, e_6, e_7, e_8, e_9$, and e_{10}) with electrons “ x ” and “ y ” in (a) and (b) states using (1a) and (1b) equations. For example, U_i is the kink energy existing between electrons e_i and x (or y). Also, r_i is the distance between two electron charges. Then we calculate the total kink energy (U_T) in both states using (2). The comparison of total kink energies in both (a) and (b) states shows which state (a or b) is more stable. We consider the state that has the lower kink energy level as the more suitable one.

As the proof method is similar for all cells and their values and also due to lack of space, only the first part of this proof is stated and the rest of relations are omitted (Figure 4).

Figure 4(a) (Electron x)

$$\begin{aligned}
 U_1 &= \frac{A}{r_1} = \frac{23.04 * 10^{-29}}{40 * 10^{-9}} \approx 0.58 * 10^{-20}(J), \\
 U_2 &= \frac{A}{r_2} = \frac{23.04 * 10^{-29}}{28.42 * 10^{-9}} \approx 0.81 * 10^{-20}(J), \\
 U_3 &= \frac{A}{r_3} = \frac{23.04 * 10^{-29}}{28.28 * 10^{-9}} \approx 0.81 * 10^{-20}(J), \\
 U_4 &= \frac{A}{r_4} = \frac{23.04 * 10^{-29}}{2.83 * 10^{-9}} \approx 8.14 * 10^{-20}(J), \\
 U_5 &= \frac{A}{r_5} = \frac{23.04 * 10^{-29}}{42.94 * 10^{-9}} \approx 0.54 * 10^{-20}(J), \\
 U_6 &= \frac{A}{r_6} = \frac{23.04 * 10^{-29}}{20.1 * 10^{-9}} \approx 1.15 * 10^{-20}(J), \\
 U_7 &= \frac{A}{r_7} = \frac{23.04 * 10^{-29}}{20 * 10^{-9}} \approx 1.15 * 10^{-20}(J), \\
 U_8 &= \frac{A}{r_8} = \frac{23.04 * 10^{-29}}{18.11 * 10^{-9}} \approx 1.27 * 10^{-20}(J), \\
 U_9 &= \frac{A}{r_9} = \frac{23.04 * 10^{-29}}{38 * 10^{-9}} \approx 0.61 * 10^{-20}(J), \\
 U_{10} &= \frac{A}{r_{10}} = \frac{23.04 * 10^{-29}}{26.91 * 10^{-9}} \approx 0.86 * 10^{-20}(J), \\
 U_{T_{11}} &= \sum_{i=1}^{10} U_i = 15.92 * 10^{-20}(J), \\
 U_{T_1} &= \sum_{i=1}^2 U_{1i} = 36.36 * 10^{-20}(J).
 \end{aligned} \tag{3}$$

Figure 4(a) (Electron y)

$$\begin{aligned}
 U_1 &= \frac{A}{r_1} = \frac{23.04 * 10^{-29}}{43.86 * 10^{-9}} \approx 0.52 * 10^{-20}(J), \\
 U_2 &= \frac{A}{r_2} = \frac{23.04 * 10^{-29}}{40 * 10^{-9}} \approx 0.58 * 10^{-20}(J),
 \end{aligned}$$

$$U_3 = \frac{A}{r_3} = \frac{23.04 * 10^{-29}}{53.74 * 10^{-9}} \approx 0.43 * 10^{-20}(J),$$

$$U_4 = \frac{A}{r_4} = \frac{23.04 * 10^{-29}}{28.28 * 10^{-9}} \approx 0.81 * 10^{-20}(J),$$

$$U_5 = \frac{A}{r_5} = \frac{23.04 * 10^{-29}}{42.94 * 10^{-9}} \approx 0.54 * 10^{-20}(J),$$

$$U_6 = \frac{A}{r_6} = \frac{23.04 * 10^{-29}}{6.63 * 10^{-9}} \approx 3.48 * 10^{-20}(J),$$

$$U_7 = \frac{A}{r_7} = \frac{23.04 * 10^{-29}}{42.05 * 10^{-9}} \approx 0.55 * 10^{-20}(J),$$

$$U_8 = \frac{A}{r_8} = \frac{23.04 * 10^{-29}}{20 * 10^{-9}} \approx 1.15 * 10^{-20}(J),$$

$$U_9 = \frac{A}{r_9} = \frac{23.04 * 10^{-29}}{26.91 * 10^{-9}} \approx 0.86 * 10^{-20}(J),$$

$$U_{10} = \frac{A}{r_{10}} = \frac{23.04 * 10^{-29}}{2 * 10^{-9}} \approx 11.52 * 10^{-20}(J),$$

$$U_{T_{12}} = \sum_{i=1}^{10} U_i = 20.44 * 10^{-20}(J).$$

(4)

Since cells 1 and 3 are roughly in a long distance from cell 8, their kink energy can be neglected. It should be noted that the value of cell 8 is transferred to the output cell, which give us a majority decision of inputs A, B, and C.

Figure 4(b) (Electron x)

$$U_{T_{21}} = \sum_{i=1}^{10} U_i = 18.1 * 10^{-20}(J),$$

(5)

$$U_{T_2} = \sum_{i=1}^2 U_{2i} = 40.03 * 10^{-20}(J).$$

Figure 4(b) (Electron y)

$$U_{T_{22}} = \sum_{i=1}^{10} U_i = 21.93 * 10^{-20}(J). \tag{6}$$

With comparison of the achieved results, the electrons in cell 8 are positioned in state (a) which is more stable and has a lower kink energy. It is worth mentioning that in all cells U_{T_1} is the kink energy in +1 polarization and U_{T_2} is the kink energy in -1 polarization.

Considering the above computing, we can infer that the proposed structure for implementing a fault-tolerant majority gate is completely correct and resulted in a correct state for the output cell when faults occur.

After physical proof, we can also check the proposed design using QCADesigner. The next section presents the simulation results of this fault-tolerant majority gate.

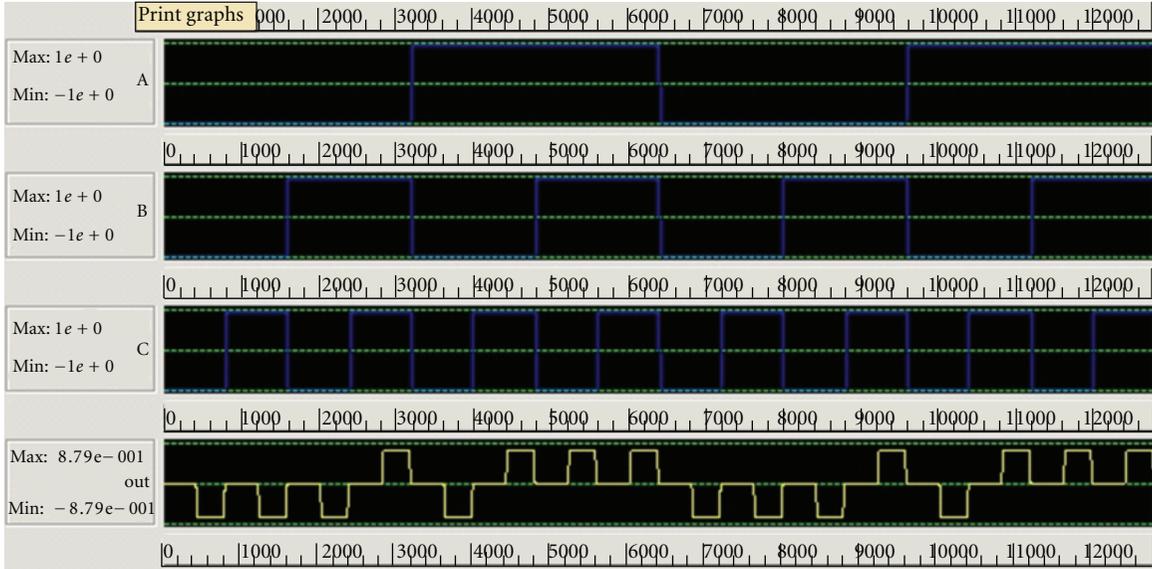


FIGURE 5: Simulation results for proposed fault-tolerant majority gate with faults.

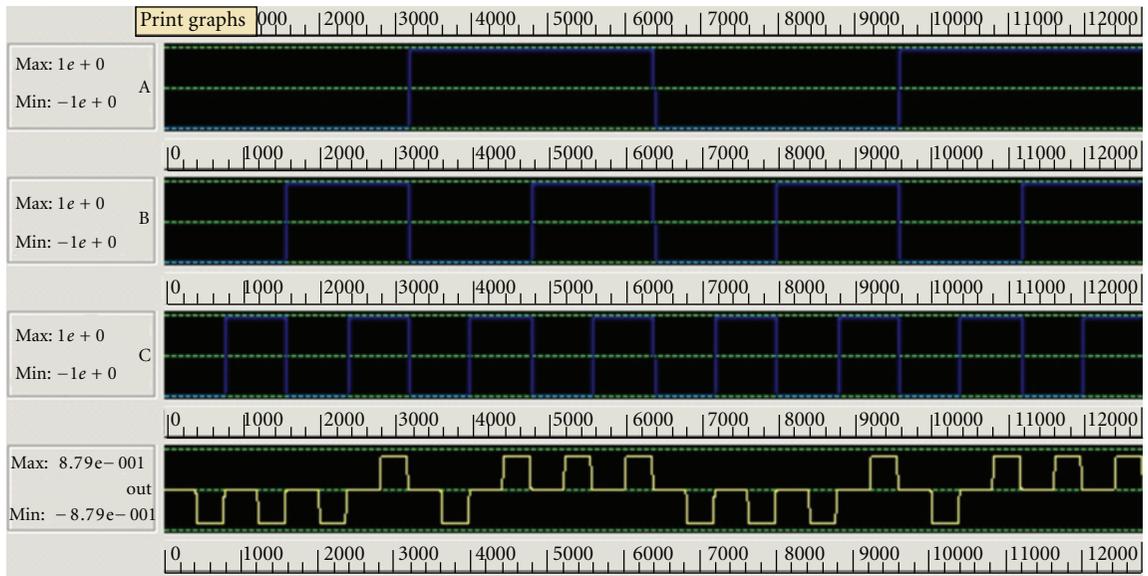


FIGURE 6: Simulation results for proposed fault-tolerant majority gate without faults.

3. Simulation Results

For the proposed circuit layout and functionality check, a simulation tool for QCA circuits, QCADesigner version 2.0.3 [29], is used. The following parameters are used for a bistable approximation:

- (i) cell size = 18 nm,
- (ii) number of samples = 50000,
- (iii) convergence tolerance = 0.0000100,
- (iv) radius of effect = 65.000000 nm,
- (v) relative permittivity = 12.900000,
- (vi) clock high = $9.800000e-022$ J,

(vii) clock low = $3.800000e-023$ J,

(viii) clock shift = 0,

(ix) clock amplitude factor = 2.000000,

(x) layer separation = 11.500000,

(xi) maximum iterations per sample = 100.

Most of the above-mentioned parameters are default values in QCADesigner.

Figures 5 and 6 show the simulation results of proposed fault-tolerant majority gate with or without faults. These results are the same as the results of physical proof that was mentioned in previous section.

Simulation results reveal that the proposed majority gate is more robust than previous ones.

4. Conclusion

In this paper, we analyzed fault-tolerance properties of the conventional design for majority gate as the based logic gate for implementing QCA circuits. High performance logic component can be achieved by utilizing this fault-tolerant majority gate. We analyzed robustness of proposed majority gate in terms of

- (i) misalignment cells,
- (ii) missing cells,
- (iii) dislocation cells.

Some physical proofs and exhaustive simulation using QCADesigner tool have verified the functionality of this scheme. The presented structure demonstrates significant improvements in terms of area, complexity, and robustness in comparison to previous designs.

Acknowledgment

The authors would like to thank Dr. Belmont Yoberd for his literature contribution.

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