Hindawi
Journal of Nanotechnology
Volume 2017, Article ID 4575013, 9 pages
https://doi.org/10.1155/2017/4575013

Research Article

Comparative Analysis of 6T, 7T, 8T, 9T, and 10T Realistic CNTFET Based SRAM

Shital Joshi[1] and Umar Alabawi[2]

[1]*Department of Computer Science and Engineering, Oakland University, Rochester, MI, USA*
[2]*Department of Computer Science, University of Tabuk, Tabuk, Saudi Arabia*

Correspondence should be addressed to Shital Joshi; j.shital84@gmail.com

Received 4 January 2017; Accepted 16 February 2017; Published 15 March 2017

Academic Editor: Hongmei Luo

CMOS technology below 10 nm faces fundamental limits which restricts its applicability for future electronic application mainly in terms of size, power consumption, and speed. In digital electronics, memory components play a very significant role. SRAM, due to its unique ability to retain data, is one of the most popular memory elements used in most of the digital devices. With aggressive technology scaling, the design of SRAM is seriously challenged in terms of delay, noise margin, and stability. This paper compares the performance of various CNTFET based SRAM cell topologies like 6T, 7T, 8T, 9T, and 10T cell with respect to static noise margin (SNM), write margin (WM), read delay, and power consumption. To consider the nonidealities of CNTFET, variations in tube diameter and effect of metallic tubes are considered for various structures with respect to various performance metrics like SNM, WM, read delay, and power consumption.

1. Introduction

Until recently, silicon based field effect transistors (FETs) were considered as ubiquitous device material for semiconductor industries. However as the transistor size gets scaled down to nanometer regime, silicon based transistors possess lots of problems like high power consumption in idle state due to large leakage, gate losing control of channel, difficulty in choosing suitable oxide material, inability to shrink oxide thickness accordingly, and various other short channel effects (SCEs). Particularly, below 10 nm, complementary metal oxide semiconductor (CMOS) has hit the power wall, that is, nonscaling of KT/q and hence nonscalability of V_{th} and V_{DD}. Furthermore, at those technology nodes, crystalline silicon breaks down into amorphous silicon making them infeasible to be used as a suitable material for future electronics. Thus to make future electronic devices smaller, smarter, and computationally efficient, it has become very important to opt for alternative device materials or alternative device concepts. As a result, various alternate building materials like FinFETs, graphene FET (GFET) [1–3], graphene nanoribbon FET (GNRFET), carbon nanotube (CNT) [4, 5], and Si-nanowire FET have been extensively studied as a future replacement for CMOS technology. Carbon nanotube has been considered in this paper due to its extremely low feature size (around 2 nm), high performance in terms of speed, and power consumption.

Carbon nanotubes are hallow seamless cylinders formed by rolling graphite sheet. Depending on the rolling pattern of the graphite sheet, CNTs exhibit both metallic and semiconductor property. Hence it is possible to make all CNT based electronic devices using metallic CNT as an interconnecting wire and semiconductive CNTs as the transistor. One of the most important aspect of CNT is its one-dimensional structure and the existence of strong quantization of electron and hole state in only 1D subband. This reduces the back scattering and results in increased conductivity (i.e., large current carrying capacity even at low applied voltage) and better control of transistor during off-state (and hence low leakage current). It is also able to utilize ballistic transport

(i.e., the mean free path is longer than the path) which reduces carrier charge collision and offers negligible resistance. Hence the transistor can achieve a speed in the range of terahertz. Some other properties exhibited by CNTFET are high-k compatibility, stability, low power consumption, and SCE even below 10 nm. These make CNT one of the strong candidates for future electronics.

Static random access memory (SRAM) is one of the most important building blocks in digital circuits which occupies about 90% of the modern chip area. With the technology as well as supply voltage shrinking down, it has become extremely challenging to design SRAM due to less noise margin and hence poor stability. So with scaled technology, it is very difficult to meet three constraints of SRAM: area, power consumption, and stability. Therefore, scaling in SRAM size has not significantly reduced as compared to other chip components. To consider the possibility of using CNTFET for SRAM, in [6, 7] the authors have compared CNTFET and MOSFET SRAM cell. In [8], the authors have considered different topologies of CNTFET based SRAM but have not considered the effect of CNT imperfection in the SRAM performance. Authors in [9] have considered the effect of diameter variations and metallic tubes on the performance of 6T based SRAM cell. In [10], the authors have compared graphene nanoribbon field effect transistor (GNRFET) based SRAM with silicon FET based SRAM and showed the power consumption of GNRFET with respect to silicon based SRAM. In [11], the authors have considered the effect of metallic CNT on the read and write delay. However they have completely ignored the effects on power and the noise margin. Similarly, in [12], the authors have considered the metallic tolerant 6T CNT for a low power design. However the noise margin, delay aspect, and also the effect of diameter for other possible SRAM structures had not been performed. So this paper analyzes CNTFET based SRAM for various topologies like 6T, 7T, 8T, 9T, and 10T considering some technological difficulties in the manufacturing of CNTFET such as metallic CNTs, variation in doping, variation in tube diameter, and variations in densities of tubes. This paper considers the effect of these variations in the static noise margin (SNM), delay, write margin, and power consumption.

The rest of the paper is organized as follows: Section 2 highlights the novel contributions of this paper. Section 3 considers the design of CNTFET based SRAM cell design for various topologies. In Section 4 various topologies of CNTFET based SRAM are compared with the corresponding topologies of SRAM cell. The effects of synthesis imperfection of CNTFETs on various SRAM topologies are considered in Section 5 and also the effects of process variations on these topologies are analyzed. Finally the conclusion and future research prospective are given in Section 6.

2. Novel Contributions of This Paper

To the best of the authors' knowledge, this is the first attempt to perform comparative analysis on various topologies of CNTFET based SRAM. All previous attempts either considered comparison of stability of ideal SRAM structures or considered comparison of process variations with just one structure. Hence the main contributions of this paper are summarized as follows:

(1) Design and comparative analysis of 6T, 7T, 8T, 9T, and 10T SRAM cell structure with respect to SNM, write margin (WM), delay, and power consumption

(2) Impact of process imperfections like presence of metallic CNT on the performance of these SRAM structures in terms of delay, power, and noise margin

(3) Effect of process variations like variations in the tube diameter on the performance of these SRAM structures

3. CNTFET Based SRAM

3.1. CNTFET Structure. The CNTFET uses carbon nanotube or an array of carbon nanotubes as a channel material serving as a bridge for the carrier movement between the source and the drain. The voltage at the gate terminal is used to control the carrier movement turning it either on or off. Unlike CMOS technology, CNTFET can exhibit either ambipolar behavior or a unipolar behavior depending upon its structure, that is, whether it is Schottky Barrier (SB) FET or MOSFET-like FET. For the complementary logic design, it is preferred to have MOSFET-like CNTFETs.

CNTFET technology faces several challenges resulting from the process variation. These variations can lead the circuit failure if not considered carefully. Even though CNTs are less sensitive to CMOS process variations like oxide thickness, channel length, channel width, and doping concentration, they are very sensitive to CNT specific variations like CNT doping, chirality, diameter, density, and CNT alignment [13, 14]. These variations can make circuit behave in a significantly different manner if not considered during the design phase. Almost all the important design constraints like delays, noise margin, leakage current, and stability are affected by these variations. So this paper analyzes the performance of SRAM with respect to these variations for different topologies. For the purpose of analysis, this paper considers CNTFET model developed by Nanoelectronics Lab at Stanford University [15].

For the comparison of effect of different parameters on the performance of SRAM, it becomes necessary to investigate the optimum design parameters. This is important in order to understand the design parameters and for identifying important aspect of the technology while improving the circuit performance. Thus as a first step towards the design of SRAM, CNT based inverter has to been considered to analyze the device performance over change in the structural device parameters. The reason for choosing inverter makes sense due to the fact that SRAM consists of inverter pairs connected in the cross-coupled fashion, since the performance of the CNT based inverter varies with CNT diameter, number of carbon nanotubes used, internanotube spacing, oxide thickness, CNT pitch, supply voltage, and other parameters. However the experiment has been restricted to just CNT diameter and the number of CNTs, which are the main objective of this paper while analyzing SRAM performance and their effects on ON current, delays, and power consumption.

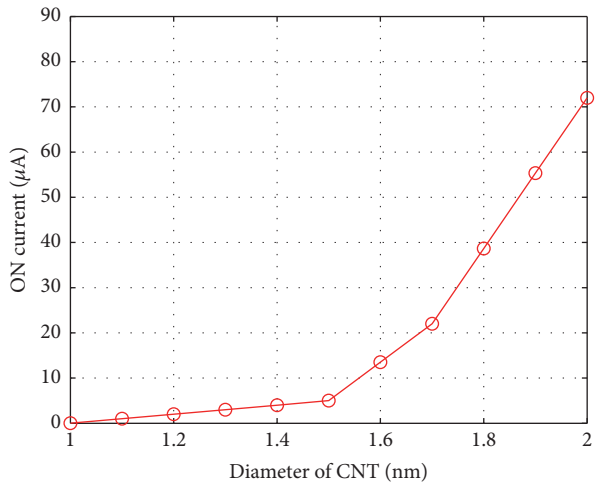


Figure 1: Effect of CNT diameter on the current.

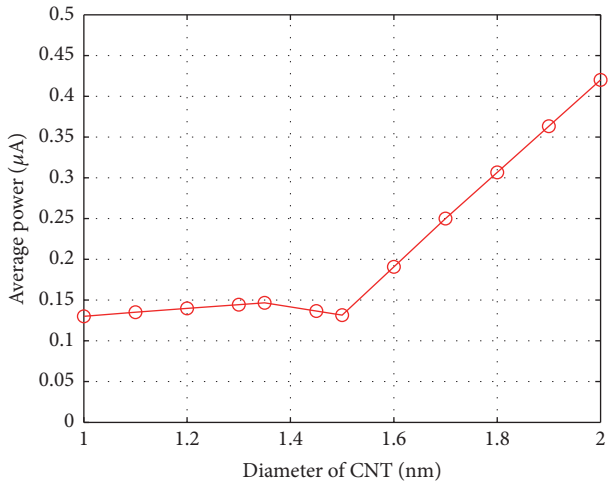


Figure 2: Effect of CNT diameter on the power consumption.

3.1.1. Effect of CNT Diameter. Diameter is one of the main parameters which affects the ON current in the CNTFET based circuits. As the CNT diameter is increased, it reduces the band gap and increases the transconductance proportionally. This results in the increment in the ON current as shown in Figure 1. The ON current in CNTFET is approximately given as [16]

$$I_{\text{CNTFET}} = \frac{N g_{\text{CNT}} \left(V_{\text{dd}} - V_{\text{th}}\right)}{1 + g_{\text{CNT}} L_s \rho_s}, \quad (1)$$

where N is the number of CNTs per device, g_{CNT} is the transconductance per CNT, V_{dd} is the supply voltage, V_{th} is the threshold voltage of the CNTFET, L_s is the source length, and ρ_s is the source resistance per unit length of doped CNT.

With the increment in the CNT diameter, CNT becomes more conducting and hence it deteriorates the power handling capability. This subsequently increases the power consumption as shown in Figure 2. This becomes very important in the design of digital circuits where the ratio of ON and OFF current should be very large so as to turn the device fast and to control the leakage current.

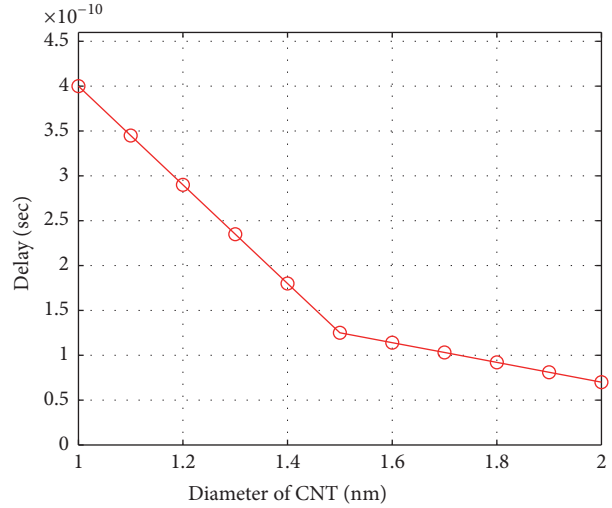


Figure 3: Effect of CNT diameter on the delay.

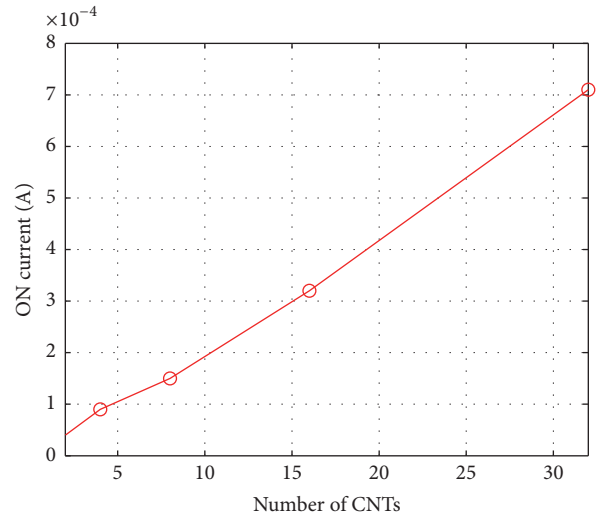


Figure 4: Effect of CNT number on the ON current.

With the increase in the ON current, the device is able to turn faster and hence the delays are reduced in the circuit as shown in Figure 3.

3.1.2. Effect of Number of CNTs. Though a transistor can be designed with a single nanotube, it is however not competitive in terms of performance with respect to the traditional MOSFET. So it becomes necessary to use multiple tube in the design of CNT based circuit. The next critical question would be to select the appropriate number of nanotubes. As can be seen from (1), the ON current in CNTFET depends directly on the number of CNTs per device as shown in Figure 4.

Similarly, the effect of increasing the number of CNTs also incurs increase in the power consumption as shown in Figure 5 as the same reason mentioned above.

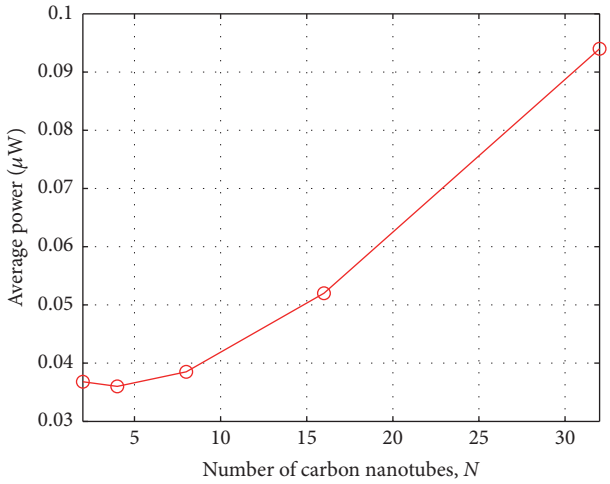


Figure 5: Effect of CNT number on the power consumption.

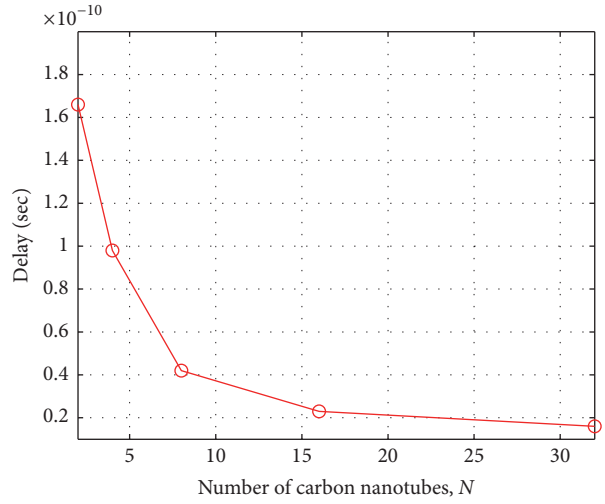


Figure 6: Effect of CNT number on the delay.

Same as the reason for CNT diameter, with the increase in the number of CNTs, the delay of the circuit decreases as shown in Figure 6.

From the results obtained in Sections 3.1.1 and 3.1.2, an appropriate value for CNTFET transistor is chosen to perform analysis for SRAM and is given in Table 1.

3.2. SRAM Cell. SRAM is a type of semiconductor memory which has the ability to retain data as long as the power is turned on. While designing SRAM there are four important design criteria: access time, density, noise margin, and power consumption. It is very difficult to simultaneously achieve all of these constraints at the same time. So depending on the application, the design needs to be focused to optimize one or more of these design constraints. Similarly, there are several SRAM structures depending upon what is of utmost importance for the application. This subsection briefly highlights several such structures and Table 2 shows the values of CNT size used for various of these topologies.

Table 1: Nominal CNTFET parameters used for HSPICE simulation [8].

Device parameters	Default values
The thickness of high-k top gate dielectric material (T_{ox})	4 nm
Gate dielectric constant	16
Interconnect capacitance	0.22 fF/μm
Physical channel length ($L_{channel}$)	32 nm
Fermi level of doped CNT source/drain extension region (L_{sd})	32 nm
Fermi level of the doped S/D tube (Efo)	0.6 eV
Chirality of tube (m, n)	(19, 0)
CNT pitch	10 nm
Flatband voltage for n-CNTFET and p-CNTFET (V_{fbn} and V_{fbp})	0 eV and 0 eV
Mean free path in intrinsic CNT (L_{ceff})	200 nm
Mean free path in p+/n+ doped CNT	15 nm
Work function of source/drain metal contact	4.6 eV
CNT work function	4.5 veV

Table 2: Sizing of a CNTFET used for the various SRAM topologies [8].

Transistor	Number of tubes
For 6T CNTFET based SRAM cell	
$M1$, $M2$, $M3$, and $M4$ transistors	3 tubes
$M5$ and $M6$ transistors	5 tubes
For 7T CNTFET based SRAM cell	
$M1$, $M2$, and $M5$ transistors	3 tubes
$M4$ and $M7$ transistors	1 tube
$M3$ transistor	8 tubes
$M6$ transistor	6 tubes
For 8T CNTFET based SRAM cell	
$L1$, $L2$, and $E1$ transistors	1 tube
$D1$ and $D2$ transistors	4 tubes
$A1$, $A2$, and $E3$ transistors	6 tubes
For 9T CNTFET based SRAM cell	
$E1$, $E3$, $E4$, and $A2$ transistors	4 tubes
$E2$ Transistor	7 tubes
For 10T CNTFET based SRAM cell	
$AL1$, $AL2$, $AR1$, and $AR2$ transistors	2 tubes
$L1$ and $L2$ transistors	3 tubes
$D1$ and $D2$ transistors	5 tubes
NR and NL transistors	8 tubes

These numbers of CNTs per transistor are chosen to optimize SRAM cells performance and functionality. It is however important to note the significant difference between CMOS based SRAM and CNTFET based SRAM: (1) unlike CMOS devices, the source and drain terminal of CNTFET are not interchangeable and (2) Unlike in CMOS devices the mobility of electrons and holes are almost similar.

3.2.1. 6T CNTFET Based SRAM Cell. The structure of 6T SRAM cell is shown in Figure 7. In this structure, four transistors ($M1$–$M4$) form a pair of inverters which are used to store a bit of information while the remaining two

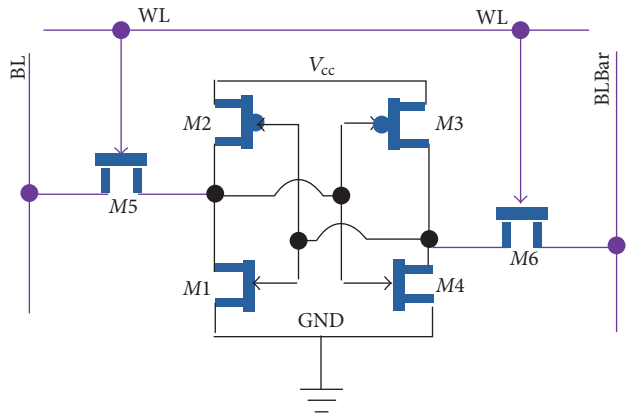


Figure 7: 6T SRAM structure.

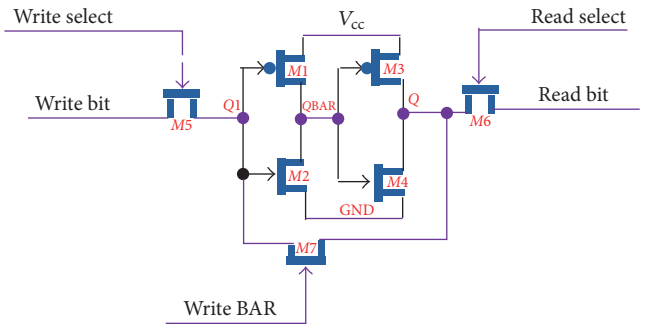


Figure 8: 7T SRAM structure.

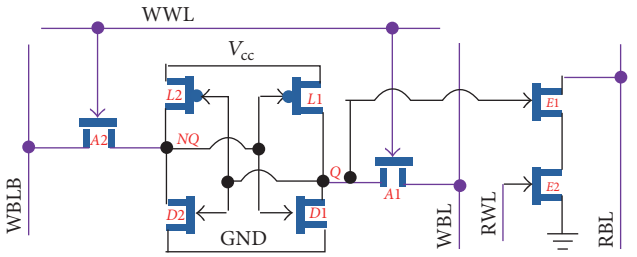


Figure 9: 8T SRAM structure.

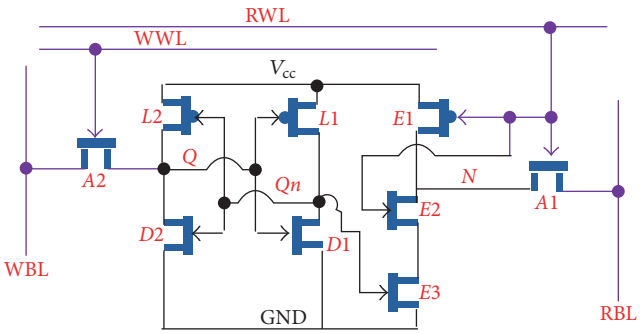


Figure 10: 9T SRAM structure.

transistors ($M5$ and $M6$) are called the access transistors which are used to access the inverter pair for read and write operation. These access transistors are controlled by the word line (WL) which thereby allows the two bit lines (BL and BLBar) to access the memory elements. Dual bit lines are chosen in this paper due to their better noise margin as compared to a single bit line.

3.2.2. 7T CNTFET Based SRAM Cell. To improve the read cycle and reduce static power, 7T SRAM cell is designed. An additional transistor $M7$ is used in the feedback structure to amplify high value on one inverter from low value at another inverter and vice versa. Two separate transistors ($M5$ and $M6$) are used to write and read from the memory cell using WRITE SELECT and READ SELECT signal, respectively. Transistor $M7$ is turned on during the read operation and is turned off during the write operation. The read cycle is improved by sizing the transistors $M6$ and $M7$ such that the read bit line can be charged faster. The structure of 7T SRAM cell is shown in Figure 8.

3.2.3. 8T CNTFET Based SRAM Cell. The 8T SRAM cell structure is shown in Figure 9, which is similar to 6T structure but with additional transistors to isolate the internal inverter from accidental write during the read cycle. Before read cycle, the read bit line (RBL) is precharged to the supply voltage. Then the read operation starts by asserting RWL, where RBL can remain either at logic "1" state or logic "0" state depending upon whether internal node Q is 0 or 1, respectively. Write cycle is similar to the 6T cell.

3.2.4. 9T CNTFET Based SRAM Cell. One bit of information is stored in the internal inverters which are formed by $L1$ and $D1$ and $L2$ and $D2$ pair as shown in Figure 10. For writing into the cell, write bit line (WBL) and the pass transistor $A2$ are used while for reading the read bit line (RBL) and transistors $E1$, $E2$, and $E3$ are used. The data stability is significantly improved in the read operation with this structure.

3.2.5. 10T CNTFET Based SRAM Cell. The noise margin for both read and write operation is significantly improved with 10T structure as shown in Figure 11. In the read mode, line WL is enabled while WWL is disabled which decouples internal data nodes Q and Q_B from the bit lines. This improves the read SNM. In the write mode, both WL and WWL are enabled to transfer data into the cell from the bit lines. Due to series access transistors ($AL1$, $AL2$ and $AR1$, $AR2$) in 10T structure, the write ability can be an issue.

4. SRAM Characteristics

As shown in Table 3, 8T, 9T, and 10T SRAM structures show more than 50% higher read SNM (RSNM) as compared to 6T SRAM structure whereas 7T SRAM structure shows no significant improvement in RSNM. In case of write SNM (WSNM), 9T structure shows the least value among all structures. 7T and 8T SRAM structure shows around 10% improvement with respect to 6T SRAM structure while 10T structure shows more than 30% improvement over 6T

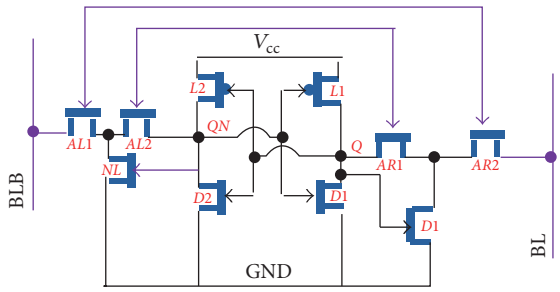


Figure 11: 10T SRAM structure.

Table 3: Characteristics of CNTFET based SRAM [8].

SRAM structure	SNM (μV)	WM (μV)	Dynamic power (nW)	Read delay (nSec)
6T SRAM	202	340	10.054	5.9
7T SRAM	223	360	4.87	3.6
8T SRAM	397	379	12.458	6.5
9T SRAM	410	330	16.548	7.6
10T SRAM	432	475	17.58	8.0

structure. The dynamic power consumption of 7T SRAM structure is minimum at 4.87 nW and is 36% less than 6T structure. For 8T, 9T, and 10T structure, the dynamic power is increased by around 36%, 67%, and 75% as compared to 6T structure. Similarly the read delay for 7T structure is the least, which is at 3.54 psec which increased by around 68%, 73%, 74%, and 76% in 6T, 8T, 9T, and 10T, respectively, as compared to 7T structure.

It has been observed that 7T SRAM structure has the least dynamic power consumption as well as the read delay as compared to other structures. In order to analyze the reason for that, analyzing its structure in a bit detail is needed. The 4 transistors ($M1$, $M2$ and $M3$, $M4$) in the center forms two cross-couple inverters INV1 and INV2. Due to the feedback structures, a low input value in the first inverter INV1 generates high value for the second inverter INV2 and a low input value on the second inverter INV2 generates high input value for the first inverter INV1. This structure is common for all the SRAM structure considered in this paper. The advantage comes with the extra n-type transistor $M7$ that is connected in the feedback path between the output of the INV2 and the input of the INV1, which performs the feedback connection and disconnection during read and write operation, respectively. During the write operation, $M7$ is off thereby disconnecting the feedback connection. This allows for a fast transfer of logic value from the write bit line "WRITE BIT" into the memory cell, where transistor $M5$ is turned on by the WRITE SELECT. Transistor $M6$ is kept off during this cycle. This reduces the dynamic power due to reducing switching activity during the memory access. The improvement in read delay is due to the following reasons:

(1) The WRITE BIT line does not need to be precharged for the preparation of the read operation.

(2) It is only necessary to precharge READ BIT line irrespective of the activity in the WRITE BIT line.

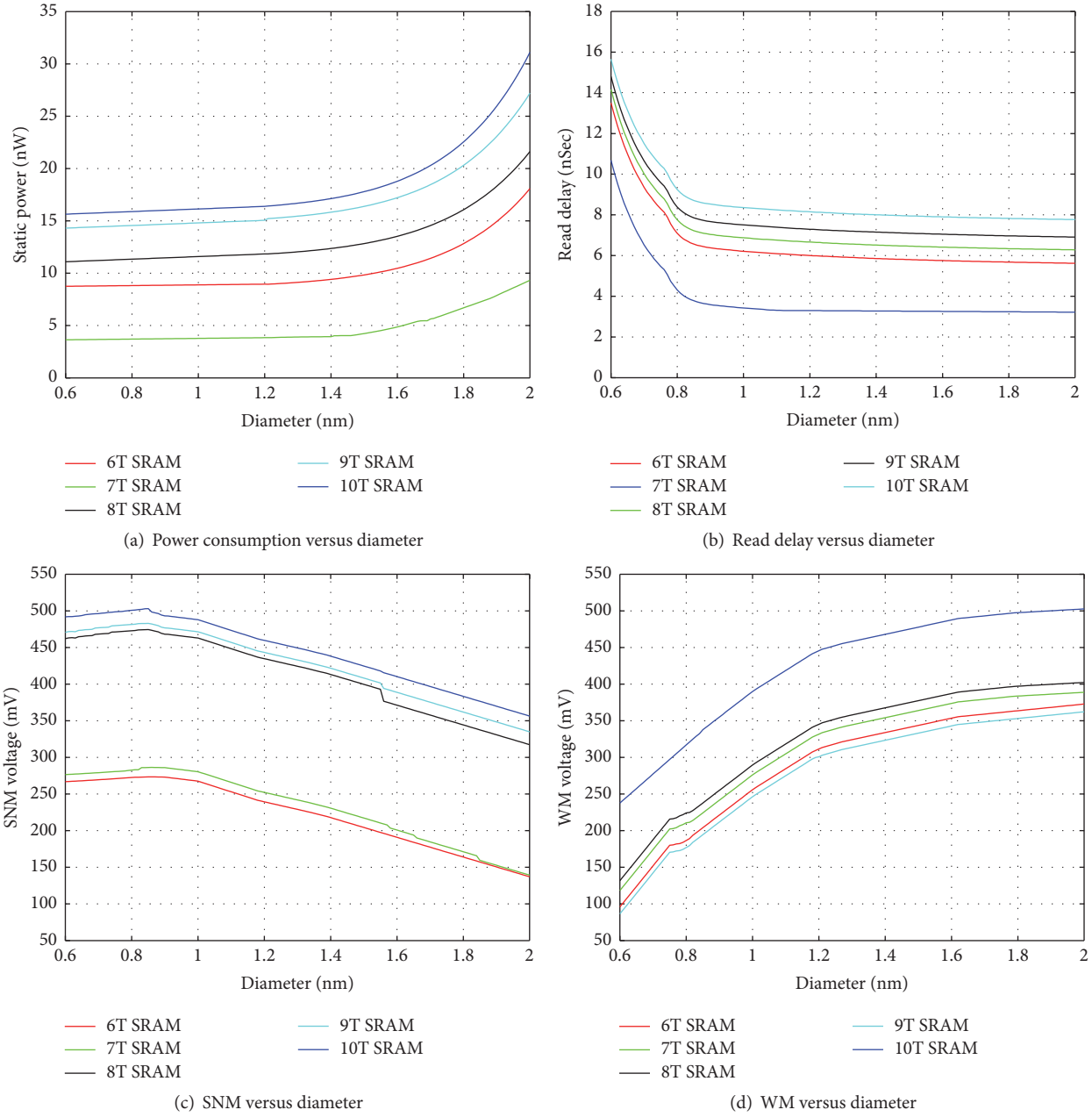
(3) The device sizing of the read zero path with the pull-down transistor $M3$ is made larger than $M6$ in order to provide a fast path to the ground.

5. Effects of CNT Imperfection on SRAM Characteristics

With the technology scaling down to nanometer regime, it becomes extremely challenging to have a precise control of the fabrication process. Thus, the process variation is bound to happen in several transistor fabrication steps. As well as with CMOS based circuits, the performance of CNTFET based circuits also shows performance variations due to the effects of process variations. Some of the most dominant sources of performance variation in CNTFETS are misaligned CNTs due to limited control over growth of CNTs, metallic CNTs, variation in doping, variation in tube diameter, variations in densities of tubes. Manufacturing variations in the doping, tube diameters, and densities of tubes all can influence delay, noise margin, and improper function of the logic circuits. So when the effects of these variations are considered in the CNTFETs based circuits, the final circuit performance will behave in a significantly different way compared to what is predicted from the ideal case. Hence it is important to determine the effect of each of these variations in the performance of SRAM. In this paper, the effect of CNT tube diameter and metallic nature of the tube have been considered. The effects of other variations are left as a part for the future work.

5.1. Effects of Tube Diameter Variation on SRAM Characteristics. The electronic properties of CNT are directly dependent on its physical characteristics. As the diameter of CNT increases, the energy band gap of the CNT decreases due to the inverse nature of relationship between them [14]. Hence the amount of electric current also varies accordingly with the tube diameter. This variation in current can cause variations in noise margin, read delays, and power consumption in the SRAM. When more than one CNT per transistor is considered then it increases the current driving capability of the circuit at the cost of increased area.

A power supply voltage of 0.9 V is used for the simulation in accordance with the ITRS roadmap for 32 nm technology. Since the static power is directly proportional to the threshold voltage in an exponential manner so any increase in the diameter variation causes increase in the static power consumption. Figure 12 shows the effect of CNT tube diameter on the performance of various SRAM structures in terms of power consumption, read delay, SNM, and write margin. As shown in Figure 12(a), static power increases very slightly when the tube diameter is increased from 0.6 nm to 1.4 nm. However after that the increase in static power is significant. The same trend is seen for all SRAM structures. Figure 12(b) shows the variation of read delay with respect to the tube diameter. The result shows that there is a sharp fall in the delay up to a tube diameter of 0.8 nm and after which the delay is not significantly changed. As the tube diameter changes from 0.6 nm to 1.4 nm, the read delay decreases by 58.4%,



(a) Power consumption versus diameter

(b) Read delay versus diameter

(c) SNM versus diameter

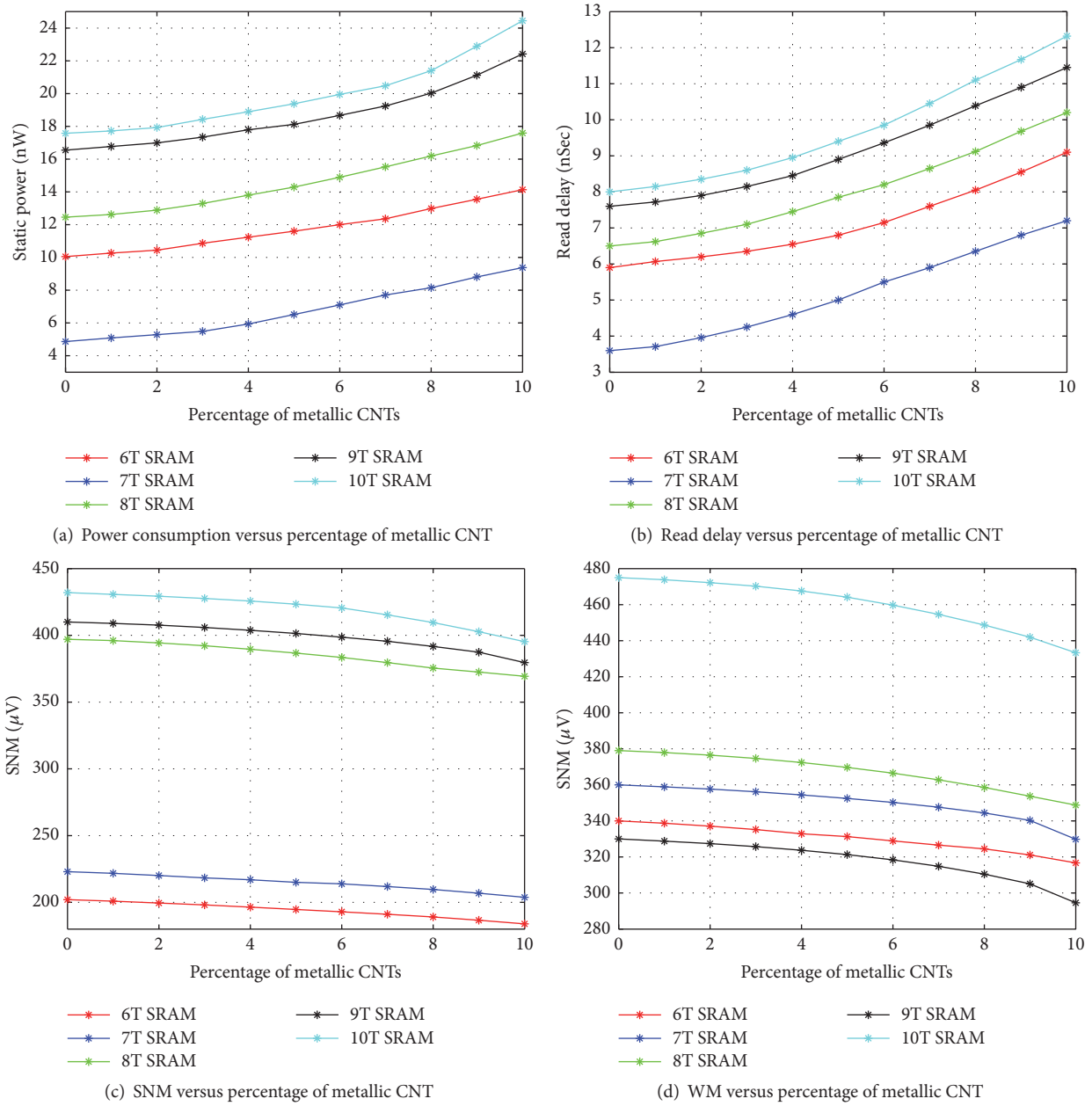
(d) WM versus diameter

Figure 12: Dependence of SRAM characteristics on the variation in the CNT diameter.

69.8%, 55.67%, 53.29%, and 50.38% for 6T, 7T, 8T, 9T, and 10T structure, respectively. Figure 12(c) shows an initial slight increase in SNM when the CNT diameter is increased from 0.6 nm to 0.8 nm. After 0.8 nm, SNM decreases linearly with increase in the tube diameter. In contrast Figure 12(d) shows that with the increase in the tube diameter the write margin in CNTFET based SRAM decreases. Hence as a designer, it becomes extremely necessary to select a suitable value of CNT tube diameter as it involves conflict between the SNM and WM which shows different nature with the tube diameter.

5.2. Effects of Metallic Tubes on SRAM Characteristics. CNTs exhibit metallic as well as semiconductor properties. Due to the random chirality, 1/3 of the synthesized CNTs possess metallic characters [17]. The presence of metallic CNTs results in the conducting channel which cannot be well controlled by the gate voltage. This causes short circuit between the drain and the source and results in excessive leakage current and hence high power consumption, delay, inferior noise performance, and even poor performance. For digital application semiconducting properties are required. However it is not possible to completely get rid of metallic tubes due to manufacturing challenges.

The effect of metallic tubes on CNTFET based SRAM cell has been considered on the HSPICE model based on [18]. The pitch (i.e., the center-to-center distance of CNT) has been



(a) Power consumption versus percentage of metallic CNT

(b) Read delay versus percentage of metallic CNT

(c) SNM versus percentage of metallic CNT

(d) WM versus percentage of metallic CNT

Figure 13: Dependence of SRAM characteristics on percentage of metallic CNT.

considered to be 6 nm with a dielectric thickness of 3 nm. The supply voltage has been chosen to be 0.9 V. With a chirality of (19, 0) for all the CNTs, the tube diameter of 1.5 nm and a threshold voltage of 0.289 V had been achieved. From [18], it has been assumed that the percentage of metallic CNT (p_m) satisfies a normal distribution with a probability density function of

$$\frac{1}{\sqrt{2\pi\sigma^2}}\exp^{(x-\mu)^2/(2\sigma^2)}. \quad (2)$$

The mean (μ) and the standard deviation (σ) have been considered as 0.102 and 0.0257, respectively. Each metallic tube has been modeled as a resistor where the effective resistance of each metallic tube is computed in the same way as that for the parallel resistors.

For the purpose of analysis of CNTFET based SRAM performance due to metallic CNT, it is considered that x% of CNTs are metallic, where x is varied from 0 to 10%. 10,000 samples are considered and Monte Carlo iterations are considered for each characteristic. The performance parameters considered for the SRAM are noise margin, read delays, and power consumption.

Figure 13 shows the effect of metallic tube on SRAM performance metrics. Figure 13(a) shows that the static power increases with the increase in the metallic tube. The result shows that the static power is increased by 54.2%, 100%, 57.8%, 50.7%, and 54% for 6T, 7T, 8T, 9T, and 10T structure,

respectively. Figure 13(b) shows that as the percentage of metallic tubes increases the read delay also increases due to decrease in the read current. As can be seen from the figure there is an increase of 40.6%, 92.61%, 41.2%, 35.5%, and 39.1% in the read delay for 6T, 7T, 8T, 9T, and 10T structure, respectively. Figures 13(c) and 13(d) show that with the increase in the metallic tubes both the SNM and WM decrease. In the case of SNM, the decrease is 8.96%, 8.6%, 6.98%, 7.4%, and 8.5% for 6T, 7T, 8T, 9T, and 10T, respectively, while WM decreases by 6.9%, 7.4%, 7.97%, 10.7%, and 8.78% as the percentage of metallic tube is increased from 0% to 10%, respectively.

6. Conclusions and Future Research

The results show that the performance of CNTFET based SRAM is manifold better than that of CMOS based SRAM under ideal condition. However once the realistic conditions are taken into account, the circuit performs in a significantly different way. Furthermore, it is difficult to conclude which effect is more dominant over other. As can be seen from Figures 12 and 13, the effect of CNT tube diameter is more on the total power as compared to metallic nature of the tube. Similarly, these effects play opposite role in the case of read delay where with the increase in CNT tube diameter the read delay decreases while with the increase in the percentage of metallic CNT the read delay increases. Obviously less read delay is required. Hence the impact of metallic nature is more important to consider. For SNM and WM, the effect of tube diameter is more pronounced than the metallic nature of the CNT. SNM decreases with increase in both the tube diameter and the metallic tubes while WM increases with the tube diameter while it decreases with the metallic tube.

As the result suggests that effect of tube diameter and metallic nature of CNT has different behavior over performance metrics, it becomes very important to perform an optimization considering the effect of both of these imperfections in the design. This would be left as a part of future work.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

[1] S. Joshi, S. Mohanty, and E. Kougianos, "Simscape based ultra-fast design exploration of graphene based nanoelectronic systems," in *Proceedings of the 14th IEEE Computer Society Annual Symposium on VLSI (ISVLSI '15)*, vol. 9060, pp. 292–296, July 2015.

[2] S. Joshi, "Simscape based ultra-fast IC design exploration: Graphene-Nanoelectronic Circuits Case Studies," *Springer Analog Integrated Circuits and Signal Processing Journal*, vol. 87, no. 3, pp. 407–420, 2016.

[3] E. Kougianos, S. Joshi, and S. P. Mohanty, "Multi-swarm optimization of a graphene FET based voltage controlled oscillator circuit," in *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI '15)*, pp. 567–572, Montpellier, France, July 2015.

[4] S. Rajendra Prasad, B. K. Madhavi, and K. Lal Kishore, "Design of a 32nm 7T SRAM Cell based on CNTFET for low power operation," in *Proceedings of the International Conference on Devices, Circuits and Systems (ICDCS '12)*, March 2012.

[5] S. R. Prasad, B. K. Madhavi, and K. Lal Kishore, "Design of a 32nm 7T SRAM Cell based on CNTFET for low power operation," in *Proceedings of the International Conference on Devices, Circuits and Systems (ICDCS '12)*, pp. 443–446, March 2012.

[6] S. Lin, Y.-B. Kim, F. Lombardi, and Y. J. Lee, "A new SRAM cell design using CNTFETs," in *Proceedings of the International SoC Design Conference (ISOCC '08)*, vol. 1, pp. 168–171, November 2008.

[7] A. K. Kureshi and M. Hasan, "Performance comparison of CNFET- and CMOS-based 6T SRAM cell in deep submicron," *Microelectronics Journal*, vol. 40, no. 6, pp. 979–982, 2009.

[8] N. S. Bhat, "Design and modelling of different SRAM'S based on CNTFET 32NM technology," *International Journal of VLSI Design & Communication Systems*, vol. 3, no. 1, pp. 69–83, 2012.

[9] B. Ebrahimi and A. Afzali-Kusha, "Realistic CNFET based SRAM cell design for better write stability," in *Proceedings of the 10th International Symposium on Quality of Electronic Design (ISQED '09)*, pp. 14–18, San Jose, Calif, USA, 2009.

[10] S. Joshi, S. P. Mohanty, E. Kougianos, and V. P. Yanambaka, "Graphene nanoribbon field effect transistor based ultra-low energy SRAM design," in *Proceedings of the IEEE International Symposium on Nanoelectronic and Information Systems (iNIS '16)*, pp. 76–79, Gwalior, India, December 2016.

[11] Z. Zhang, J. G. Delgado-Frias, and J. Nyathi, "CNTFET SRAM cell design with tolerance to metallic CNTs," in *Proceedings of the 53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS '10)*, pp. 1105–1108, Seattle, Wash, USA, August 2010.

[12] L. Sun, J. Mathew, R. A. Shafik, D. K. Pradhan, and Z. Li, "A low power and robust carbon nanotube 6T SRAM design with metallic tolerance," in *Proceedings of the 17th Design, Automation and Test in Europe (DATE '14)*, March 2014.

[13] B. C. Paul, S. Fujita, M. Okajima, T. H. Lee, H.-S. P. Wong, and Y. Nishi, "Impact of a process variation on nanowire and nanotube device performance," *IEEE Transactions on Electron Devices*, vol. 54, no. 9, pp. 2369–2376, 2007.

[14] K. J. Kuhn, "Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS," in *Proceedings of the IEEE International Electron Devices Meeting (IEDM '07)*, pp. 471–474, Washington, DC, USA, December 2007.

[15] http://nano.stanford.edu/models.php.

[16] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—part I: model of the intrinsic channel region," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3186–3194, 2007.

[17] Z. Wang, M. Karpovsky, and A. Joshi, "Influence of metallic tubes on the reliability of CNTFET SRAMs: error mechanisms and countermeasures," in *Proceedings of the 21st Great Lakes Symposium on VLSI (GLSVLSI '11)*, pp. 359–362, Lausanne, Switzerland, May 2011.

[18] Y. Li, D. Mann, M. Rolandi et al., "Preferential growth of semiconducting single-walled carbon nanotubes by a plasma enhanced CVD method," *Nano Letters*, vol. 4, no. 2, pp. 317–321, 2004.