Research Article

Characterization and Optimization of a Single-Transistor Active Pixel Image Sensor with Floating Junction Connected to Floating Gate

Xin-Yan Liu, Jun Wu, Xiao-Yong Liu, Shuai Zhang, Xi Lin, Chun-Min Zhang, Peng-Fei Wang, and David Wei Zhang

State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University, Room 208, Complex Building, No. 400, Guo Ding Road, Yang Pu District, Shanghai 200433, China

Correspondence should be addressed to Peng-Fei Wang; pfw@fudan.edu.cn

Received 7 November 2014; Accepted 22 April 2015

Academic Editor: Marco Grassi

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The application of semifloating gate transistor (SFGT) as the single-transistor active pixel image sensor (APS) is investigated in this paper. This single-transistor (1T) APS can realize the functions of the conventional 3T CMOS image sensor. The device operation mechanism, optimization methods, and transient behavior measurements will be discussed. Because the floating junction of this device is connected to the floating gate, special behaviors such as floating gate voltage pinning effects were observed. The transient time measurement emulating the exposure procedure also confirmed the light sensing function as a single-transistor image sensor.

1. Introduction

Active pixel image sensor (APS) is a concept of structure, which realizes photon absorption, signal charge storage, signal charge to voltage conversion, and signal voltage amplification inside the pixel. Basic APS structure is composed of three transistors and one photodiode (3T-APS). Compared with passive pixel sensor (PPS), an APS converts the accumulated signal charges to a potential in the gate. By introducing amplification at a pixel, APS improves image quality compared with PPS [1]. The 4-transistor APS has improved pixel performance with the addition of one transistor to suppress the noise level and improve the dynamic range. However, the increased number of transistors leads to decreased fill factor (FF) and in return limits the exposure speed and photodiode capacitance (C_{PD}). Historically, many methods for raising FF have been put forward in [2–8]. For example, back illumination has been widely developed to improve FF. Circuits with shared transistors have been widely used in image sensor to reduce the transistor number. Recently, a semifloating gate transistor (SFGT) having imaging function has been proposed. The floating junction is connected to the floating gate. The signal charge to voltage conversion

and signal voltage amplification are realized by a single device. Thus, SFGT has the active imaging function and FF of pixel array can be improved. In this paper, this structure concept will be investigated by device simulation and device measurements.

2. Device Structure and Cell Operation

In Figure 1, the equivalent circuit and the cross-sectional view of the planar channel 1T-IPD APS cell are shown. This device consists of one floating gate (FG) NMOS and one floating junction photodiode (PD). The control gate (CG) is n^+ doped and the FG is p^+ doped. A window is opened at one side of the first silicon-dioxide (SiO_2) layer. The p^+ -type FG is connected to the floating anode of the photodiode. P^+ -type floating well is surrounded by n -doped well to form a p - n junction photodiode.

Electrically, the SFGT image sensor is composed of one photodiode and one N -type MOSFET with a floating gate. The threshold voltage of the FG NMOSFET can be modulated by the current through the p - n junction photodiode. In order to improve the performance, the tunneling generation

FIGURE 1: (a) Equivalent circuit; (b) cross-sectional view of simulated structure of the proposed APS cell.

mechanism must be suppressed and the photogeneration mechanism must be enhanced. Meanwhile, the operation voltage of FG NMOSFET should be adjusted so that the read-out operation window falls inside its linear region ($V_g - V_{th} \gg V_{ds}$) or drain current saturation region ($V_g - V_{th} < V_{ds}$) intentionally. In the following, these optimization methods will be discussed by simulation. Devices are first constructed by using Silvaco TCAD Athena process simulator and then transferred into the Silvaco TCAD Atlas device simulator.

2.1. Suppression of Tunneling Effect. As shown in Figure 1(b), the PD is gate controlled along the surface of silicon, which is well known as a tunneling field effect transistor. In previous research [9], TFET is used as a selective switch to enhance the reverse-biased diode current and write “1” signal charges into the floating gate. During the writing “1” operation, electrons in the valence band of the P⁺ floating gate flow to the conduction band of N⁺ drain by large local electric field. Therefore, the tunneling current is a generation current and the generated signal charges—holes are stored in the floating gate by several parallel capacitors and the generated electrons can flow out through the electrode. Similarly, illumination can generate electron-hole pairs and electric field separates them and forms current. Therefore, two carrier-generation mechanisms occur in this device. When this device is used as an image sensor, the gate controlled tunneling generation mechanism of the embedded tunneling field effect transistor (TFET) should be suppressed to improve the dark current level. A feasible method is to adjust the implant dose and energy to suppress the tunneling effect below gate of the embedded TFET. Figure 2 shows the effect of doping profile on the tunneling generation current. The doping profiles below the control gate are shown as Figure 2(a) by a cutline. The corresponding tunneling performances of four different devices with varying doping profiles are exhibited in Figure 2(b). It can be seen that devices with lower n⁺ doping level have lower tunneling current magnitude. Considering the exposure operation with V_d at 2 V and V_{cg} at -1 V, the tunneling current is picoamperes per micron for device structure-4.

TABLE 1: Bias conditions for reset, exposure, and read operations.

Operation	V_{cg} (V)	V_d (V)	Time (μ s)
Reset	3	0	1
Exposure	-1	2	1
Read	1	1	1

2.2. Photodiode. Photodiode normally works under the reverse-biased condition as a light sensor [1]. When illuminated, electron-hole pairs are generated and then separated by the electric field. Therefore, most of the signal charges are generated inside or near the depletion region. Because of the stable current of a reverse-biased diode in a relatively large voltage window, the potential change in the storage point (FG) just slightly affects the photogeneration current. Therefore, the potential change is almost linear during the exposure operation. Figure 3 shows the photocurrent responses of the integrated photodiodes to four lights with different wavelengths. The source bias varies from -2.0 V to 0 V. It can be seen that the green light is the most sensitive. When the source bias varies from -2.0 V to 0 V, almost the same current level is observed. The gate bias will have impact on the depletion depth and in return affect the photocurrent. When biasing the gate at -1 V, the depletion region of the silicon surface right below the gate is expanded and more charged carriers are forced by the electric field. As a result, the difference between dark current and light current is the effect of illumination, which is to be calculated by correlated double sampling (CDS) circuit to eliminate flat pattern noise (FPN).

2.3. NMOSFET and Its Operation. Figure 4(a) shows the schematic and transfer characteristics of the embedded NMOSFET at $V_{ds} = 0.1$ V. The threshold voltage of the simulated FG-NMOSFET is 1.162 volts. The transient operation includes reset, reading, and exposure. Figures 4(b) to 4(d) illustrate the current density of the device during different operation status. The operation conditions are given in Figure 5 and Table 1, respectively. First, CG is biased at

FIGURE 2: (a) Embedded TFET and the cutline for net doping, (b) corresponding I_d - V_d curves family, and (c) corresponding I_d - V_g curves family.

3 V and drain is biased at 0 V to reset the device. As shown in Figure 4(b), signal charges are pushed out of the FG. During the reading operation, CG and drain are biased with the voltage setting of reading operation. As shown in Figure 4(c), the drain-source current through the embedded NMOSFET is read out. During the exposure operation, the photodiode is reversely biased and the embedded NMOSFET is turned off. Under illumination, photocurrent can be of

several orders of magnitude higher than dark condition. As shown in Figure 4(d), there are three pn diodes in this device and the diode connected to FG contributes to signal charges collection.

2.4. Transient Simulation of SFGT Image Sensor. Because there is one color filter array before the sensor array in digital cameras to split light into three colors (red, green, and blue),

FIGURE 3: Current voltage characteristics of the photodiodes under dark and illumination conditions. (a) Comparison between pn diode and TFET without BBT.KANE model, (b) comparison between pn diode and TFET with BBT.KANE model, and (c) response to four separate wavelength lights.

FIGURE 4: (a) I_d - V_g characteristics of the embedded NMOSFET and contour diagrams of total current density under different operational conditions: (b) reset, (c) read, and (d) exposure.

the responses of SFGT image sensor to these three colors are simulated. 470 nm, 550 nm, and 700 nm wavelengths are assumed to represent blue, green, and red light, respectively. The response to multispectral light is also studied.

According to Figure 5, the full operation sequence has four steps: reset/reading/exposure/reading. Each step has a pulse width of $1\mu\text{s}$ including 1 ns ramping up/down edges. The transient simulation results of multispectral light are shown in Figure 6. For different illumination intensity, the read-out drain current varies. That means the signal of light intensity is converted to drain current signal directly using a single transistor. Thus, a single-transistor APS is realized. According to the transient simulation results, the 2nd reset operation results in different current levels, which is known as flat pattern noise and is to be eliminated by following CDS (correlated double sampling) circuit. The current levels under multispectral condition were also investigated and similar results were observed.

The potentials of SFG are extracted and shown in Figure 7, where a linear response to exposure time was

observed. Considering the constant pn junction reverse-biased current obtained from Figure 3, conversion gain is $11.85\mu\text{V}/\text{hole}\cdot\mu\text{m}$, $19.2\mu\text{V}/\text{hole}\cdot\mu\text{m}$, and $12.78\mu\text{V}/\text{hole}\cdot\mu\text{m}$ for 470 nm, 550 nm, and 700 nm, respectively. Corresponding differential capacitance is $13.5\text{fF}/\mu\text{m}$, $8.33\text{fF}/\mu\text{m}$, and $12.5\text{fF}/\mu\text{m}$ for 470 nm, 550 nm, and 700 nm, respectively.

3. Device Fabrication and Measurements

The proposed device is fabricated using $0.18\mu\text{m}$ technology. The TEM photograph is shown as Figure 8. The drain side doping profile is adjusted to suppress tunneling effect induced by control gate. The control gate forms one MOS capacitor and the depletion region can be extended to enhance physical PD area if a negative V_{CG} is applied, as is similar to the charge-coupled device (CCD).

3.1. Direct Current Measurement. Direct current measurement is performed to investigate the static behavior of the device.

FIGURE 5: V_d and V_{cg} along the transient simulation time.

The output characteristics of SFGT image sensor are shown in Figure 9(a). In a SFGT image sensor, the drain region is coupled to the floating gate through a parasitic pn junction diode. That means the floating gate voltage is pinned to drain voltage if the sweeping speed is slow enough. It can be seen in Figure 9(a) that the drain current curves overlap as the delay time of the bias point is longer than 60 ms during DC measurement. The pinning effect results in V_d larger than $V_{cg} - V_{th}$; thus, the device works in its drain current saturation region if very slow sweeping speed is used for measurement. From Figure 9(a), the threshold voltage of parasitic NMOS transistor is around 1.25 volts that highly matches the simulation results.

Under light illumination, it takes much shorter time to achieve the balance between floating gate voltage and the drain voltage because of the addition of light current. The measured results are shown in Figure 9(b). Drain current has two components: I_{pn} (current through pn diode) and I_{ch} (channel current). There are two “steady states” on the hysteretic diagram with forward sweeping and backward sweeping. Basically I_{ch} is the dominant current component which interprets the rise and fall of drain current. Higher and lower steady states resulted from the light-induced load current and the sweeping speed. Higher steady states work near the V_{oc} point (solar cell mode). Lower steady states are deeply influenced by light intensity because of very different characteristic curve of load current on pn diode. There are three important effects observed in Figure 9(b). Firstly, I_{ch} is increased because of the increased FG potential because of an additional voltage under solar cell mode.

TABLE 2: Voltage settings of transient time measurement.

Operation	V_{cg} (V)	V_d (V)	Time (ms)
Reset	2	-1	10
Exposure	0	4	20
Read	1.2	1.5	0.3
Standby	0	0.5	x

Secondly, higher light sensing speed is achieved because of the increased photocurrent. Thirdly, backward scanning drain current curve gets much closer to the forward scanning drain current because the floating gate voltage is balanced with the drain voltage very quickly so that the control gate switching only has minor impact on the floating gate voltage.

In Figure 9(c), the device is measured under a light intensity of 70 lux and with varying delay time of scanning. The control gate voltage was swept from -3 V to 3 V and then swept back. With faster sweeping speed, the control gate voltage becomes dominant; thus a higher steady drain current is observed when sweeping V_{CG} from -3 V to 3 V. With slower sweeping speed, the V_{FG} pinning effect becomes dominant so that V_{FG} is closer to V_D . The steady drain current during forward sweeping is lowered.

3.2. Transient Time Measurement. The exposure transient operation is executed. The timing and voltage settings are shown in Figure 10(a) and Table 2. Figure 10(b) is the zoom-in picture of Figure 10(a) for the 0.3 ms voltage settings of read operation. The transient time measurement results are shown

FIGURE 6: (a) Drain current along the transient time under different light conditions. (a) Blue, (b) green, (c) red, and (d) visible light range.

FIGURE 7: Extracted potential states in SFG along the transient simulation time under different light conditions. (a) Blue, (b) green, (c) red, and (d) visible light range.

FIGURE 8: TEM photograph of the proposed 1T APS with SFG structure.

FIGURE 9: Direct current test results: (a) sweep drain voltage, (b) double directional sweep control gate voltage, and (c) influence of sweeping delay time.

in Figure 10(c). It can be seen that, with different light illumination intensities, the resulting read-out drain current varies. That means that light is sensed by this cell and converted to read-out current locally. A single-transistor active pixel

image sensor is realized and confirmed. Depending on the voltage settings, the read-out working point can work in the linear region or the saturation region of the FG NMOSFET. However, because of the parasitic capacitance of the cables

FIGURE 10: (a) Voltage settings of transient time measurement, (b) zoom-in picture of the voltage settings of read operation, and (c) dependence of drain current on transient time during the transient time measurement.

and the noise introduced by the off-chip amplifier, strong noise is also observed. Integration of amplifier on chip can improve the signal/noise ratio.

4. Conclusion

In this paper, one novel single-transistor APS cell was simulated and measured. Because the floating junction is connected to floating gate, special behaviors such as floating gate voltage pinning effects are observed by simulation and measurements. The optimization methods were studied to enhance the light sensitivity. Finally, the transient time

measurement emulating the exposure procedure confirmed the light sensing function as a single-transistor image sensor.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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