Hindawi Publishing Corporation
Journal of Sensors
Volume 2016, Article ID 1436371, 7 pages
http://dx.doi.org/10.1155/2016/1436371

Research Article

A 5 V-to-3.3 V CMOS Linear Regulator with Three-Output Temperature-Independent Reference Voltages

San-Fu Wang

Department of Electronic Engineering, Ming Chi University of Technology, Taishan, Taiwan

Correspondence should be addressed to San-Fu Wang; sf_wang@mail.mcut.edu.tw

Received 24 May 2016; Revised 15 August 2016; Accepted 19 September 2016

Academic Editor: Hao Gao

This paper presents a 5 V-to-3.3 V linear regulator circuit, which uses 3.3 V CMOS transistors to replace the 5 V CMOS transistors. Thus, the complexity of the manufacturing semiconductor process can be improved. The proposed linear regulator is implemented by cascode architecture, which requires three different reference voltages as the bias voltages of its circuit. Thus, the three-output temperature-independent reference voltage circuit is proposed, which provides three accurate reference voltages simultaneously. The three-output temperature-independent reference voltages also can be used in other circuits of the chip. By using the proposed temperature-independent reference voltages, the proposed linear regulator can provide an accurate output voltage, and it is suitable for low cost, small size, and highly integrated system-on-chip (SoC) applications. Moreover, the proposed linear regulator uses the cascode technique, which improves both the gain performance and the isolation performance. Therefore, the proposed linear regulator has a good performance in reference voltage to output voltage isolation. The voltage variation of the linear regulator is less than 2.153% in the temperature range of −40°C–120°C, and the power supply rejection ratio (PSRR) is less than −42.8 dB at 60 Hz. The regulator can support 0~200 mA output current. The core area is less than 0.16 mm^2.

1. Introduction

Over the last few years, the miniature sensor, the medical electronic, and the portable electronic products are increasingly popular [1–3]. In order to make these products easy to use, easy to carry, and easy to promote, the demands of these products are small size, low cost, low power, and integrated several functions on a chip. Therefore, reducing the size and cost of these products is an important research direction. The traditional miniature sensor and medical electronic and portable electronic products utilize the external linear regulator to convert the input voltage to the required voltage. And the external linear regulator usually has large size and high cost, which do not meet the requirements of the miniature sensor and medical electronic and portable electronic products. Based on these reasons, on-chip linear regulator is required to meet the low cost and small size requirement.

In most of CMOS process, in order to reduce the complexity and the cost of the manufacturing semiconductor process, manufacturers do not provide high voltage transistor. For example, a typical 0.18 μm CMOS process usually does not provide 5 V transistor. Thus, a 5 V-to-3.3 V linear regulator circuit, which uses the 3.3 V CMOS transistors to replace the 5 V CMOS transistors, is important, because it can reduce the cost and the size of products effectively.

Moreover, the miniature sensor and the medical electronic products usually need accurate reference voltages and supply voltages to improve the accuracy of the miniature sensors and medical electronics. A complex electronic system usually needs many different reference voltages to support the requirements of the different circuits on a chip. Those reference voltages need to have a good characteristic to cover temperature variation.

According to the above concepts, a full on-chip 5 V-to-3.3 V CMOS linear regulator [4] with three-output temperature-independent reference voltages has been proposed in this paper, which can achieve the requirements of high accuracy, small size, low cost, low power, stable output voltage, and three-output temperature-independent accurate reference voltages. Thus, it is suitable for the miniature sensor and medical electronic and portable electronic applications.

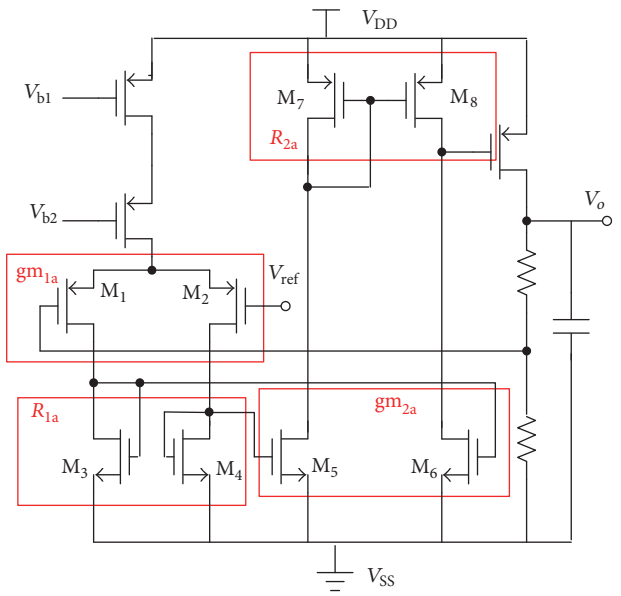

Figure 1: The conventional linear regulator.

2. Proposed Circuit

A linear regulator typically consists of several parts [5–8]: an error amplifier circuit, a temperature-independent reference circuit [9], a feedback resistance network [10, 11], pass transistors, and output capacitors [12]. The error amplifier circuit and temperature-independent reference circuit are the most important components of linear regulator, which are discussed below.

2.1. Error Amplifier Circuit. The error amplifier circuit usually dominates the performance of linear regulator [13, 14], especially for the gain of error amplifier, which can influence the performances of line regulation, load regulation, and power supply rejection ratio (PSRR). However, the characteristics of error amplifier usually make trade-off between gain and current consumption. Therefore, how to design an error amplifier with both high gain and low current consumption is important.

The conventional linear regulator is shown in Figure 1. The gain of error amplifier in a typical regulator can be approximately calculated by

$$A_{\text{typical}} = 2 \times \text{gm}_{1a} \times R_{1a} \times \text{gm}_{2a} \times R_{2a}, \tag{1}$$

where gm_{1a} is the transconductance of transistors M_1 and M_2 and gm_{2a} is the transconductance of transistors M_5 and M_6, and those stages are common-source topology. R_{1a} is the output resistance of devices M_3 and M_4, and R_{2a} is the output resistances of devices M_7 and M_8. However, the conventional 5 V-to-3.3 V linear regulator in Figure 1 cannot be implemented by using the 3.3 V transistors. Moreover, (1) shows the gain of the error amplifier in Figure 1. It shows that if we want to increase the gain of the error amplifier, increase of the transconductance of gm_{1a} and gm_{2a} is inevitable, and it requires more quiescent current.

Figure 2 shows the proposed linear regulator, which uses the cascode technique in the design. The drop of input voltage is dispersed by the cascode transistors. Thus, the proposed circuit can use the 3.3 V CMOS transistors to replace the 5 V CMOS transistors. In this case, the gain of error amplifier in the proposed regulator can be approximately calculated by

$$\begin{aligned} &A_{\text{proposed error amplifier}} \\ &\quad = 2 \times \text{gm}_{1b} \times R_{1b} \times \text{gm}_{2,\text{cascode stage}} \times R_{2,\text{cascode stage}}, \end{aligned} \tag{2}$$

$$\begin{aligned} &\text{gm}_{2,\text{cascode stage}} \\ &\quad \approx \frac{\text{gm}_{15}\text{ro}_{15}\left[\text{ro}_{17}\left(\text{gm}_{17} + \text{gm}_{b17}\right) + 1\right]}{\text{ro}_{15}\text{ro}_{17}\left(\text{gm}_{17} + \text{gm}_{b17}\right) + \text{ro}_{15} + \text{ro}_{17}} \\ &\quad = \frac{\text{gm}_{16}\text{ro}_{16}\left[\text{ro}_{18}\left(\text{gm}_{18} + \text{gm}_{b18}\right) + 1\right]}{\text{ro}_{16}\text{ro}_{18}\left(\text{gm}_{18} + \text{gm}_{b18}\right) + \text{ro}_{16} + \text{ro}_{18}}, \end{aligned} \tag{3}$$

$$\begin{aligned} R_{2,\text{cascode stage}} &\approx \left(\text{gm}_{19} + \text{gm}_{b19}\right)\left(\text{ro}_{19}\text{ro}_{21}\right) \\ &= \left(\text{gm}_{20} + \text{gm}_{b20}\right)\left(\text{ro}_{20}\text{ro}_{22}\right), \end{aligned} \tag{4}$$

where gm_{1b} is the transconductance of transistors M_{11} and M_{12} and $\text{gm}_{2,\text{cascode stage}}$ is the transconductance of cascode transistors M_{15}, M_{16}, M_{17}, and M_{18}. This stage provides large transconductance and high input-output isolation. R_{1b} is the output resistance of transistors M_{13} and M_{14}. $R_{2,\text{cascode stage}}$ is the output resistance, which is composed of devices M_{19}, M_{20}, M_{21}, and M_{22}. This stage is also a cascode stage, which provides high impedance for output load. To compare (1) and (2), the proposed linear regulator increases the gain for the error amplifier without increasing current dissipation. In other words, compared with the conventional topology, the proposed error amplifier can achieve the same gain with less current. Moreover, the common-gate stage circuit (M_{17} and M_{18} in Figure 2) also improves the reverse isolation performance between output voltage and reference voltage. Thus, no matter whether the output load has changed or not, the input reference voltage will not be disturbed. And the reference voltages also can be used for other circuits on the chip, simultaneously.

2.2. Multioutputs Temperature-Independent Reference Circuit. The temperature-independent reference circuit is perhaps the most important component in the mixed-signal integration chip. It provides the accurate reference voltage for many blocks in the chip. Moreover, it determines the accuracy of the measured signals.

In Figure 2, the proposed linear regulator needs three accurate reference voltages (V_{ref} 0.8, V_{ref} 1.7, and V_{ref} 3.3), simultaneously. The conventional temperature-independent reference circuit uses the operation amplifier to achieve conversion between different reference voltages. However, these additional operation amplifiers not only consume the power but also increase the chip area. Figure 3(a) shows the conventional temperature-independent reference circuit, and Figure 3(b) shows the conventional method of the conversion between different reference voltages.

Figure 4 shows the proposed temperature-independent reference circuit, which is also implemented by cascode

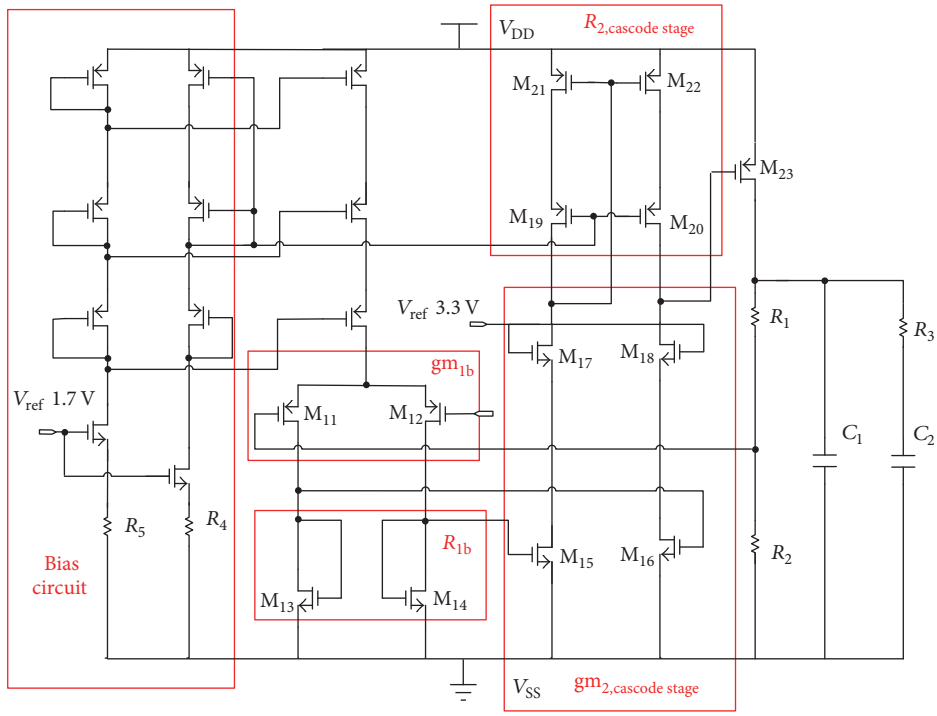

Figure 2: The proposed linear regulator.

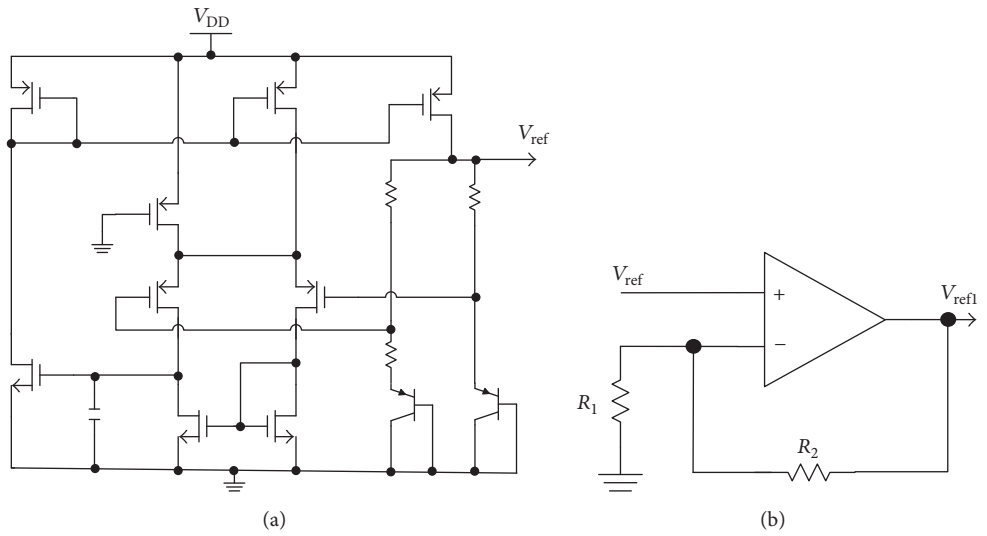

Figure 3: The conventional temperature-independent reference circuit and reference voltage conversion circuit.

architecture. Therefore, it can use the 3.3 V CMOS transistor to replace the 5 V CMOS transistor. The cascode architecture also provides a stable current source to resistance and BJT.

The conventional temperature-independent reference circuit adds negative temperature coefficient and positive temperature coefficient with proper weighting to get a zero temperature coefficient. However, the proposed reference voltages conversion circuit uses different technique. In Figure 4, the first temperature-independent reference voltage, V_{ref} 1.7, is generated by the above technique, the second temperature-independent reference voltage, V_{ref} 0.8, is generated by V_{ref} 1.7-V_{gsMn1}, and the third temperature-independent reference voltage, V_{ref} 3.3, is generated by V_{ref} 1.7-V_{gsMp1}.

In other words, the proposed reference voltage conversion technique is implemented by the NMOS gate-source voltage drop and PMOS gate-source voltage rise. Furthermore, the proposed reference voltage can get accurate reference voltages by adjusting R_2 and R_3. According to the above technology, the three-output temperature-independent reference voltages circuit is proposed, which provides three accurate reference

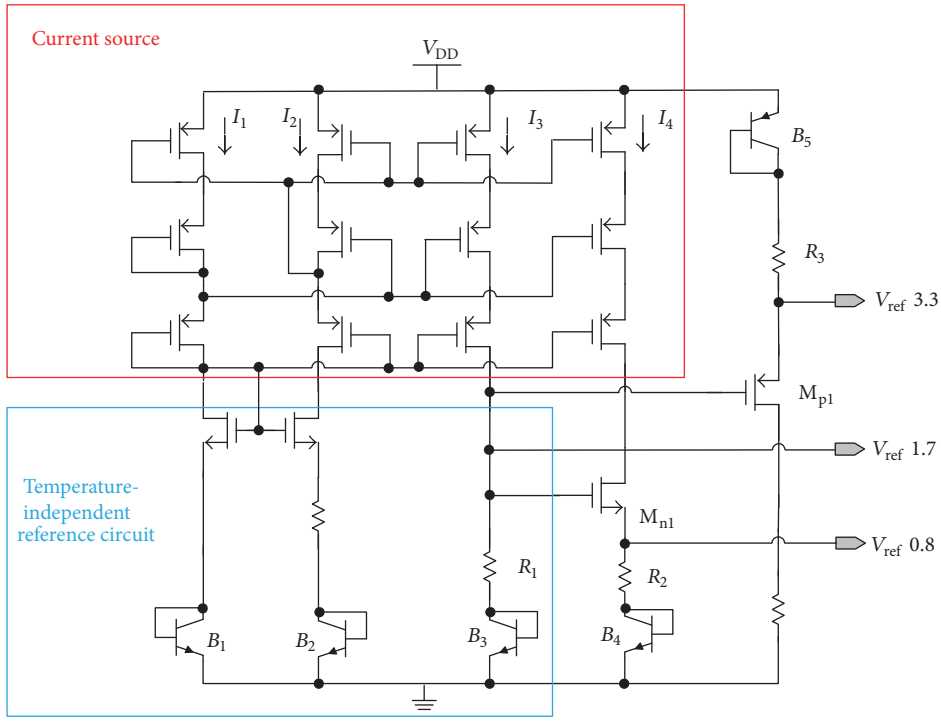

Figure 4: The proposed three-output temperature-independent reference circuit.

voltages simultaneously. The three-output temperature-independent reference voltages also can be used in other circuits of the chip. Compared to standard voltages conversion circuit, shown in Figure 3(b), the proposed voltages conversion circuit is implemented without additional operation amplifiers, which reduce the power consumption and the chip area. So, it is suitable for low cost, low power, small size, and highly integrated system-on-chip (SoC) applications.

3. Measurement and Simulation Results

The linear regulator and three-output temperature-independent reference voltages circuit is designed with a TSMC 0.18 μm CMOS process with 5 V supply voltage.

Figure 5 shows the measurement results of output voltage, which is operated in the range of environmental temperature between −40°C and 120°C. The output voltage variation of proposed linear regulator is less than 2.153%. It verifies that the relationship of output voltage and environmental temperature is very small.

In general, the settling time is an important specification of linear regulator. It is the time required for an output to reach stability when the load is changed. Thus, we measure the dynamic voltage change and current change responses from light load to heavy load as shown in Figure 6 and from heavy load to light load as shown in Figure 7. Figures 6 and 7 also show that the settling time of the proposed linear regulator is less than 50 ns. Figure 8 shows the PSRR measured results of the proposed linear regulator at 60 Hz. In this experiment, the input noise frequency was fixed at 60 Hz, and the measurements were made at the output port (V_o).

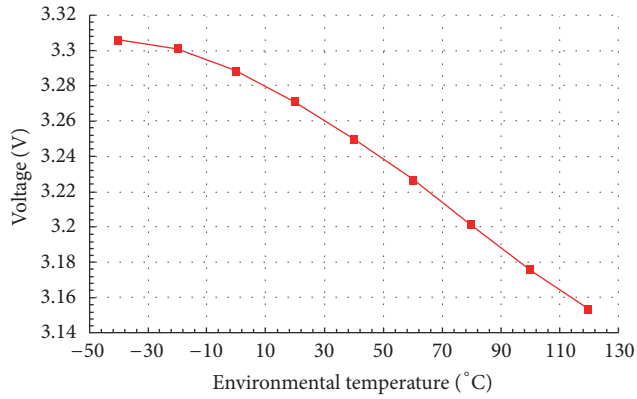

Figure 5: The relationship of the output voltages and the environmental temperatures.

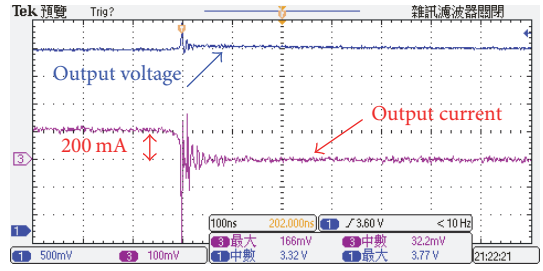

Figure 6: The experimental results of dynamic response, the output voltage V_o, and the output current from 200 to 0 mA (horizontal scale: 100 ns/div; vertical scale: 500 mV/div and 200 mA/div).

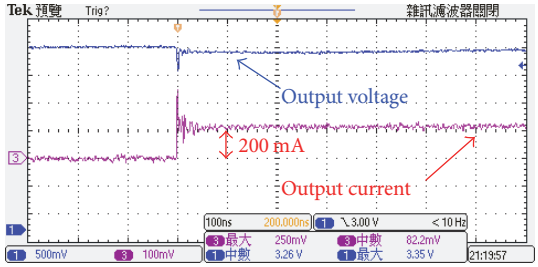

Figure 7: The experimental results of dynamic response, the output voltage V_o, and the output current from 0 to 200 mA (horizontal scale: 100 ns/div; vertical scale: 500 mV/div and 200 mA/div).

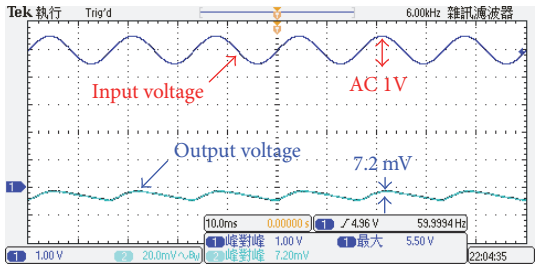

Figure 8: The PSRR of the proposed linear regulator, the input voltage V_{DD}, and output voltage V_o. (horizontal scale: 10 ms/div; vertical scale: 1000 and 20 mV/div, from top to bottom).

The input noise amplitude is AC 1 V at input port (V_{DD}). It verifies the PSRR performance of the proposed linear regulator is 42.85 dB at 60 Hz, which can prove against of AC (household power) noise rejection. Figure 9 shows the PSRR performance at difference input noise frequencies. They verify the proposed linear regulator has good PSRR performance. Figure 10 shows the simulation results of three-output temperature-independent reference voltages. Because we did not put measured points for these three-output temperature-independent reference voltages during the chip design, in here, we only show the simulation results of the proposed three-output temperature-independent reference voltages. It is verified that the proposed circuit can provide three temperature-independent reference voltages simultaneously. When the temperature changes between −40°C and 120°C, the amount of 3.3 V, 1.7 V, and 0.8 V reference voltages range is less than 0.424%, 1.462%, and 1.219%, respectively.

The chip micrograph of the proposed linear regulator is shown in Figure 11. The total area is 0.38 × 0.42 mm^2. A summary of the proposed linear regulator's characteristics is given in Table 1. Finally, we compare the proposed linear regulator with the other existing linear regulators in Table 2, which demonstrates that the proposed linear regulator has larger output current, smaller load regulation, faster settling time, and smaller chip area than the other linear regulators. Moreover, the reference voltages and bias circuit usually were not discussed in the other existing linear regulator papers. This paper discusses reference voltage circuit and linear regulator circuit together, which makes the high integrity of the circuit. In addition, the proposed circuit also has accurate output voltage in different environmental temperatures, and it also can provide three temperature-independent reference voltages simultaneously, which can improve the accuracy of the miniature sensors and the medical electronics products.

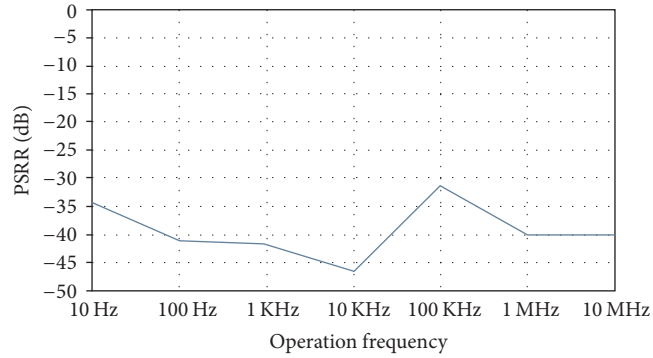

Figure 9: The measured results show the PSRR performance at difference input noise frequencies.

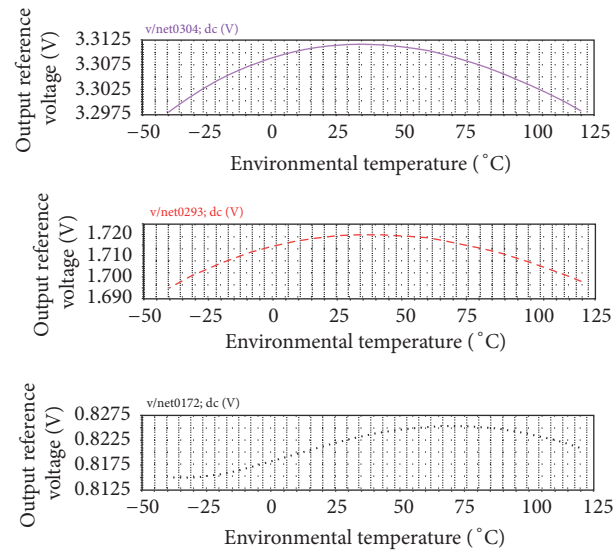

Figure 10: The simulated results of the proposed three-output temperature-independent reference voltages.

Table 1: The specifications of proposed linear regulator.

5 V–3.3 V liner voltage regulator	
Technology	TSMC 0.18 μm CMOS
Supply voltage (V)	5
Output voltage (V)	3.3
Maximum output current (mA)	200
Temperature range (°C)	−40~120
Temperature dependence (ppm/°C)	284
Quiescent current (μA)	247.6
Settling time (ns)	50
PSRR (dB)	−42.85@60 Hz
Chip size: W (mm) × L (mm) = mm^2	0.38 × 0.42 = 0.16

Table 2: The comparison of the proposed linear regulator to other existing linear regulators.

Specifications	2007 [4] TCS-I	2010 [6] TCS-II	1998 [7] JSSC	2010 [10] Microelectronics	This work
Process	0.35 μm CMOS	0.5 μm CMOS	2 μm CMOS	0.35 μm CMOS	0.18 μm CMOS
Supply voltage (V)	3	4.2	1	1.8	5
Quiescent current (μA)	65 (without reference circuit)	50 (without reference circuit)	23 (without reference circuit)	492 (without reference circuit)	247.6 (with reference circuit)
Load regulation (mV/mA)	NA	1.2	0.4	0.013	0.4
PSRR (dB)	−53 (1 KHz)	N/A	NA	NA	−42.85 (60 Hz)
Settling time	15 us	4 us	70 us	50 ns	50 ns
Maximum output current (mA)	50	100	50	180	200
Chip size (mm^2)	0.12	0.263	1.375	0.205	0.16

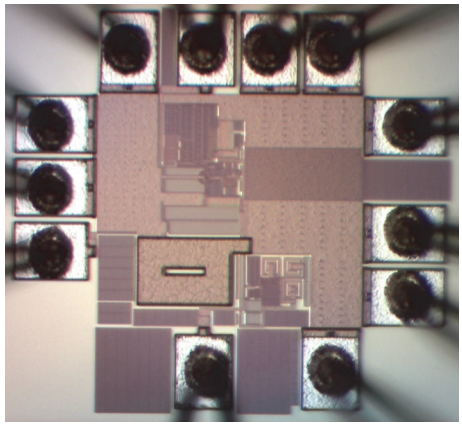

Figure 11: The chip microphotograph of the proposed linear regulator.

4. Conclusions

The proposed linear regulator utilizes the cascode technique to improve the gain and to achieve high line regulation, load regulation, and power supply noise rejection ratio. The proposed circuit uses the 3.3 V CMOS transistors to replace the 5 V CMOS transistors. Thus, the complexity of the manufacturing semiconductor process can be improved. Moreover, the proposed linear regulator can significantly raise the accuracy of the signals. Hence, it is suitable for highly integrated products such as the miniature sensor and the medical electronic and the portable electronic products.

Competing Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

The author would like to thank the National Science Council and the Chip Implementation Center of Taiwan for the project support, chip implementation, and chip measurement.

References

[1] D.-S. Kim, S.-J. Jang, and T.-H. Hwang, "A fully integrated sensor SoC with digital calibration hardware and wireless transceiver at 2.4 GHz," *Sensors*, vol. 13, no. 5, pp. 6775–6792, 2013.

[2] D. Liu, R. Wang, K. Yao, X. Zou, and L. Guo, "Design and implementation of a RF powering circuit for RFID tags or other batteryless embedded devices," *Sensors Journal*, vol. 14, no. 8, pp. 14839–14857, 2014.

[3] W.-Y. Chang, C.-C. Huang, C.-C. Chen, C.-C. Chang, and C.-L. Yang, "Design of a novel flexible capacitive sensing mattress for monitoring sleeping respiratory," *Sensors*, vol. 14, no. 11, pp. 22021–22038, 2014.

[4] R. J. Milliken, J. Silva-Martínez, and E. Sánchez-Sinencio, "Full on-chip CMOS low-dropout voltage regulator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 9, pp. 1879–1890, 2007.

[5] G. W. den Besten and B. Nauta, "Embedded 5V-to-3.3V voltage regulator for supplying digital ICs in 3.3V CMOS technology," in *Proceedings of the 23rd European Solid-State Circuits Conference (ESSCIRC '97)*, pp. 52–55, September 1997.

[6] A. Garimella, M. W. Rashid, and P. M. Furth, "Reverse nested miller compensation using current buffers in a three-stage LDO," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 4, pp. 250–254, 2010.

[7] G. A. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 36–44, 1998.

[8] Z. Du, X.-S. Mei, and M.-X. Xu, "Modelling and analysis of a new piezoelectric dynamic balance regulator," *Sensors*, vol. 12, no. 11, pp. 14671–14691, 2012.

[9] Y.-H. Lam and W.-H. Ki, "CMOS bandgap references with self-biased symmetrically matched current-voltage mirror and extension of sub-1-V design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no. 6, pp. 857–865, 2010.

[10] J.-J. Chen, B.-H. Hwang, and Y.-S. Hwang, "A dual-loop shunt regulator using current-sensing feedback techniques," *Microelectronics Journal*, vol. 41, no. 12, pp. 840–844, 2010.

[11] J.-J. Chen, M.-S. Lin, C.-M. Kung, and Y.-S. Hwang, "Low-quiescent-current fast-response current-feedback shunt regulator," in *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS '08)*, pp. 530–533, Macao, China, December 2008.

[12] J.-J. Chen, M.-S. Lin, H.-C. Lin, and Y.-S. Hwang, "Sub-1V capacitor-free low-power-consumption LDO with digital controlled loop," in *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS '08)*, pp. 526–529, Macao, China, December 2008.

[13] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, 2003.

[14] W. Oh and B. Bakkaloglu, "A CMOS low-dropout regulator with current-mode feedback buffer amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 10, pp. 922–926, 2007.