Research Article

Design and Implementation of 24 GHz Multichannel FMCW Surveillance Radar with a Software-Reconfigurable Baseband

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We designed and developed a 24 GHz surveillance FMCW (Frequency Modulated Continuous Wave) radar with a software-reconfigurable baseband. The developed radar system consists of transceiver, two selectable transmit antennas, eight parallel receive antennas, and a back-end module for data logging and to control the transceiver. The architecture of the developed radar system can support various waveforms, gain control of receive amplifiers, and allow the selection of two transmit antennas. To do this, we implemented the transceiver using a frequency synthesizer device and a two-step VGA (Variable Gain Amplifier) along with switch-controlled transmit antennas. To support high speed implementation features along with good flexibility, we developed a back-end module based on a FPGA (Field Programmable Gate Array) with a parallel architecture for the real-time data logging of the beat signals received from a multichannel 24 GHz transceiver. To verify the feasibility of the developed radar system, signal processing algorithms were implemented on a host PC. All measurements were carried out in an anechoic chamber to extract a 3D range-Doppler-angle map and target detections. We expect that the developed software-reconfigurable radar system will be useful in various surveillance applications.

1. Introduction

In recent years, radar systems have been widely used in various applications, such as defense, automotive, shipping, security, traffic, the medical field, and sports, as radar sensors guarantee system reliability irrespective of environmental factors such as weather and/or light conditions [1]. Generally, for every new or modified application, different radar hardware configurations are needed, which leads to problems such as system cost increases and integration issues. In order to resolve these issues, the SDR (Software Defined Radio) is an attractive solution [2]. The software-reconfigurable radar system, which does not require reengineering, has also been proposed based on the SDR concept [3]. Thus, several radar systems have been studied based on SDR technology for various applications: weather surveillance [4], human motion monitoring [5], radar/communication multifunctionality [6], doorway identification and classification [7], and medical imaging applications [8].

In addition, SDR-based combination of a FMCW (Frequency Modulated Continuous Wave) and CW radar front-end module was developed [9]. In this radar front-end module, the user can control the transmit waveform thorough a DDS (Direct Digital Synthesizer) chip for surveillance radar applications with precise range measurement requirements.

However, for various civil surveillance radar applications to monitor automobile and pedestrian traffic as well as intruders, the range, the azimuth angle, and radial velocity should be simultaneously indicated as target parameters [10]. Moreover, for optimized radar for each type of surveillance application, it should be possible to control the various radar parameters, such as the waveform, receive gain, and sampling rate.

Thus, in this paper, we developed a 24 GHz multichannel FMCW surveillance radar system with a software-reconfigurable baseband. As [10], FMCW radar systems have been, in recent years, used in a variety of surveillance applications
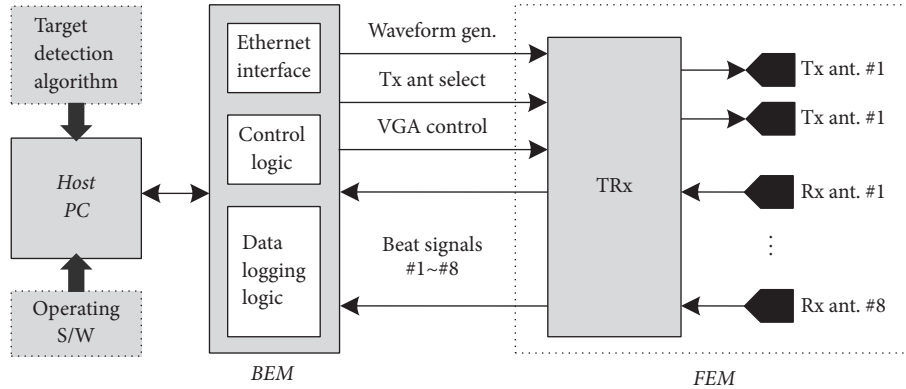
FIGURE 1: Block diagram of the 24 GHz multichannel FMCW radar with a software-reconfigurable baseband.

owing to their simpler hardware architecture, lower peak power output, and lower cost compared to pulse radar.

In the commercial FMCW automotive radar system, direct VCO (Voltage Controlled Oscillator) driving methods have been used. That is, a DAC (Digital Analog Converter) in the back-end module directly controls VCO input voltage to generate a frequency modulation wave. In this case, owing to the VCO tuning characteristics, we cannot generate a linear FMCW transmit signal. In addition, the transmit center frequency can easily be changed according to the temperature condition. Thus, a compensation method is required to resolve these problems, such as an open loop algorithm. In the typical radar architecture, a slow ramp with a different modulation slope for the transmit signal and a pairing algorithm to calculate the detected range and velocity are used [11]. A leading chip vendor, Infineon, has employed such an architecture for their automotive 24 GHz radar system [12].

However, the VCO direct controlled architecture cannot support the fast-ramp based FMCW radar used in this paper, which is a very effective method when used to detect a moving target in a cluttered environment. For fast-ramp generation, the linearity of the modulation is more important, and the phases of the transmitting signals should all be synchronized every modulation period.

Thus, in this paper, we developed a fast-ramp based 24 GHz multichannel FMCW radar system with a software-reconfigurable baseband.

Figure 1 shows a block diagram of the radar system developed in this paper, which is divided into three parts: the FEM (front-end module), BEM (back-end module), and host PC. The FEM is composed of two transmit antennas, eight receive antennas, and a transceiver. The roles of the BEM are to control the FEM and to log the received data and transfer the data to the host PC in real-time. In the host PC, the target detection algorithms and the operating software are implemented. In the target detection algorithms, the ranges and relative velocities of multiple targets can be obtained using means of 2D range-Doppler-FFT (Fast Fourier Transform) processing [13–15]. Moreover, the angle information can be determined by DBF (Digital Beam Forming) based on an array of receiving antennas.

For software-reconfigurable baseband, we implemented a frequency synthesizer device, a two-step VGA (Variable Gain Amplifier), and the two selected transmit antennas in the FEM. Moreover, for the real-time data logging and for effective FEM control, we employed a FPGA (Field Programmable Gate Array) for the developed BEM. The FPGA has become an attractive solution with a good combination of high speed implementation features, along with flexibility for SDRs [16, 17].

For detailed descriptions, this paper is organized as follows. Section 2 describes the architecture and implementation of the proposed radar system. Section 3 shows various experimental results. Finally, Section 4 concludes the article.

2. Implementation of the Software-Reconfigurable Baseband Radar System

2.1. Front-End Module. In this paper, we designed a FEM consisting of a transceiver, antennas, and a radome. A block diagram and a photograph of the FEM are presented in Figures 2 and 3, respectively. In addition, a summary of the corresponding performances is also described in Table 1.

In the transmit part, an ADF4158 frequency synthesizer device is used with a PLL (Phase Locked Loop), resulting in highly linear frequency modulation to compensate for the nonlinear HMC739 VCO (Voltage Controlled Oscillator) tuning characteristics. In order to generate various waveforms with the proper modulation period (T) and bandwidth (B), a PIC16F76 microprocessor is used to control the ADF4158 frequency synthesizer based on a command issued from the BEM interface (with the signal name "*Waveform gen*"). The VCO output is connected to two PAs (Power Amplifiers) through a power divider each with an output power of 10 dBm.

The proposed FEM has two patch-type transmitting antennas with a difference gain (14.1 dB and 19.1 dB) and azimuth angle (26° and 12°) and identical elevation angles (9.9°). The two antennas are selectable through the BEM interface (with the signal name "*Tx ant select*"). The measured
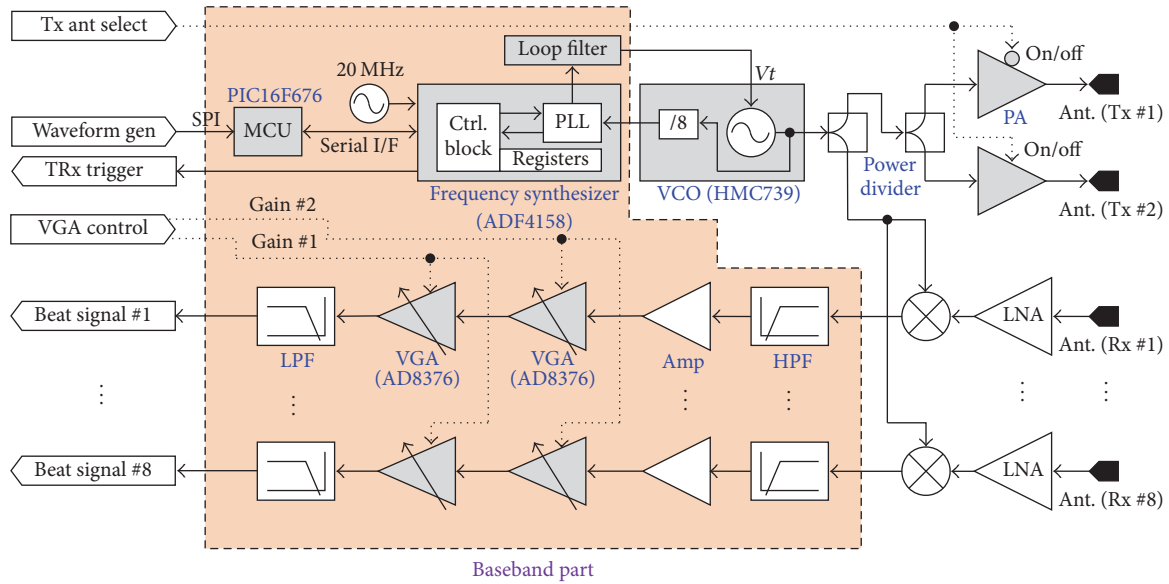
FIGURE 2: Block diagram of the 24 GHz radar front-end module with a software-reconfigurable baseband.
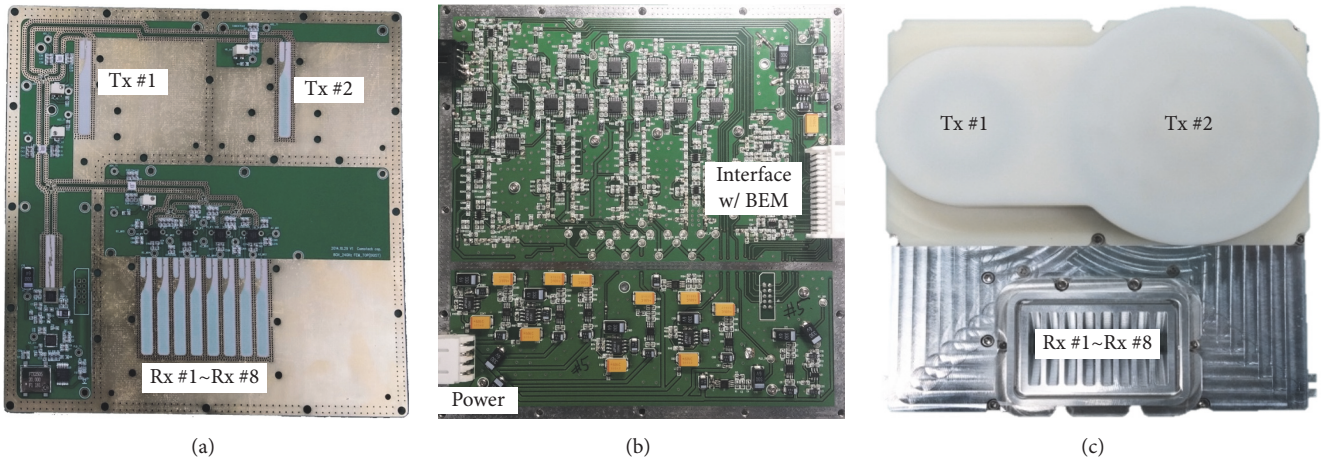

FIGURE 3: Photograph of the 24 GHz radar front-end module with a software-reconfigurable baseband (whole size: 172 ∗ 155 mm^2): (a) top view, (b) bottom view, and (c) final appearance.

azimuth radiation patterns of the two antennas are shown in Figure 4.

Next, in the receiver part, eight channels are implemented. Each channel has a patch-type antenna, a mixer, a HPF (High Pass Filter), an amplifier, a two-step VGA, and a LPF (Low Pass Filter). Each antenna has a 10 dB gain, and the azimuth and vertical FOV (Field Of View) are 99.6° and 9.9°, respectively. Here, all antennas are implemented with half-wave intervals.

The receiver has an overall noise figure of 8.01 dB, and the first amplifier has a fixed gain of 6 dB. The variable gain of each AD8376 VGA can range from −2.5 dB to 42.5 dB. Eight receive beat signals are fed into the BEM through interfaces: the *"Beat signal #1"~"Beat signal #8"* interfaces. In this case, the transmit trigger signal *"TRx trigger"* is also connected

such that BEM can digitalize the beat signals with precise modulation timing.

Therefore, the designed transceiver has a reconfigurable baseband so that it can be controlled by the back-end module. Moreover, in the designed FEM, replacing transmitting and receiving antennas is possible because the connection between the antennas and the transceiver is based on a waveguide type of connection. Thus, the system has very useful architecture for various surveillance applications.

2.2. Back-End Module. The developed BEM consists of an analog part, a FPGA, a DSP (Digital Signal Processor), and a host PC interface, as shown in the block diagram in Figure 5. Here, the hardware of the BEM consists of a main board and a bridge board such as in the photograph shown in Figure 6.

Table 1: Summary of the performance of the developed 24 GHz radar front-end module.

	RF center frequency	24 GHz
	Maximum bandwidth	2 GHz
	Transmitted power	10 dBm
	Number of antennas	2
Tx part	Antenna gain	14.1 dB (Tx #1), 19.1 dB (Tx #2)
	Antenna beamwidth	Azimuth: 26° (Tx #1), 12° (Tx #2)
		Elevation: 9.9° (for both antennas)
	Noise figure	8.02 dB
	Number of antennas	8
	Antenna gain	10 dB
Rx part	Antenna beamwidth	Azimuth: 99.6° (for all antennas)
		Elevation: 9.9° (for all antennas)
	Amp gain	Fixed gain amp: 6 dB
		Variable gain amp: −2.5 dB~42.5 dB

Table 2: Hardware resources of the developed back-end module.

	Devices	Xilinx Virtex-5
	Maximum frequency	294.811 MHz
FPGA	Used slices register/total	166/51,840 (0.32%)
	Used slices LUTs/total	118/51,840 (0.23%)
	Used embedded memory/total	104/288 (36.11%)
	Used I/O pin/total	145/1,200 (12.08%)
	Device	TI TMS320C6xxx
DSP	System clock	1.2 GHz
	Used program memory/total	790 KB/1 MB

represents the structure of 3D memory of the received beat signals on the eight channels.

For 3D data logging in real-time, we utilized a Xilinx Virtex-5 FPGA and used Velilog HDL (Hardware Description Language) to implement the parallel logging functions. In the FPGA shown in Figure 5, the primary data logging path begins with eight parallel LVDS (Low Voltage Differential Signaling) at the serial ADC DDR (Dual Data Rate) clock. The digitalized bit streams are translated as SES (Single Ended Signaling) at the DDR clock, adjusted as the single-ended data rate timing, and then deserialized into 14-bit words at the given sampling rate. Subsequently, the 14-bit words are synchronized with the *"TRx trigger"* signal in the synchronizer block and saved into DPM (Dual Port Memory).

The stored data is transferred to a TI TMS320C DSP through an EMIF (Eternal Memory Interface) and are resent to the host PC through Ethernet. The host PC is used instead of a DSP for signal processing. Thus, the role of the DSP is simply to act as a bridge controller between the FPGA and the host PC, but in the future, we can implement corresponding target indication algorithms in real-time.

The main control unit in the FPGA can generate a waveform based on the context of the waveform LUT (Look-up Table), which contains the setting information for the frequency synthesizer device of the transceiver. In addition, this unit can control the gain of each VGA and select transmit antennas according the configuration registers. The LUT and configuration resisters are managed by host PC through the DSP.

Table 2 shows the hardware resources of the FPGA and DSP for the radar BEM developed in this paper. Because the maximum possible internal operating frequency of the FPGA is reported to be 295.811 MHz, the FPGA can support various ADC sampling rates between 5 MHz and 50 MHz.

As noted above, in this paper the FPGA is optimized for a fast-ramp based FMCW, as shown in Figure 7. If we want to support another modulation or waveform such as CW (Continuous) and/or FSK (Frequency Shift Keying), it can be done by updating the control registers to set the frequency synthesizer and then implementing functionalities for the corresponding data logging process into the FPGA without modifying the hardware. Moreover, if we want to use another radar transceiver with the developed back-end module, this can be done possibly by replacing the bridge board with a
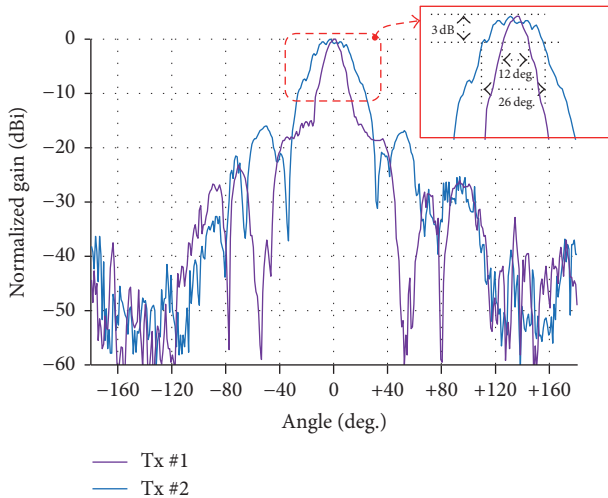

Figure 4: Measured radiation pattern of antennas.

In the analog part, a 14-bit 8-channel AD9252 ADC (Analog to Digital Converter) is implemented to digitalize the eight received beat signals simultaneously. In addition, an 8-bit dual-channel AD5303 DAC (Digital to Analog Converter) is used to control the two VGAs of the FEM. Here, the sampling clocks of the ADC and DAC are generated by a FPGA together with management of their data interfaces.

In the paper, we employ a fast-ramp based FMCW radar waveform for the surveillance radar application, because the method is very effective to detect moving target information (range, velocity, and angle) from clutter environment [13–15]. Figure 7(a) shows the transmitted fast-ramp train, which has a saw-tooth shape in the frequency-time domains. Figure 7(b)
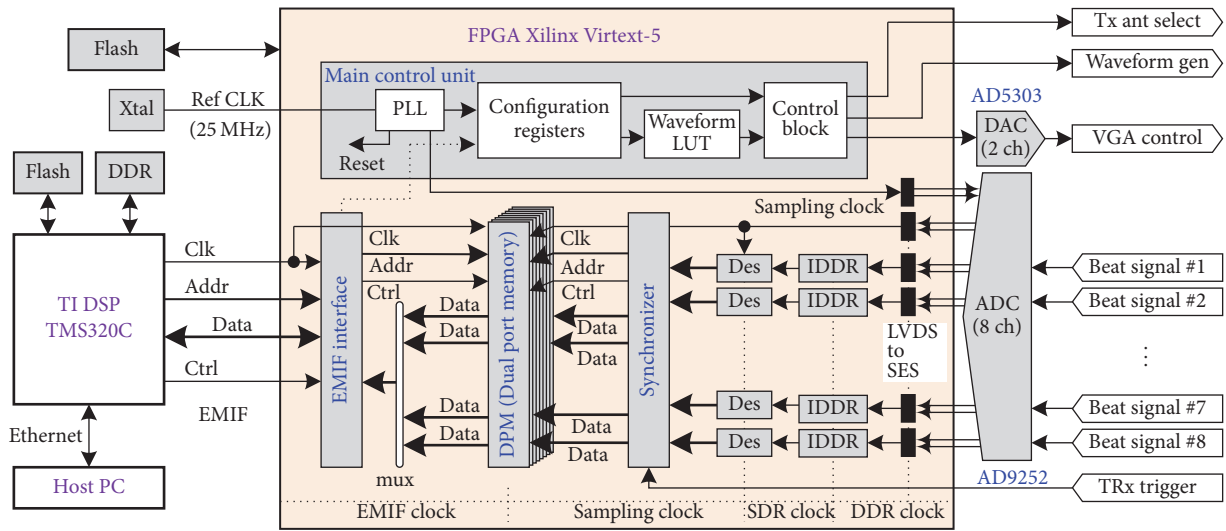
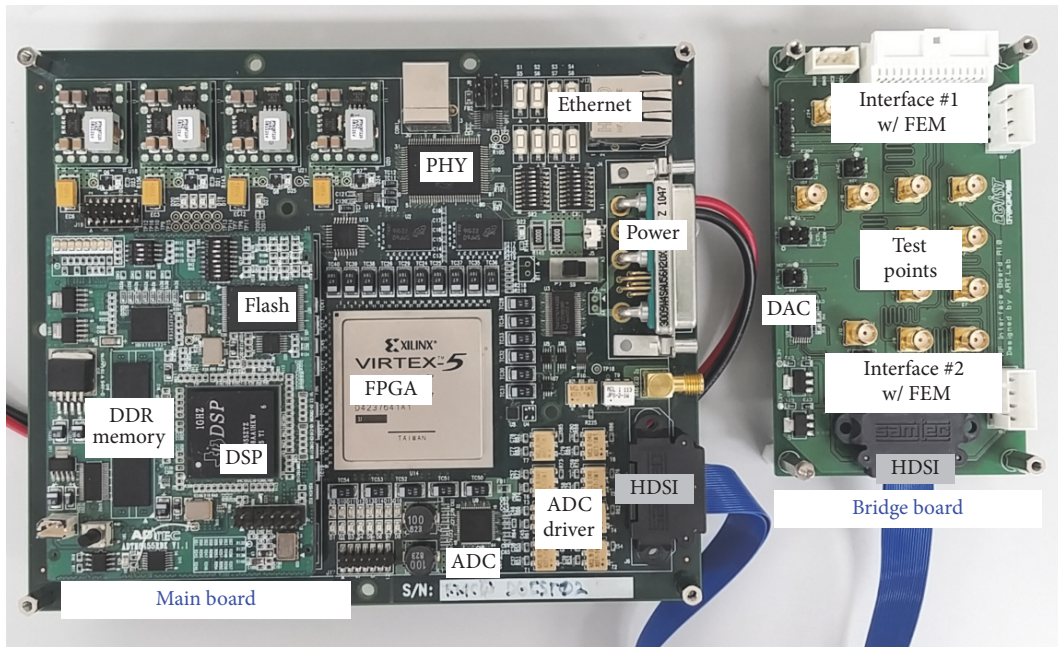FIGURE 5: Block diagram of the radar back-end module to control the reconfigurable baseband of the front-end module.

FIGURE 6: Photograph of the radar back-end module to control the reconfigurable baseband of the front-end module (main board size: $180 * 150\,mm^2$, bridge board size: $70 * 120\,mm^2$).

new one that can work with the interfaces of other radar transceivers.

2.3. Target Detection Algorithm. The target detection algorithms, based on the fast-ramp based FMCW radar scheme, are presented in Figure 8. In this paper, all algorithms were implemented on the host PC using Matlab instead of a DSP.

The algorithms consist of range-FFT, Doppler-FFT, DBF (Digital Beam Forming), and thresholding functions.

In each channel, 2D FFT processing is conducted for a 2D range-Doppler map. First, in range-FFT processing, the received beat signal in the domain is transformed using the FFT into the frequency domain within each ramp and every channel. Next, for the Doppler-FFT step, the target Doppler-frequency spectrum is also estimated using FFT processing together inside the single range-bin and over a sequence of adjacent ramp signals in the ramp-index direction. The procedure is repeated for all channels. Next, the DBF process completes the range-Doppler-angle 3D cube. That is, using the data of the same single range-Doppler cell over all channels, DBF is conducted through FFT. Finally, the thresholding block determines whether each cell of the 3D cube is a target or clutter. The details are described in earlier work [13–15].
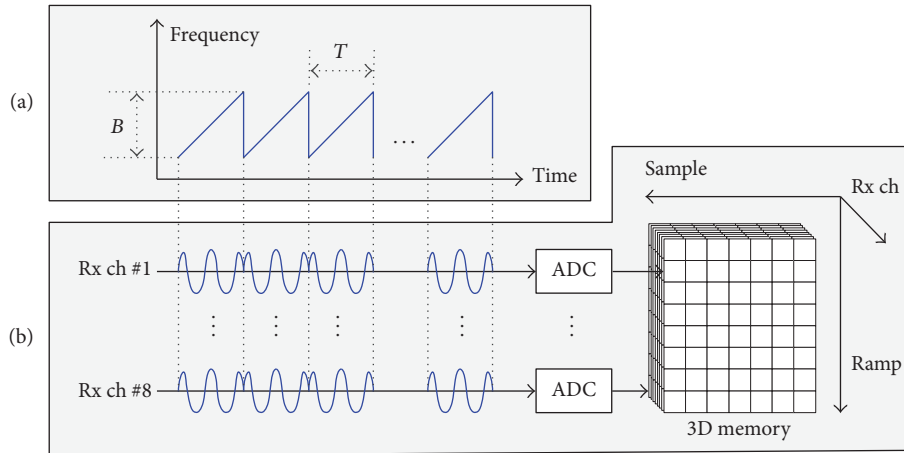
FIGURE 7: Basic concept of the fast-ramp based FMCW radar: (a) transmitted signal in the frequency-time domains and (b) the received signals on eight channels and the structure of the 3D memory.
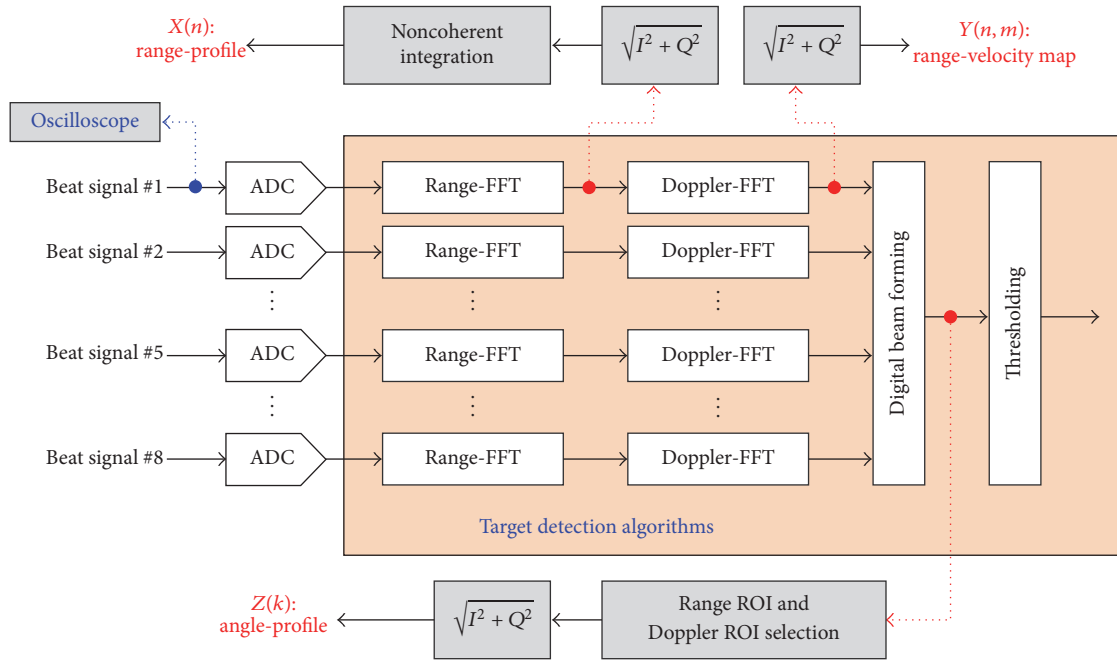

FIGURE 8: Block diagram of the target detection algorithms and monitoring methods.

In this paper, in order to monitor the performance of the developed radar effectively, we inserted monitoring points into each algorithm step with a corresponding measurement method. In addition, we captured the received beat signal on the first channel using oscilloscope before the ADC sampling step.

First, to monitor range-profile $X(n)$ in the first channel, absolute and noncoherent integration processes over several ramps are carried out after range-FFT processing. Here, $n = 1 \sim N$ denotes the range-bin index.

Next, to obtain the range-Doppler map $Y(n, m)$ in the first channel, we calculate the magnitude using the range-FFT and Doppler-FFT processing results, where $m = 1 \sim M$ is the Doppler-bin index.

Last, to analyze the angle-profile $Z(k)$ on the range-bin and Doppler-bin occupied by a target, we select both the range and Doppler ROIs (Regions Of Interest) and extract the angle-profile. Here, $k = 1 \sim K$ is the angle-bin index. In this paper, K is 16 because a 16-point DBF is employed.

In the 2D FFT algorithm using the fast-ramp based FMCW, the maximum detectable velocity ($V_{\max}$) is inversely proportional to the modulation period (T), as given in the equation $V_{\max} = c/4f_cT$. Here, c is the light velocity and f_c is the center frequency. For example, when T is 80 us, 200 us, 400 us, and 800 us, $V_{\max}$ is estimated as 140.63 km/h,
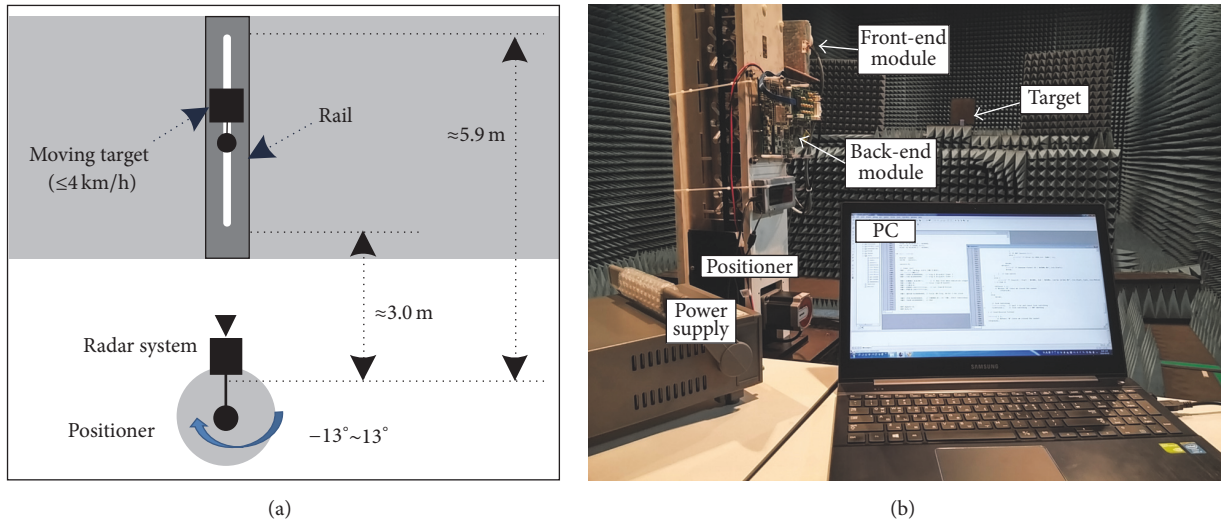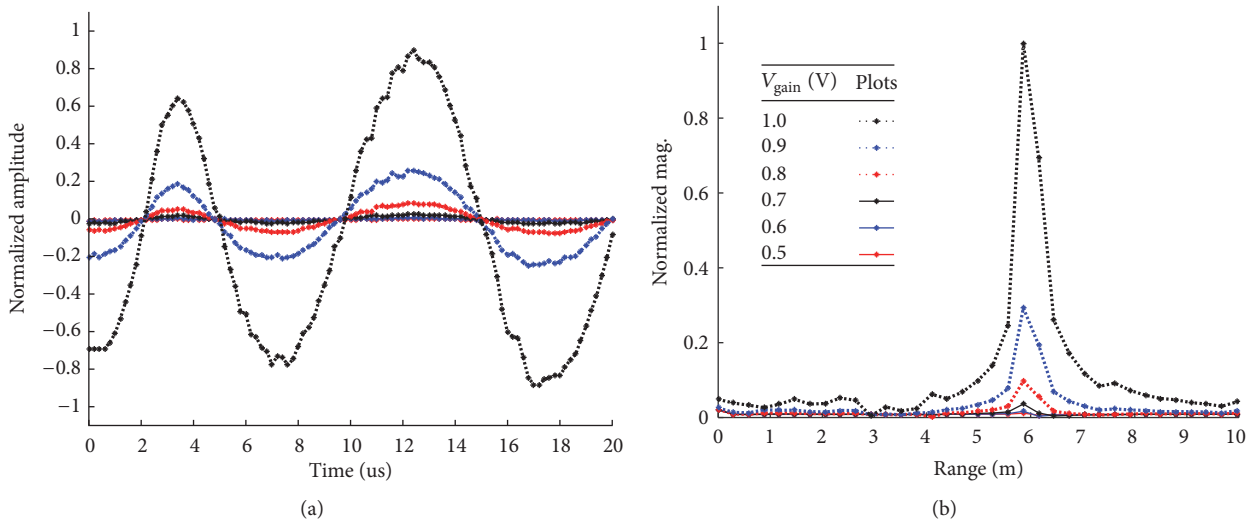
FIGURE 10: Measurement results based on various VGA gains when T = 200 us and B = 500 MHz: (a) beat signals on receive channel #1 and (b) the range-profiles.

56.25 km/h, 28.13 km/h, and 14.06 km/h. Thus, T should be selected based on the applications.

If a target is moving with speed more than V_{max}, the detected target velocity is not correct due to aliasing. In order to resolve this problem, a tracking algorithm is typically used as postprocessing. However, a description of this method is beyond the scope of this paper.

3. Experimental Results

To verify the developed radar system, we configured a measurement set-up in an anechoic chamber located at DGIST in Korea, as shown in Figure 9. The developed radar system was installed on a positioner. A single target (size: 30 cm by 30 cm) can move on a rail between 3 m and 5.9 m at less than

4 km/h. In addition, we can assess the detection of the target angle by varying the installation angle from −13° to 13°.

First, we measured the range-profile $X(n)$ of the first channel by varying the VGA input voltage from 1.0 V to 0.5 V at an increment of 0.1 V. In this VGA, the input voltages 1.0 V and 0.5 V correspond to gains of −2.4 dB and 20 dB gain. For this measurement, T and B were set to 200 us and 500 MHz, respectively. Transmit antenna #1 was selected and the ADC sampling rate was 5 MHz. Here, we placed the stationary target at a distance of about 5.9 m.

In Figure 10, the digitalized samples in one ramp and one channel are 1,000 because the sampling rate is 5 MHz and the modulation period is 200 us. Thus, these samples were transferred into the range frequency domain using 1024-point FFT processing at every ramp and channel.
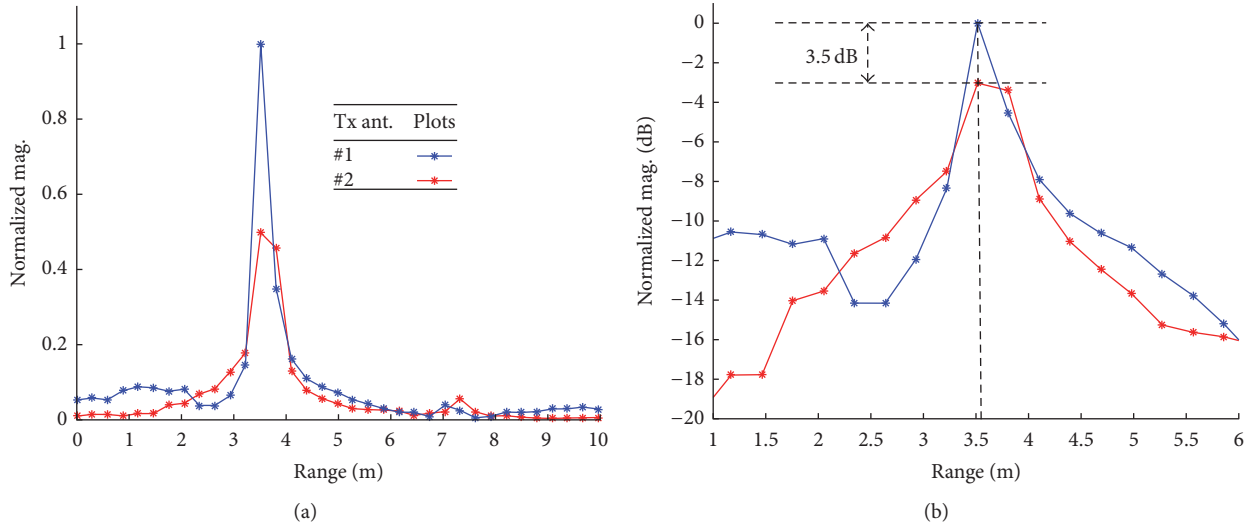
FIGURE 11: Measurement results when the two transmit antennas are selected. Here, T = 200 us and B = 500 MHz: (a) range-profiles received on channel #1 and (b) range-profile on the dB scale.

Figure 10(a) shows the amplitude of the received beat signals in the time domain. Here, to easily monitor the beat signal in the time domain, we show the signal results over a 20 us zoomed section from a full period (200 us). Next, Figure 10(b) presents the range-profiles, where the x-axis is the range (meters) and the y-axis is the normalized magnitude. From the experimental results, we find that the received signal amplitudes change based on the VGA gain.

Second, we measured the target detection performance based on the selection of the two transmit antennas. Here, T and B are set as in the first experiment, the VGA input is 0.5 V, and the ADC sampling rate is 5 MHz. The stationary target used in this case is located at a distance of approximately 3.5 m. For the purpose of investigating the gain between two Tx antennas, we measured the range-profile in the same test environment including the hardware set-up. We also apply the same parameters in the signal processing algorithm.

Figure 11(a) shows the range-profile of receive channel #1, where the x-axis is the range (meters) and the y-axis is the normalized magnitude. In Figure 11(b), the magnitude is expressed on the dB scale. Here, this signal processing result of an echo signal shows a gain difference of nearly 3.5 dB between the two antennas, while difference of 5 dB was noted in the antenna measurement, as shown in Table 1.

Next, we measured target detections based on waveforms with four combinations of T and B: 80 us, 200 MHz, 200 us, 500 MHz, 400 us, 1 GHz, and 800 us, 2 GHz. Here, the VGA gain input is 0.5 V, transmit antenna #1 is selected, and the ADC sampling rate is set to 5 MHz.

Figure 12 shows the range-profiles using actual data reflected from approximately 3 m. In this case, Figures 12(a)–12(d) show the captured oscilloscope images containing the "*TRx Trigger*" signal and beat signals for every combination. We can confirm the modulation period based on the time division of the captured image.

Figure 12(e) shows the results of the range-FFT processing step. At a narrow bandwidth of 200 MHz, the range frequency spectrum was broadened despite the fact that a zero-padding FFT was processed (see the red-dashed graph). Therefore, for high range resolution, given that a sufficient number of actual data samples are needed, frequency modulation with wide bandwidth is required (see the solid blue line).

Next, we measured target detection by the radar system while varying the installed angles at −13°, −12°, −10°, −8°, −6°, −4°, −2°, 0°, 2°, 4°, 6°, 8°, 10°, 12°, and 13°. Here, the measurement set-up matches that of the second experiment.

Figure 13(a) shows the measured angle-profile spectra $Z(k)$ according to each target angle position of −13°, −6°, 0°, 6°, and 13°. Here, the x-axis is the angle (degree) and the y-axis is the normalized magnitude. Figure 13(b) presents the detected angles versus the actual target angle positions. Because we employed a 16-point FFT for DBF processing and given that eight receiving antennas are implemented at half-wave intervals, the measured angle resolution was approximately 7.2°.

Finally, to evaluate the detection performance of the developed radar system in a multitarget environment, we conducted experiments with two targets. One stationary target was placed at a distance of about 6 m and a single target moved on a rail between 3 m and 5.9 m at less than 4 km/h. Here, the other measurement configurations match those of the second experiment.

In Figure 14, the digitalized samples in one ramp and one channel are 1,000, and then these samples were transferred into the range frequency domain using 1024-point FFT processing for every ramp and channel. Moreover, because the number of the used ramp is 256, the Doppler spectrum was generated through 256-point FFT. Here, the maximum detectable absolute velocity is 56.25 km/h because the modulation period (T) is 200 us and the center frequency (f_c)
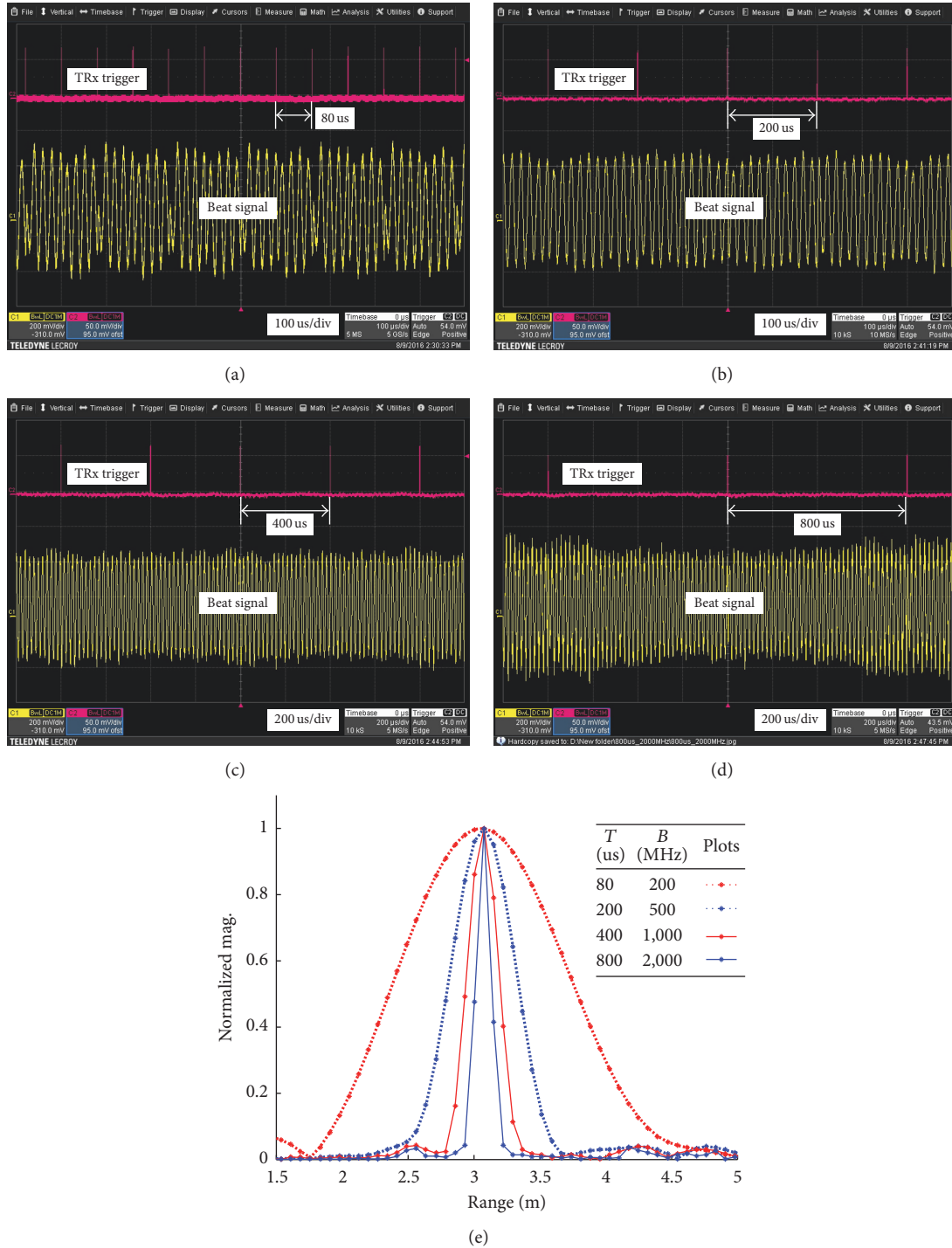
(a)

(b)

(c)

(d)

(e)

FIGURE 12: Measurement results based on the waveforms with four combinations of T and B: (a)–(d) TRx triggers and beat signals captured in an oscilloscope and (e) range-profiles.

is 24 GHz. Thus, we can detect the target velocity without aliasing.

Figure 14(a) presents the detected range-profile over 300 frames, where the x-axis is the frame number and the y-axis is the range (meters). That is, the beat signal in each frame was transformed into the range frequency spectrum using range-FFT processing, and we placed the range-profile $X(n)$ in the vertical direction over 300 frames in Figure 14(a). In the

measurement, the time interval for one frame is 0.277 sec. It was noted that one target was moving round while the other target remained at an identical distance.

Figure 14(b) shows the measured range-velocity maps at the 120th frame, where the x-axis is the range (meter) and the y-axis is the velocity (km/h). That is, the beat signal in each frame was transformed into a 2D range-velocity map $Y(n, m)$ through the range-FFT and Doppler-FFT processing.
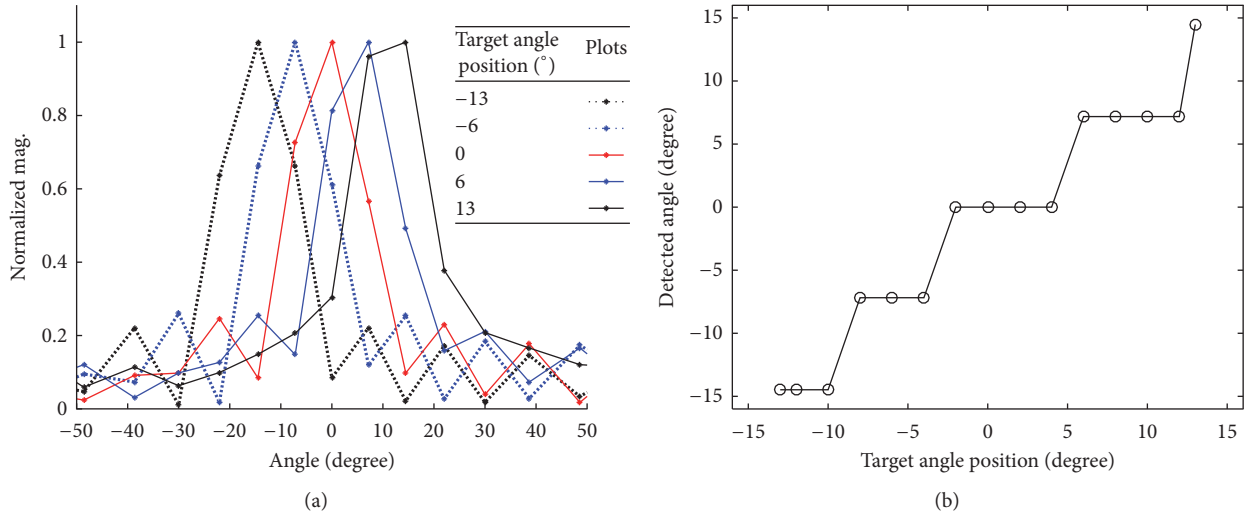
(a)

(b)

FIGURE 13: Measurement results when the target is located at various angle positions. Here, $T = 200$ us and $B = 500$ MHz: (a) angle-profiles and (b) the detected angle value versus the actual target angle position.
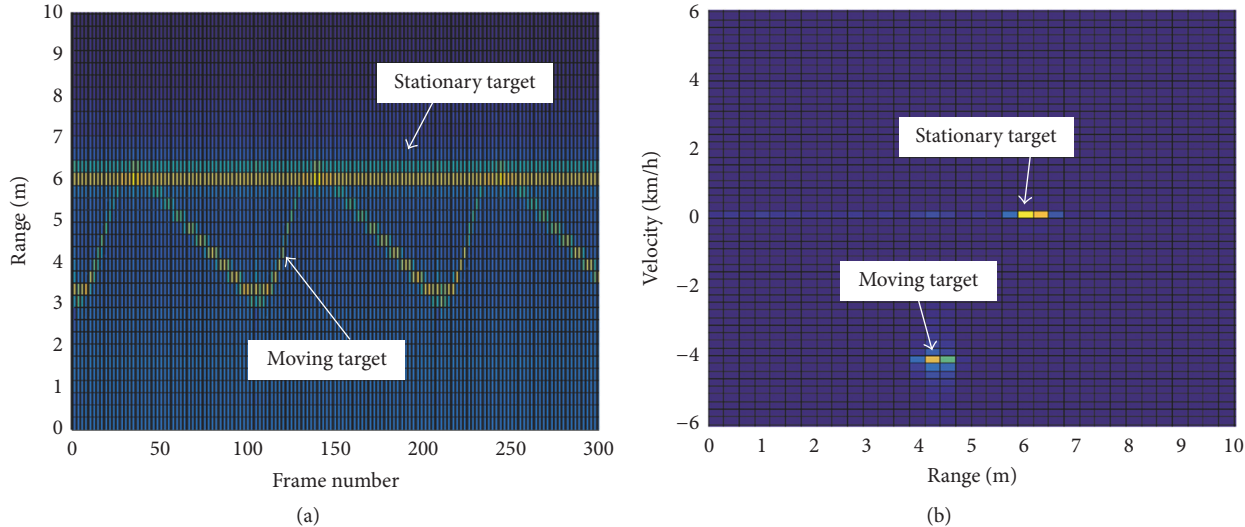

(a)

(b)

FIGURE 14: Measurement results of one stationary target and one moving target when $T = 200$ us and $B = 500$ MHz: (a) range-profile on long time term and (b) range-velocity map.

One stationary target was seen at approximately 6 m, and the moving target was seen at a speed of approximately 4 m.

4. Conclusion

In this paper, we developed a 24 GHz FMCW surveillance FMCW radar system with a software-reconfigurable baseband. The developed radar system is divided into a front-end module and back-end module. The front-end module consists of two selectable transmit antennas, eight parallel receive antennas, and a transceiver. We developed the transceiver to support various waveforms using a frequency synthesizer device, and the gain of the receive channel is controlled using a VGA device.

In the back-end module, for real-time data logging, we implemented a parallel architecture according to transmit synchronization in FPGA. In addition, the FPGA supports the functions of controlling the baseband of the transceiver. The beat signals of eight digitalized channels were transferred to a host PC, in which target detection algorithms based on 2D-FFT and DBF were processed.

To verify the developed radar system, we configured the measurement set-up in a clear chamber and carried out five experiments. First, we investigated the detection performance while setting various VGA gains. Second, we compared the range-profile when switching the two transmit antennas with difference gains. Next, based on various combinations of modulation periods and frequency bandwidths, we

confirmed the relationship between the range resolution and the bandwidth using the analysis results of the range-profile. Next, according to DBF processing results, we analyzed the angle-profile of a target located at various angle positions and confirmed the angle resolution of the developed radar system. Last, the multitarget detection performance was verified in tests involving the same chamber for each trial.

In this paper, we have tested under ideal laboratory conditions to verify the developed hardware with basic target detection algorithms. In the future, we will undertake the verification of the developed radar sensor in typical automotive conditions. To do this, instead of the basic target detection algorithm used in this paper, we will employ additional algorithms from the previous works, including those for weak target detection under a strong clutter environment [14], moving target detection [18], multitarget tracking [19], and the separate detection of moving and stationary targets. Moreover, we will carry out experiments to verify the detection performance capabilities of various surveillance applications, including pedestrian detection, automotive detection, and traffic monitoring.

Because the developed radar system supports the various radar modulations by updating the FPGA firmware software, we expect that the system will be very useful for radar research on various surveillance radar applications. On the other hand, the developed radar sensor has a disadvantage of a higher price compared to those of commercial radar systems, as a high-end FPGA and DSP, as well as an extra frequency synthesizer, were used to support its various functions. Thus, in the future, to customize the radar, we will initially replace the back-end module with a FPGA with lower specifications by optimizing the logic. Second, instead of a DSP, we will employ a microprocessor suitable for the complexity of the implemented algorithm. Finally, we will reduce the size of the back-end module by eliminating unnecessary parts and test points.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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