

Research Article

Study of the Photo- and Thermoactivation Mechanisms in Nanoscale SOI Modulator

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A new nanoscale silicon-based modulator has been investigated at different temperatures. In addition to these two advantages, nanoscale dimensions (versus MEMS temperature sensors) and integrated silicon-based material (versus polymers), the third novelty of such optoelectronic device is that it can be activated as a Silicon-On-Insulator Photoactivated Modulator (SOIPAM) or as a Silicon-On-Insulator Thermoactivated Modulator (SOITAM). In this work, static and time dependent temperature effects on the current have been investigated. The aim of the time dependent temperature simulation was to set a temporal pulse and to check, for given dimensions, how much time would it take for the temperature profile and for the change in the electrons' concentration to come back to the steady state. Assuring that the thermal response is fast enough, the device can be operated as a modulator via thermal stimulation or, on the other hand, can be used as thermal sensor/imager. We present here the design, simulation, and model of the second generation which seems capable of speeding up the processing capabilities. This novel device can serve as a building block towards the development of optical/thermal data processing while breaking through the way to all optic processors based on silicon chips that are fabricated via typical microelectronics fabrication process.

1. Introduction

1.1. Silicon-Based Devices for Optoelectronic Modulation. Nanoscale silicon-based optoelectronic devices are under investigation and development for more than two decades. The interest for coupling both electronic and optic behaviors is very high, since such devices can be integrated in a smooth way inside the circuits of the existing microelectronics industry [1–3]. The constantly growing use of real time computing generates constant urge for much faster processors than those which are currently available in the market. Correspondingly there is an accelerated development of new optics communication related applications and components. The effort to combine those two trends leads to the generation of new optoelectronic nanodevices. Such hybrid devices may allow high operation speed, reduced cross talk and other noises, and low operation power and obviate the need for the existing electrooptical convertors.

The need for nanoscales devices, coupling both electrical and optical properties, is constantly growing; in particular the need to develop silicon photonics capabilities towards future optical communication between blocks and chips is more than desirable. In this perspective, several types of hybrid devices are developed. Part of them are light emitting devices when the activation is electrical, for example, electroluminescence based devices [4–6], and part are receptor devices [7–10] such as the SOIPAM nanoscale improved device, in which the modulation control command is optic, as previously reported [11–13]. Additional investigations and simulations brought some breakthrough in this modulator, when it appears that thermal activation is also possible. We present here a dual-mode device: SOITAM (Silicon-On-Insulator Thermoactivated Modulator) and SOIPAM (Silicon-On-Insulator Photoactivated Modulator), as, respectively, presented in Figures 1 and 2.

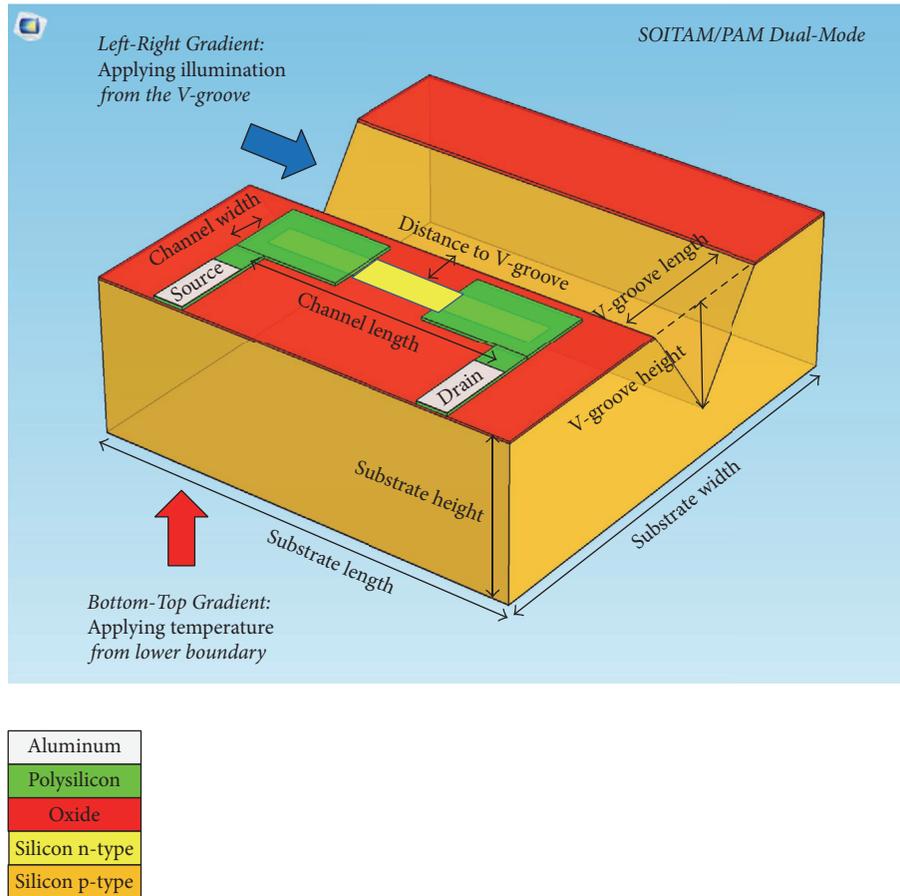


FIGURE 1: Comsol 3D simulated cross-view of the SOITAM device functionality, showing the direction of the illumination and temperature gradients of the dual-mode activation. Scales are summarized in Table 1 for the three generations.

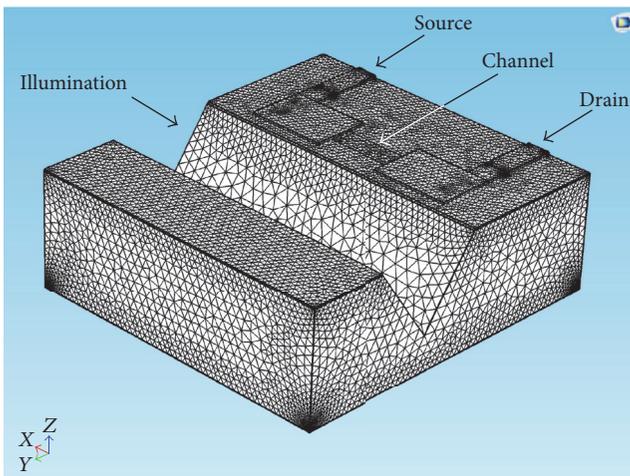


FIGURE 2: Comsol 3D simulated cross-view of the SOITAM device showing the complexity of the mesh accuracy.

1.2. From SOIPAM to SOITAM: Three Device Generations. As summarized in Table 1, first generation (micrometric) [10, 11] and second generation (nanometric) [12, 13] of the SOIPAM

have been reported. In these generations, the semiconductor device is controlled by light. The device is expected to overcome the speed barrier of currently existing silicon-based technology. Like in a MOSFET, the information current is passing through a silicon channel limited by two ports (source and drain). The novelty of the device is that the control command that opens/closes the n-type silicon channel is performed through external illumination and not by an electrical voltage. Thus the device's time response can be reduced since the semiconductor RC time constant limitation is no longer relevant [14]. The basic limitation in the time response of the proposed device is related to the drift velocity of the free carriers and the photogeneration rate in silicon. The scaling to nanoscale is the main issue to improve the operation frequency of such devices to allow operational rates of several tens of GHz. Moreover, the fast drift motion of the photogenerated free carriers in the silicon (relative to diffusive motion) will contribute to enhance the modulation rate as explained below. A third generation, this time thermoactivated (SOITAM) derived from the nanometric device, is presented for the first time in this article (Table 1).

If thermoactivated devices have been recently studied [15, 16], most of them were not silicon-based and cannot be integrated in a smooth way into the silicon microelectronics

TABLE 1: Comparison between nanometric and micrometric devices.

Parameter	SOIPAM Microdevice 1st generation	SOIPAM/TAM Nanodevice 2nd generation	SOITAM Nanodevice 3rd generation
Substrate width	20 μm	20 μm	250 nm
Substrate length	28 μm	28 μm	65 nm
Substrate height	10 μm	10 μm	100 nm
V-groove length	10 μm	10 μm	100 nm
V-groove height	7.06 μm	7.06 μm	70 nm
BOX thickness	150 nm	150 nm	30 nm
Channel thickness t	30 nm	30 nm	30 nm
Channel length L	18 μm	300 nm	45 nm
Channel width W	2 μm	2 μm	22 nm

standard industry. Other studies related to silicon starting material, involving piezo sensitive MEMS structures [17, 18], were not found relevant for nanotechnology applications. Additional studies of CMOS and MEMS based on SOI (Silicon-On-Insulator) wafers have been published [19–26]. Some recent studies mentioned the check list of possible silicon diode temperature sensor applications [27]. Such diodes can be used for temperature sensing due to the strong temperature dependence of their forward bias voltage drop. Many different semiconductor materials have been reported in literature for diode temperature sensors (silicon, germanium, and selenium are some examples). There are clear benefits of silicon-based sensors [27, 28] such as low cost, chip integration, and low degradation related to self-heat failure mechanism [29].

There is today some benefit to develop such SOITAM thermoactivated nanoscale device. One possible application would be to use it in an electrical stabilizing circuit: In regular electrical circuit, while operating, the devices are self-heating. Here we can, in a controlled way, generate an optical beam which will cancel the thermal drifts, so it can be used as a device in the control loop. The advantage of such device, when compared to other existing sensors, is its thermal responsivity, so we checked if the sensitivity is indeed higher in respect to conventional thermoresistor. Moreover, the geometrical dimensions of the device (V-groove) make it a better modulator because of the enhanced thermal responsivity and because of the more compact coupling of the control light.

1.3. Physical Concept of Operation. Starting from a SOI material, our SOIPAM device is similar to an inverted MOSFET transistor but the modulation of the drain current is achieved via a modulated illumination of the substrate rather than a classic gate voltage modulation. The channel consists of a 30 nm thick n-type silicon channel contacted to source and drain terminals and insulated from the substrate by a 150 nm thick buried oxide layer. Since the n-type doping level (N_d donors' concentration is 10^{17} cm^{-3}) of the channel is designed to be larger than the p-type substrate (N_a acceptors' concentration is 10^{15} cm^{-3}), the thickness of the depletion

layer in the n-type area is narrower than the depletion layer in the p-type region. Moreover, the device is designed in such a way that, in dark conditions, the depletion layer in the channel is smaller than the channel thickness so the device is partially depleted and can be considered as normally, that is, moderately conducting under dark condition and zero gate voltage. The operation modes of the second generation device are presented for illustration in Figures 3–5 for the three main steps.

A negative gate potential V_{GS} is applied to the bottom side of the p-type silicon substrate such that a negatively charged depletion layer appears under the buried oxide layer. Consequently, a positively charged depletion layer appears inside the n-type channel upon the buried oxide. The channel thickness and the doping of the p and n regions are designed so the channel is still partially depleted in such conditions. In dark condition, an inversion electrons layer would be built-up under the buried oxide by thermal generation and then enlarge the positive depletion layer in the n-type region and eventually close the channel. A solution to avoid the thermal generation consists in applying a rapid modulation of the gate potential V_{GS} to keep p-type area in deep depletion. By synchronously illuminating the p-type area through a 10 μm depth V-groove (being etched deep inside the substrate and close to channel), free photogenerated electrons concentration can significantly be increased until the inversion state is reached. As a result, the n-type channel will be fully depleted so the drain current decreases significantly. In this article we add the thermal influence on above described mechanisms.

2. Optothermoelectrical Simulations

2.1. Steady State versus Nonequilibrium Deep Depletion. It must be emphasized that the foregoing discussion describes the transient state of deep depletion of the p-type substrate. The nonequilibrium dynamics of this state are at the heart of the previous models and investigations. In the current study the semiconductor dynamics, described by the drift-diffusion-Poisson equations, were assumed to be in a steady state at any given time. The difference between the two regimes is the following: in the deep depletion regime, the potential drop on the device is quickly increased by applying

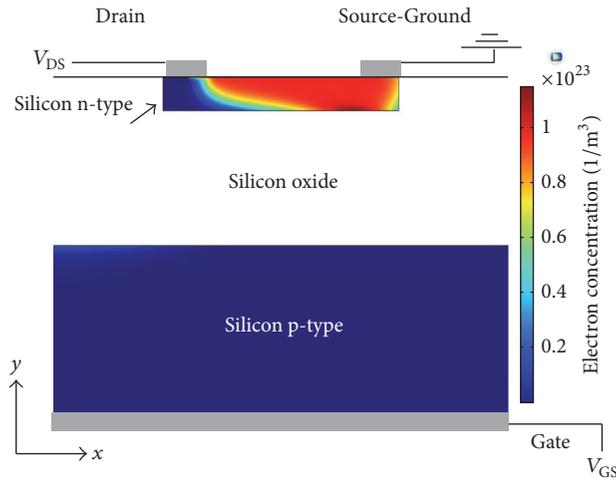


FIGURE 3: Comsol 2D cross-view of the device at equilibrium. No applied voltage or illumination. N-type channel is normally open. Here $V_{GS} = 0$ V.

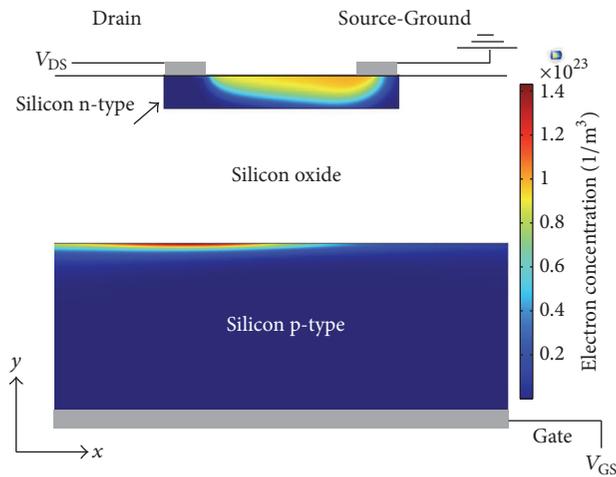


FIGURE 4: Comsol 2D cross-view of the SOIPAM device's operation mode. Applying gate voltage closes the channel partially. Here $V_{GS} < 0$, $V_{DS} > 0$ V.

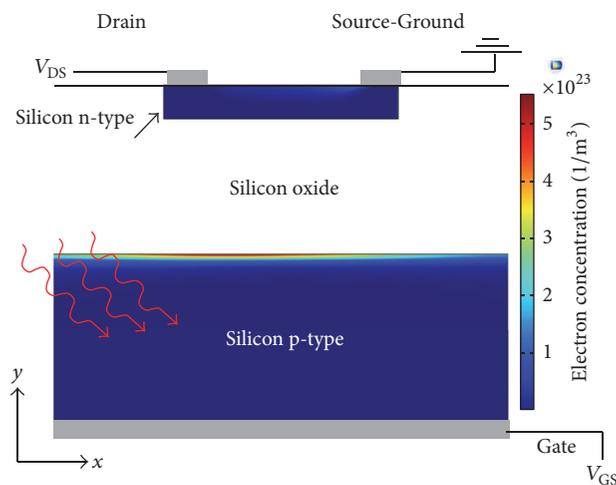


FIGURE 5: Comsol 2D cross-view of the SOIPAM device's operation mode. Applying illumination with the gate voltage closes the channel completely. Here $V_{GS} < 0$, $V_{DS} > 0$ V, and $\lambda = 550$ nm.

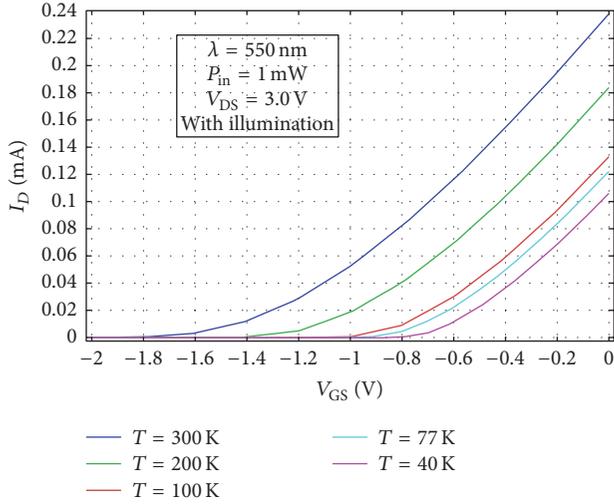


FIGURE 6: Numerical simulations showing the drain current as a function of the gate voltage V_{GS} for several temperatures values ($V_{DS} = 3.0$ V, $P_{in} = 1$ mW).

a negative voltage pulse at the gate, greater than the substrate threshold voltage for inversion. If thermal generation cannot react fast enough to provide charge for an inversion layer, the potential drop then falls mainly on the bulk (body). This leads to a depletion layer and surface potential (depletion potential) larger than the equilibrium values. The system now has a propensity to return to the equilibrium value, by creating an inversion layer at the expense of the superdepleted region beneath. If carriers are now generated by illumination they can accumulate below the buried oxide and form an inversion layer. The inversion charge thus serves as a “photon counter,” increasing with the number of photons absorbed. A constant flux of photons will result in accrued charge of quantity proportional to the time of exposure. We thus obtain the time-integration familiar from CCD-cameras and gated-arrays. Similarly, with the passage of time, thermal generation acts to create inversion charge and return equilibrium. This is the familiar “dark current” noise which increases with time, eventually reaching saturation.

By contrast, in the steady state the quantity of inversion charge device reacts not to the number of photons accrued, but to their rate of absorption. This is the behavior familiar from devices such as photodiodes, phototransistors, and photoresistors, whose output measures the instantaneous radiation flux. In this study, transient thermal dynamics were included, investigated, and coupled to steady-state behavior on the part of the semiconductor.

2.2. Temperature Influence on Current, for Fixed Illumination.

As part of the temperature influence investigations transfer curves (Figure 6) have been simulated at temperatures varying from 40 K to 300 K. The illumination of the device (e.g., photoactivation) was kept fixed at visible wavelength of 550 nm. It appears that the applied temperature influences the threshold voltage. As presented, the higher the temperature, the higher the device measured current.

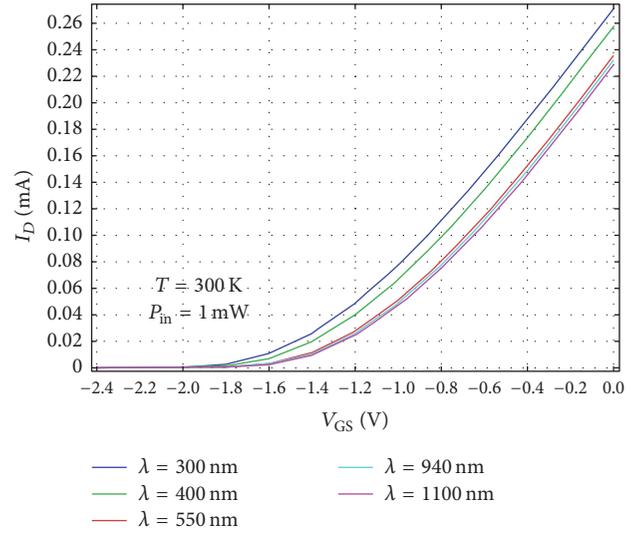


FIGURE 7: Drain induced current numerical simulations as a function of the gate voltage V_{GS} for several wavelengths. $T = 300$ K, $P_{in} = 1$ mW, $V_{DS} = 3$ V.

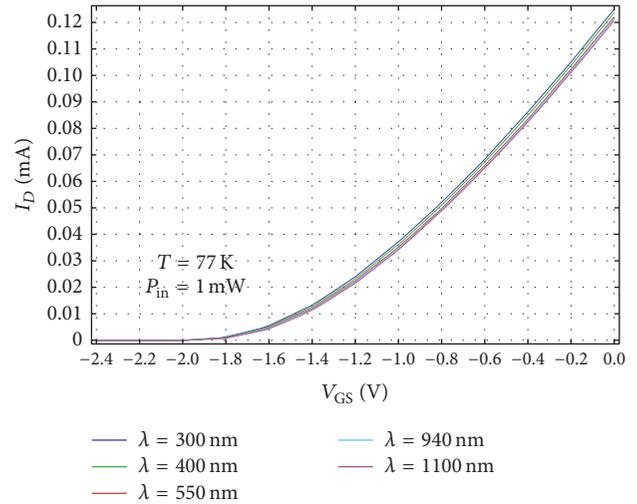


FIGURE 8: Drain induced current numerical simulations as a function of the gate voltage V_{GS} for several wavelengths. $T = 77$ K, $P_{in} = 1$ mW, $V_{DS} = 3$ V.

2.3. Wavelength Influence on the Current Sensitivity to Temperature (CST). Another interesting aspect was to check the temperature influence on the drain current for several wavelengths. In Figures 7 and 8, we present a series of simulations of the drain induced current versus gate voltage by varying the wavelength from visible to near infrared (NIR). In both the cases of the temperature, respectively, 300 K and 77 K, the optical power remains constant ($P_{in} = 1$ mW), at a given $V_{DS} = 3$ V.

At 300 K, the decrease of the drain current is noticeable by increasing the illumination wavelength till 550 nm (Figure 10). However, at 77 K, the decrease of the drain current is negligible by increasing the illumination wavelength. This

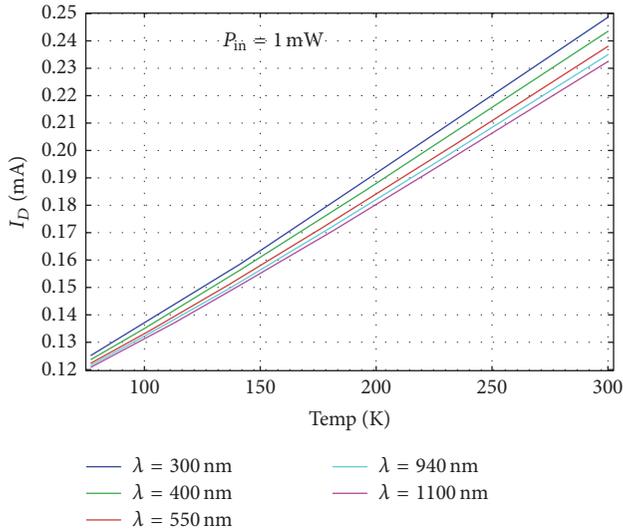


FIGURE 9: Numerical simulation of the current as a function of the temperature for several illumination wavelengths. $P_{in} = 1 \text{ mW}$, $V_{DS} = 3 \text{ V}$, $V_{GS} = 0 \text{ V}$.

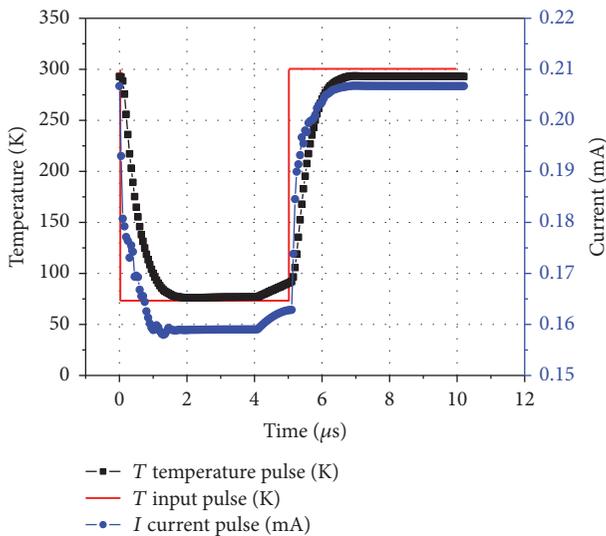


FIGURE 10: Numerical simulation of the 77 K pulse. Initial temperature = 300 K. At $t = 0$, a 77 K pulse is applied. After approximately $2 \mu\text{s}$ the device is stabilized. At $t = 5 \mu\text{s}$ the temperature that is being applied is going back to room temperature. Drain current is simulated for $V_{DS} = 3 \text{ V}$, $V_{GS} = 0 \text{ V}$.

behavior is expected since the light absorption, and so the carriers generation process, is increasing within the silicon substrate at shorter wavelength. If, at room temperature, we can observe a series of separated transfer curves as a function of the wavelength (Figure 7), at low temperature all the curves are now matching (Figure 8). As seen in Figure 9, the drain current variation (under constant illumination power) is increasing linearly with the temperature. Then the slope dI/dT which we define as the Current Sensitivity to Temperature (CST) slightly increases with shorter wavelengths and its value is about $440 \pm 10 \text{ nA/K}$ in the 77–300 K range.

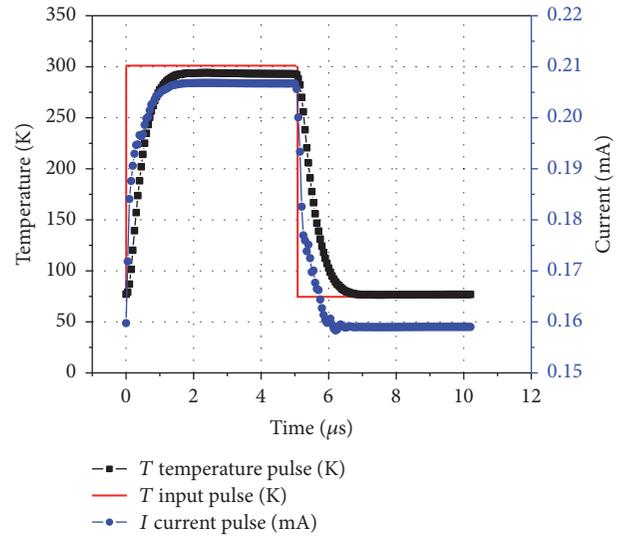


FIGURE 11: Numerical simulations of the 300 K pulse. Initial temperature = 77 K. At $t = 0$, a 300 K pulse is applied. After approximately $2 \mu\text{s}$ the device is stabilized. At $t = 5 \mu\text{s}$ the temperature that is being applied is going back to low temperature. Drain current is simulated for $V_{DS} = 3 \text{ V}$, $V_{GS} = 0 \text{ V}$.

2.4. Temperature Pulses towards Sensor Functionality Check. The next step was to check sensitivity for larger range of temperatures and as a consequence to enable 300 K to 77 K (Figure 10) and 77 K to 300 K (Figure 11) fast transitions using thermal pulse simulations. In Figure 10, the initial temperature is 300 K. At $t = 0 \mu\text{s}$, a 77 K pulse is applied. After approximately $2 \mu\text{s}$ the temperature is stabilized at the top of the device structure. Then, at $t = 5 \mu\text{s}$, the temperature which has been applied is set back to room temperature. In Figure 11, the initial temperature is 77 K. At $t = 0 \mu\text{s}$, a 300 K pulse is applied. This time again, after approximately $2 \mu\text{s}$ the device is stabilized. Then, at $t = 5 \mu\text{s}$ the applied temperature is going back to low temperature. The CST is found to be $(\pm 250 \text{ nA/K})$.

3. Discussion

3.1. Temperature Sensitivity of the Drain Current. The first result pointed out from the simulation results is that the thermal sensitivity of the device (variation of the drain current per Kelvin) is increased by decreasing the illumination wavelength in the 77 K to 300 K domain (Figure 9). We present here an explanation of this phenomenon. Generally speaking, the temperature dependence on the photocurrent can be traced to several phenomena including (1) the general temperature dependence of electronic transport, that is, the mobility, in the bulk and in the channel, (2) the temperature dependence of the Band to Band absorption, in particular the temperature dependence of the band gap, (3) the increase of available carriers with temperature characteristic of semiconductors, and (4) the temperature dependence of the inversion layer created under the bulk as a result of photogeneration of hole-electron pairs.

The carrier population in the channel indeed increases with temperature so that the resistance decreases leading to a current increase. Indeed, $1/\rho \cong q(n_e\mu_e + n_h\mu_h)$, where ρ is the resistivity, q is the unit of electric charge, n_e and n_h are the electron and hole densities, respectively, and μ_e and μ_h are their corresponding mobilities. However the channel is a majority carrier device, essentially a one-sided MESFET (see below). Hence, the electron population is essentially fixed at the donor impurity density $n_e \cong N_d \gg n_h$, with only a negligible temperature dependence in the 130–500 K range. Below 130 K dopant freeze-out becomes significant [30]; however the possibility of incomplete donor and acceptor ionization was included in the simulation. However, in this case, the temperature dependence of the electron concentration n_e should be exponential. But as depicted in Figure 9, the drain current linearly increases with the temperature. We must look deeper then to find the cause of this temperature dependence above 130 K as presented in the discussion part.

3.2. MOS-Cap-in-MESFET Model. To understand the SOITAM in general and in particular the temperature dependence of the drain current, it is helpful to model the device as a MESFET device (since the drain/source contacts to the N-channel are made of N+ polysilicon), with a MOS capacitor embedded in the gate located at the backside. For reminder, the MESFET controls the top silicon n-type channel current through a buried oxide (BOX) layer on a p-doped substrate, acting as the back gate terminal. It is important to note that, in this device, the only gate is located at the backside and is connected to the backside contact; there is no top gate (see Figure 1).

Then, for a given drain and gate voltages, the drain current at any point x along the channel can be described by the following equation [31]:

$$I_D(x, T) \sim qn_e W(x, T) = N_d \left(W_0 - \sqrt{2\epsilon\epsilon_0 \frac{V_{COx}(x, T)}{qN_d}} \right), \quad (1)$$

where W_0 is the total channel thickness at equilibrium (no voltage applied), while the square root term describes the width W_C of depletion layer; the latter is obviously dependent on V_{COx} , the potential difference between the channel (at the x point) and the BOX layer (which depends on temperature). To arrive at the source of the temperature dependence of the current photosensitivity, then, we must investigate how V_{COx} changes in response to wavelength illumination and the possibility of temperature dependence therein.

The channel depletion is usually determined by a negative V_{GC} , the Gate-to-Channel voltage drop; the larger V_{GC} is, the more the channel is constricted. However, the SOIPAM differs from a MESFET, in that the channel depletion is not controlled by V_{GC} alone, but also via external optical excitation.

Although the total V_{GC} is controlled externally, part of it falls on the MESFET, part on the BOX, and part on the substrate. The apportionment of the total voltage drop V_{GC} amongst the different regions can be understood similarly to

that in a MOS capacitor: initially most of V_{GC} falls on the substrate, creating a depletion layer. Approaching a threshold value V_T , an inversion layer is formed directly below the BOX and screens the depletion layer of the substrate. The surface potential, that is, the potential drop on the depletion layer φ_{dep} or φ_B (“B” is for “Body”), becomes “pinned” at approximately the value $\varphi_{dep,0} \sim 2(E_F - E_i)/q$, where E_F is the Fermi level of the bulk p-type silicon substrate, while E_i is the intrinsic Fermi level which almost linearly depends on the temperature [31]. Further increase of V_{GC} leads to little increase in φ_{dep} ; instead, incremental contributions to V_{GC} now accrue primarily on the BOX and the MESFET channel above it.

3.3. Photoexcitation. In order to detect photoexcitation, V_{GC} is first tuned to the threshold value V_T , such that φ_{dep} takes on the critical value, just below the onset of inversion; this is the strong inversion regime of the substrate. Note that if V_{GC} is applied steeply the substrate reaches the “deep depletion” mode so the inversion layer cannot be longer generated by thermal activation. The introduction of photoexcitation now serves to increase the available minority carriers, augmenting the inversion layer and shifting more of the voltage drop to the BOX and the embedded MESFET. The channel thus constricts incrementally, and I_{DS} drops accordingly. In fact, as Figure 9 displays other factors overcome this trend, so that the current in fact increases with temperature. As we shall see however, a nonlinear interaction exists between the temperature dependence and the contribution of photoexcitation to the inversion layer, such that the latter increases together with the temperature. We will carry out the analysis as for a MOS capacitor; that is, we will regard the BOX layer as the dielectric material, leading to the capacitance C_{OX} . Our goal is to determine the change in the Channel-Oxide voltage drop, δV_{COx} , resulting from increasing the intensity of illumination, and then study its temperature dependence. We will make use of charge conservation to argue that, just as in a parallel-plate capacitor, the depletion charge of the channel, above the BOX, equals the total charge, from depletion and inversion, below the BOX: $Q_C = q_{inv} + Q_{dep}$. Including the value of the pinned surface potential will lead to the desired result.

3.4. Voltage Drop and Temperature Dependence. To begin the analysis we decompose the total and constant gate voltage drop, V_{GC} , into several contributions: (1) V_{FB} , the flat-band voltage drop arising from the difference in Fermi level between the n-doped MESFET channel and the p-type substrate which is assumed constant with temperature, (2) V_{COx} , the potential difference between the channel and the BOX alluded to previously, (3) ΔV , the capacitive voltage drop on the BOX, and (4) φ_{dep} , the voltage drop through the depletion region of the substrate. Additional contributions are due to surface states and trapped impurities but are fixed relative to photoexcitation and hence may be ignored. Consequently for a given point x along the channel, we have

$$-V_{GC} = V_{FB} + V_{COx} + \Delta V + \varphi_{dep}. \quad (2)$$

For the sake of clarity, explicit reference to x has been suppressed here and in the foregoing discussion. For $|V_{GC}| \geq V_T$, the strong inversion regime, the inversion layer screens the substrate, and the substrate depletion voltage φ_{dep} . In our conditions this occurs at zero gate voltage since our device is “normally” open.

The voltage drop across the channel V_{COx} arises from the channel depletion layer. Integrating Poisson's equation across the width of the depletion region, W_C gives

$$V_{\text{COx}} = \frac{1}{2} \frac{qN_d}{\epsilon\epsilon_0} W_C^2. \quad (3)$$

The effective channel depletion surface charge density is temperature dependent and related to the channel width via

$$Q_C = qN_d W_C. \quad (4)$$

We may thus express V_{COx} as

$$V_{\text{COx}} = \frac{Q_C^2}{\alpha'^2}, \quad (5)$$

where

$$\alpha' \equiv \sqrt{2q\epsilon\epsilon_0 N_d}, \quad (6)$$

and ϵ and ϵ_0 are the dielectric constant (relative permittivity) of silicon and the vacuum permittivity, respectively.

More familiar relation is given by

$$Q_C = \alpha' \sqrt{V_{\text{COx}}} = \sqrt{2q\epsilon\epsilon_0 N_d V_{\text{COx}}}. \quad (7)$$

(1) φ_{dep} . The analysis of the substrate depletion voltage parallels that for the channel. As mentioned above, φ_{dep} , which is temperature dependent, is given by

$$\varphi_{\text{dep}} = \frac{Q_B^2}{\alpha^2} \quad (8)$$

with

$$\alpha \equiv \sqrt{2q\epsilon\epsilon_0 N_a}. \quad (9)$$

The surface charge density of the depleted body is then

$$|Q_B| = \sqrt{2q\epsilon\epsilon_0 N_a \varphi_{\text{dep}}} = \alpha \sqrt{\varphi_{\text{dep}}} \sim \alpha \sqrt{\frac{2(E_F - E_i)}{q}}. \quad (10)$$

(2) ΔV . Next, the capacitance voltage drop across the BOX layer, ΔV , arising from the accumulated charge on either side of the effective oxide region should be constant at charge equilibrium. This surface charge may be decomposed into two components; one is the charge of the depletion region within the substrate Q_B ; the other is the inversion layer, which behaves effectively as a surface charge, q_{inv} . Hence:

$$\Delta V = \frac{q_{\text{inv}} + Q_B}{C_{\text{ox}}} = \frac{Q_C}{C_{\text{ox}}}, \quad (11)$$

where

$$C_{\text{ox}} = \frac{\epsilon_{\text{SiO}_2} \epsilon_0}{t_{\text{BOX}}} \quad (12)$$

is the capacitance of the BOX per unit area, and t_{BOX} is its thickness. Consequently, V_{COx} is temperature dependent as Q_B .

3.5. *Modeling the Wavelength Dependence on CST.* We now aim to assess the wavelength dependence of the CST. For this purpose the effect of photogeneration is modeled as a perturbation of the inversion charge, and hence we write

$$q_{\text{inv}} \longrightarrow q_{\text{inv}} + \delta q_L, \quad (13)$$

where δq_L is the photo-induced perturbation presenting the inversion charge variation δq_{inv} induced by the wavelength illumination λ .

Let us first explain the current dependence on the wavelength. In fact, δq_L is proportional to G_L , the photogeneration rate per unit area. Such photogeneration rate is wavelength dependent through the absorption coefficient γ since $G_L \propto e^{-\gamma x}$, where $\gamma \propto (E_{\text{ph}} - E_g)^2$ for an indirect band gap (energy E_g) with photon energy $E_{\text{ph}} = hc/\lambda$ [32]. So G_L is increasing with lambda increasing, and then δq_L . Consequently, the drain current is decreasing with lambda increasing.

Now, let us determine the temperature dependence of the drain current derivative $\delta I/\delta q_{\text{inv}}$ taken as a measurement of the device wavelength sensitivity.

As mentioned above, the inversion charge layer screens the substrate. The incremental change in the inversion charge δq_{inv} thus shifts some of the voltage drop to the oxide and to the channel, reducing the substrate voltage drop φ_{dep} and in turn reducing the depletion charge Q_B . To express this quantitatively we can use (11) to write:

$$\delta \Delta V = \frac{\delta q_{\text{inv}} + \delta Q_B}{C_{\text{ox}}}. \quad (14)$$

It follows from the neutrality condition (12) that the change in q_{inv} and Q_B implies a change in the channel depletion charge,

$$\delta Q_C = \delta q_{\text{inv}} + \delta Q_B. \quad (15)$$

The change in the channel potential drop is by

$$\delta V_{\text{COx}} = \frac{2Q_C}{\alpha'^2} \delta Q_C. \quad (16)$$

Similarly the change in the substrate surface potential is found via (8):

$$\delta \varphi_{\text{dep}} = \frac{2Q_B}{\alpha^2} \delta Q_B. \quad (17)$$

So we can finally find the relation between δq_{inv} on the one hand and δQ_B and hence $\delta \varphi_{\text{dep}}$ on the other.

We may now proceed to find the relation between δq_{inv} on the one hand and δQ_C on the other. The total Gate-Channel

voltage drop is set externally and is thus unaffected by the incident radiation, so from (2) we can write

$$\delta V_{GC} = \delta V_{FB} + \delta V_{COx} + \delta \Delta V + \delta \varphi_{dep} = 0. \quad (18)$$

Since the flat-band voltage V_{FB} is an intrinsic property of the materials in the device it too is unaffected by the illumination, $\delta V_{FB} = 0$, and we thus obtain

$$\delta V_{COx} + \delta \Delta V + \delta \varphi_{dep} = 0. \quad (19)$$

Next we express each of the contributions to (19) in terms of Q_C . Equations (14) and (8) lead to

$$\delta \Delta V = \frac{\delta Q_C}{C_{ox}} \quad (20)$$

and from (17) we get

$$\delta \varphi_{dep} = \frac{2}{\alpha^2} (\delta Q_C - \delta q_{inv}). \quad (21)$$

Inserting these into (18) together with (16) we obtain

$$\frac{2Q_C}{\alpha'^2} \delta Q_C + \frac{\delta Q_C}{C_{ox}} + \frac{2Q_B}{\alpha^2} (\delta Q_C - \delta q_{inv}) = 0. \quad (22)$$

Gathering terms gives

$$\left(\frac{2Q_C}{\alpha'^2} + \frac{1}{C_{ox}} + \frac{2Q_B}{\alpha^2} \right) \delta Q_C = \frac{2Q_B}{\alpha^2} \delta q_{inv}. \quad (23)$$

We thus find the following relation between δQ_C and δq_{inv} :

$$\delta Q_C = \frac{(2/\alpha^2) Q_B}{(2Q_C/\alpha'^2 + 1/C_{ox} + 2Q_B/\alpha^2)} \delta q_{inv}. \quad (24)$$

Before proceeding to analyze the influence on the current, and thence to considerations of temperature, it is physically instructive to consider once again the perturbation to the substrate surface potential. Substituting (24) into (21) and into (16) gives, respectively,

$$\delta \varphi_{dep} = -\frac{(2Q_B/\alpha^2)(2Q_C/\alpha'^2 + 1/C_{ox})}{(2Q_C/\alpha'^2 + 1/C_{ox} + 2Q_B/\alpha^2)} \delta q_{inv}, \quad (25)$$

$$\delta V_{COx} = \frac{2Q_C}{\alpha'^2} \frac{(2/\alpha^2) Q_B}{(2Q_C/\alpha'^2 + 1/C_{ox} + 2Q_B/\alpha^2)} \delta q_{inv}. \quad (26)$$

The increment to the inversion charge due to the incident radiation reduces the depletion voltage and hence the depletion charge in the substrate. Consequently, the depletion charge in the channel increases according to (24) and constricts the channel, and the drain current is reduced as we now elaborate.

The illumination is directed to the substrate region; hence one may assume that it does not directly influence the channel current density. However the disturbance in the charge density will lead to a redistribution of the charge and

electric potential. The change in the current may be using the same technique as in the unperturbed case:

$$\delta I = \frac{\mu_e d}{L} \int_{-V_{GS}}^{-V_{GS}+V_{DS}} \delta Q_C(V(x)) dV. \quad (27)$$

(Recall that this represents a positive contribution to a *negative* current, so that the magnitude decreases.) Substituting (24) for δQ_C leads to

$$\delta I = \frac{\mu_e d}{L} \cdot \delta q_{inv} \int_{-V_{GS}}^{-V_{GS}+V_{DS}} \frac{(2/\alpha^2) Q_B(V)}{(2Q_C(V)/\alpha'^2 + 1/C_{ox} + 2Q_B(V)/\alpha^2)} dV. \quad (28)$$

The sensitivity of the channel current to an increase of illumination induced charge can thus be expressed as

$$\frac{\delta I}{\delta q_{inv}} = \frac{\mu_e d}{L} \cdot \int_{-V_{GS}}^{-V_{GS}+V_{DS}} \frac{(2/\alpha^2) Q_B(V)}{(2Q_C(V)/\alpha'^2 + 1/C_{ox} + 2Q_B(V)/\alpha^2)} dV. \quad (29)$$

The variation in current is positive, but the current as defined is negative, so the current magnitude decreases with illumination, as expected. In principle to investigate the temperature dependence of the wavelength current sensitivity (29) we must consider the two cases of depletion and inversion and insert the appropriate forms for Q_C and Q_B ; into these one substitutes the temperature dependence of $\varphi_{dep,0}(T)$ as well. We will suffice here with a few general comments.

(1) Under depletion $Q_B = Q_C$ so (24) and (29) are, respectively,

$$\delta Q_C = \frac{(2/\alpha^2) Q_C}{((2/\alpha'^2 + 2/\alpha^2) Q_C + 1/C_{ox})} \delta q_{inv}, \quad (30)$$

$$\frac{\delta I}{\delta q_{inv}} = \frac{\mu_e d}{L} \int_{-V_{GS}}^{-V_{GS}+V_{DS}} \frac{(2/\alpha^2) Q_C}{((2/\alpha'^2 + 2/\alpha^2) Q_C + 1/C_{ox})} dV. \quad (31)$$

With increasing temperature Q_C decreases, albeit mildly, and so the drain current decreases as well.

(2) Under inversion, $Q_B = \alpha \sqrt{\varphi_{dep,0}}$; hence

$$\frac{\delta I}{\delta q_{inv}} = \frac{\mu_e d}{L} \cdot \int_{-V_{GS}}^{-V_{GS}+V_{DS}} \frac{(2/\alpha) \sqrt{\varphi_{dep,0}}}{(2Q_C(V)/\alpha'^2 + 1/C_{ox} + (2/\alpha) \sqrt{\varphi_{dep,0}})} dV. \quad (32)$$

With increasing temperature, $\varphi_{dep,0}$ in the numerator decreases, while Q_C in the denominator increases, and so the photosensitivity decreases with temperature under inversion too.

We have presented here a mathematical model for the behavior of the SOIPAM device as observed in numerical simulation. The degree of correspondence between this analytic model and the presented simulation results is of interest. In particular we focused on the decrease of the sensitivity with temperature as calculated from (29) and (32). In general utilization of the model to devise a way to enhance the sensitivity of the device to temperature and/or illumination is of prime importance in continuing work.

4. Conclusion

The proof of concept of a new dual-mode, photo- and thermoactivated, silicon nanoscale device has been presented. The SOITAM presents a lot of advantages, such as (1) nanoscale dimensions versus regular MEMS temperature sensors, (2) silicon-based material versus polymers for chip integration, (3) dual-mode versus single mode, (4) low cost, (5) high sensitivity, and (6) low degradation related to self-heat failure mechanism. These advantages enable the device to become a building block and to serve in an electrical stabilizing circuit. If a first generation of devices was successfully fabricated and tested, second and third generations of devices, sharing nanoscale dimensions, have been largely designed and simulated. Using Comsol and Matlab software modules, a series of electrooptical and electrothermal simulations have been performed, in order to evaluate the induced current as a function of several parameters, such as the illumination wavelength (λ), the illumination power (P_{in}), in the device structure, and the temperature sensitivity versus pulses. The first opto- and thermoelectronic characterizations and simulations are encouraging and match the expected physical model. Efforts should be now concentrated in order to optimize the device in order to achieve higher rate of operation and better sensitivity, prior to future fabrication of this third generation.

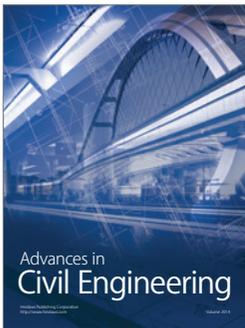
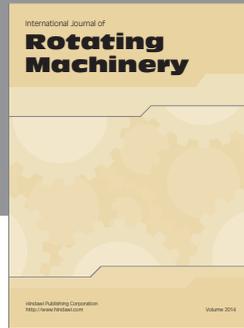
Competing Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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