Hindawi
Journal of Sensors
Volume 2018, Article ID 6436481, 10 pages
https://doi.org/10.1155/2018/6436481

Research Article

A One-Dimensional Magnetic Chip with a Hybrid Magnetosensor and a Readout Circuit

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Received 11 August 2017; Revised 25 November 2017; Accepted 5 December 2017; Published 25 March 2018

Academic Editor: Lucio Pancheri

This work presents a one-dimensional magnetic chip composed of a hybrid magnetosensor and a readout circuit, which were fabricated with 0.18 μm 1P6M CMOS technology. The proposed magnetosensor includes a polysilicon cross-shaped Hall plate and two separated metal-oxide semiconductor field-effect transistors (MOSFETs) to sense the magnetic induction perpendicular to the chip surface. The readout circuit, which comprises a current-to-voltage converter, a low-pass filter, and an instrumentation amplifier, is designed to amplify the output Hall voltage with a gain of 43 dB. Furthermore, a SPICE macro model is proposed to predict the sensor's performance in advance and to ensure sufficient comprehension of the magnetic mechanism of the proposed magnetosensor. Both simulated and measured results verify the correctness and flexibility of the proposed SPICE macro model. Measurements reveal that the maximum output Hall voltage V_{H}, the optimum current-related magnetosensitivity S_{RI}, the optimum voltage-related magnetosensitivity S_{RV}, the averaged nonlinearity error NLE, and the relative bias current I_{bias} are 4.381 mV, 520.5 V/A·T, 40.04 V/V·T, 7.19%, and 200 μA, respectively, for the proposed 1-D magnetic chip with a readout circuit of 43 dB. The averaged NLE is small at high magnetic inductions of ±30 mT, whereas it is large at low magnetic inductions of ±30 G.

1. Introduction

The Hall plate is a type of a CMOS magnetic induction sensor that can sense the magnetic induction perpendicular to the sensor plate surface and convert it into a corresponding electrical signal such as voltage, current, or frequency [1–3]. That is, the CMOS Hall sensor can be used in output of either voltage (voltage mode) or current (current mode). In both modes, sensitivity and offset are valuable features for evaluating the performance of the Hall sensor [4]. Various techniques have been developed to improve these characteristics based on conventional voltage-mode Hall sensors [5–8]. Voltage-mode Hall sensors have dominated most applications for many years [2, 4]. A cross-shaped Hall plate (CSHP) is a widely used Hall sensor that uses a Wheatstone bridge topology [1]. However, the Hall plate achieves lower voltage-related magnetosensitivity than the magnetotransistor or the MAGFET [9] does. To enhance magnetosensitivity, the hybrid magnetosensor has been developed to have a large output Hall current, which is the drain current of MOSFET whose gate is biased with a polysilicon CSHP in voltage mode. Notably, the magnetosensitivity is enhanced because the drain current of MOSFET is a quadratic equation of the induced Hall voltage at a gate terminal and because the offset is effectively eliminated with an instrumentation amplifier (IA).

The split-drain MAGFET is used as a Hall sensor by sensing the magnetic induction perpendicular to the MAGFET plane, in which a current difference is obtained between two adjacent drains of the MAGFET [10]. The relative sensitivity depends on the primary geometric parameters and biasing conditions of the applied device [11, 12]. Among all the proposed shapes in [10], measurements show that the sectorial structure with two 90° lobes exhibits the most sensitivity with respect to the magnetic induction. That is, a symmetrical and differential structure enables favorable sensitivity. In addition to the geometric parameters, the biasing condition should be considered. As shown in [13], the strip

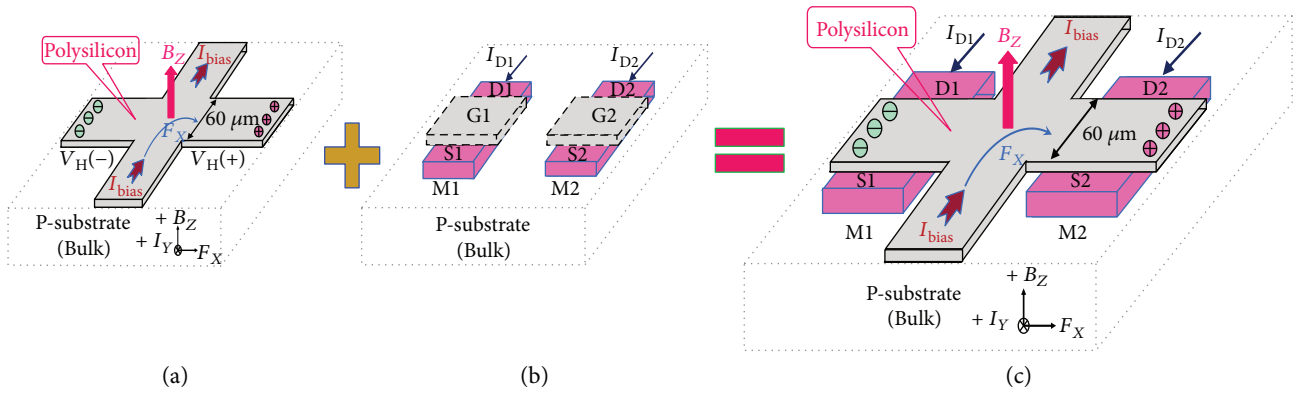

FIGURE 1: The proposed 1-D hybrid magnetosensor in which the B_Z is the magnetic induction perpendicular to the chip surface, I_{bias} is the bias current in the y-direction, and F_X is the Lorentz force in the x-direction. (a) Polysilicon CSHP, (b) two identical MOSFETs, M1 and M2, and (c) detailed topology.

approach can carry the biasing current up to 500 mA, whereas the biasing current in the coil approach is limited to 20 mA. The biasing current of the strip MAGFET with two sources is superior to that of the MAGFET with a shared source [14]. Additionally, an obvious advantage to the operation of CMOS systems is that thermal noise is reduced [11], whereas the flicker noise remains fairly temperature independent [15]. This paper proposes a hybrid magnetosensor composed of a polysilicon CSHP and a pair of identical MOSFETs. The MOSFET enhances the magnetic sensitivity with a quadratic equation of the induced Hall voltage at the polysilicon CSHP, and the strip structure with two separated sources improves the biasing current.

Additionally, this paper proposes a SPICE macro model that is suitable for detecting the magnetic induction in voltage mode [16, 17]. Both simulated and measured results are provided to verify the correctness and flexibility of the proposed SPICE macro model. The rest of this paper is organized as follows: Section 2 describes the operational principles of the proposed topology of the 1-D hybrid magnetosensor and its SPICE macro model. Section 3 presents the readout circuit for the magnetosensor. Section 4 provides simulated and measured results of the magnetic chip. Section 5 presents the discussion and the conclusions.

2. Operational Principle of the Hybrid Magnetosensor

Figure 1 presents the proposed 1-D hybrid magnetosensor, which is composed of a polysilicon CSHP as shown in Figure 1(a) and a pair of identical MOSFETs, M1 and M2, as shown in Figure 1(b), to sense the magnetic induction B_Z perpendicular to the chip surface. Here, I_{bias} is the biasing current in the y-direction and F_X is the Lorentz force in the x-direction. The polysilicon CSHP is located on M1 and M2 to establish a hybrid magnetosensor, which is a magnetically coupled current sensor using CMOS split-drain transistors with a high biasing current [13]. In the absence of the applied magnetic induction B_Z, two output currents, I_{D1} and I_{D2}, are the same at D1 and D2 of MOSFETs M1 and M2, respectively. After passing through the readout circuit, the output voltage V_{OUT} of the IA is constant. That is, $\Delta V_{OUT} = 0$. In contrast to $B_Z = 0$, the output voltage V_{OUT} is a function of the bias current I_{bias} with respect to the applied magnetic induction B_Z.

As shown in Figure 1(a), a magnetic induction B_Z and a bias current I_{bias} are applied to the polysilicon CSHP and the positive and negative Hall voltages, $V_H(+)$ and $V_H(-)$, are induced by a Lorentz force F_X in the x-direction. After putting the polysilicon CSHP on the two identical MOSFETs as shown in Figure 1(c), two drain currents, I_{D1} and I_{D2}, can be expressed by grounding two sources, S1 and S2. That is,

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[(V_{GS} + V_H(-)) - V_{TH}\right]^2,$$
$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[(V_{GS} + V_H(+)) - V_{TH}\right]^2, \quad (1)$$

where μ_n, C_{ox}, W, L, and V_{TH} are the electron mobility, parasitic capacitance per unit gate area, width, length, and threshold voltage, respectively. V_{GS} is the gate-to-source voltage without magnetic induction. The induced Hall voltage V_H is then derived from the Lorentz force.

$$V_H = V_H(+) - V_H(-) = \frac{GR_H I_{bias} B_Z}{t}, \quad (2)$$

where $R_H = -\mu_n^*/\sigma_n = -r_n/nq$ represents the Hall coefficient, I_{bias} is the bias current in the y-direction, B_Z is the magnetic induction in the z-direction, and t and G are the polysilicon thickness and the geometrical correction factor, respectively [18]. Thus, the current difference between I_{D1} and I_{D2} can be expressed as

$$\Delta I_D = I_{D2} - I_{D1} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(V_{GS} - V_{TH}) \times (V_H)\right]. \quad (3)$$

Rewriting (3), we have

$$\Delta I_D = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}) \times \left(\frac{GR_H I_{bias} B_Z}{t}\right). \quad (4)$$

Consequently, the current difference ΔI_D is directly proportional to the bias current I_{bias} and the magnetic induction B_Z. When the bias current is set to be constant, the larger the magnetic induction B_Z is, the higher the induced current

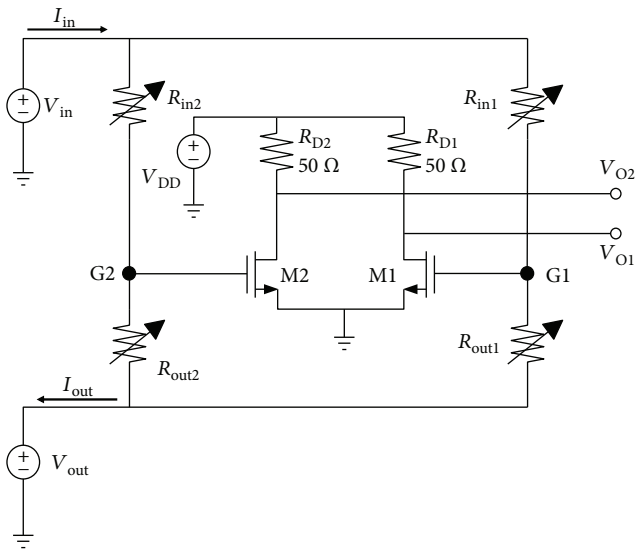

Figure 2: Macrocircuit equivalent model for the proposed 1-D hybrid magnetosensor, including a polysilicon CSHP and two identical MAGFETs.

difference ΔI_D is. A comprehensive macroanalysis is presented in Figure 2 to facilitate comprehension of the Hall effect at the proposed 1-D hybrid magnetosensor fabricated using standard 0.18 μm CMOS technology. The physical mechanism is proposed to involve the Lorentz force F_X pushing the positive charge right to gather it at the right side of the polysilicon CSHP, which is connected to the gate terminal of the second MOSFET M2. Thus, the drain current of the M2 is a quadratic equation of the induced positive Hall voltage $V_H(+)$ at the gate terminal. The magnetic sensitivity could be improved effectively. Meanwhile, the electron current is directly injected into the left side of the polysilicon CSHP, which is connected to the gate terminal of the first MOSFET M1 to reduce the drain current of the M1. The corresponding netlist file is provided in the appendix. By applying a magnetic induction B_Z (~mT), the output voltage V_{OUT} at the output of the readout circuit can be measured by multiplying the induced differential drain voltage, $V_{O1} - V_{O2}$, by 43 dB. Note that the differential drain voltage is equal to the current difference ΔI_D multiplied by the external resistor R_D (~50 Ω). In the netlist file, the voltage source V(mag_in) represents the induced Hall voltage, which is generated with the applied magnetic induction B_Z. Figure 3 shows those equivalent resistors of the proposed polysilicon CSHP. Two resistors, R_{in2} and R_{out1}, are reduced by the Lorentz force F_X which pushes those carriers to the right of the CSHP; meanwhile, R_{in1} and R_{out2} are increased with the Lorentz force.

3. Readout Circuit

Two drain currents, I_{D1} and I_{D2}, obtained at two separate drains of the MAGFET sensor over the considered magnetic induction range are of the order of a few tens of microamperes. By passing the current signal through the current-to-voltage converter (I-to-V converter) and low-pass (LP) RC filter, the high-frequency noise is filtered out before the instrumentation amplifier. Figure 4 shows the readout circuit of the proposed hybrid magnetosensor, which includes the I-to-V converter, LP filter, and instrumentation amplifier. The offset can be removed by the instrumentation amplifier, and a single output V_{OUT} is easy to use.

As shown in Figure 4, the I-to-V converter is employed to convert the induced drain current obtained from the proposed 1-D magnetosensor. Two output voltages of the I-to-V converter can be expressed as

$$\begin{aligned} V_{O1} &= I_{D1} \times R_{D1} + V_{REF1} = I_{D1} \times R_D + V_{REF1}, \\ V_{O2} &= I_{D2} \times R_{D2} + V_{REF2} = I_{D2} \times R_D + V_{REF2}, \end{aligned} \tag{5}$$

where V_{O1} and V_{O2} are the output voltages of OP1 and OP2, respectively. V_{REF1} and V_{REF2} represent the two reference voltages for adjusting the bias voltages in operational amplifiers OP1 and OP2. R_D is the drain resistor which is equal to R_{D1} and R_{D2} in Figures 2 and 4. The output voltage of the instrumentation amplifier V_{OUT} passing through the LP filter is given by

$$\begin{aligned} V_{OUT} = V_{REF3} + \left\{ [(V_{REF1} - V_{REF2}) + (I_{D1} - I_{D2})R_D] \times \frac{1}{1 + sR_2C_1} \right\} \\ \times \left(1 + 2\frac{R_A}{R_G}\right) \times \left(\frac{R_C}{R_B}\right), \end{aligned} \tag{6}$$

where V_{REF3} is a constant reference voltage, which is used to adjust the output level. For DC magnetic induction, $s = 0$; the small-signal output voltage is given by

$$v_{out} = \Delta I_D \times R_D \times \left[1 + 2\left(\frac{R_A}{R_G}\right)\right] \times \left(\frac{R_C}{R_A}\right). \tag{7}$$

Next, we address the offset voltage, which is contributed by three reference voltages, for the DC magnetic induction. That is,

$$V_{offset} = V_{REF3} + (V_{REF1} - V_{REF2}) \times \left[1 + 2\left(\frac{R_A}{R_G}\right)\right] \times \left(\frac{R_C}{R_A}\right). \tag{8}$$

Note that the voltage difference, $\Delta V_{REF} = V_{REF1} - V_{REF2}$, plays a dominant role in the offset voltage because it is amplified by $[1 + 2(R_A/R_G)] \times (R_C/R_B)$. A large offset voltage limits the output range considerably. Furthermore, the drain resistor R_D is completed with the common-centroid layout to eliminate the impact of noise, and the resistors, R_2, R_A, R_B, R_C, and R_G, and capacitor C_1 are the external components.

Figure 5 shows the folded cascode operational amplifier (op amp) with a cascode PMOS load that performs with a large differential output voltage swing, and the choice of the input common-mode level is easy [19]. The left part of Figure 5 depicts a bias circuit that is used to provide three constant bias voltages, V_1, V_2, and V_3. To obtain a single-ended output, the active PMOS load (M17–M20) can be modified (Figure 5) so that M17 and M18 are biased at the edge of the triode region. The adopted folded cascade amplifier saves one PMOS threshold voltage in the output swing [19].

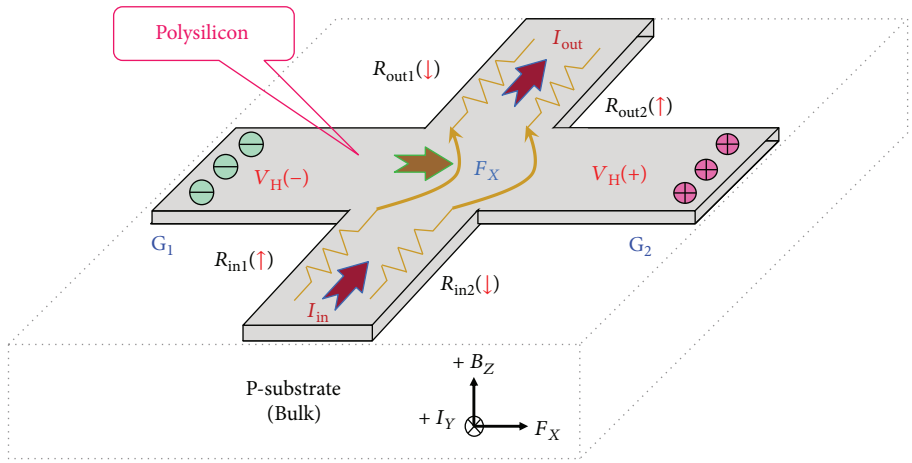

FIGURE 3: Equivalent resistors of the proposed polysilicon CSHP with the Lorentz force F_X. Two symbols, ↓ and ↑, mean decrement and increment in resistors, respectively.

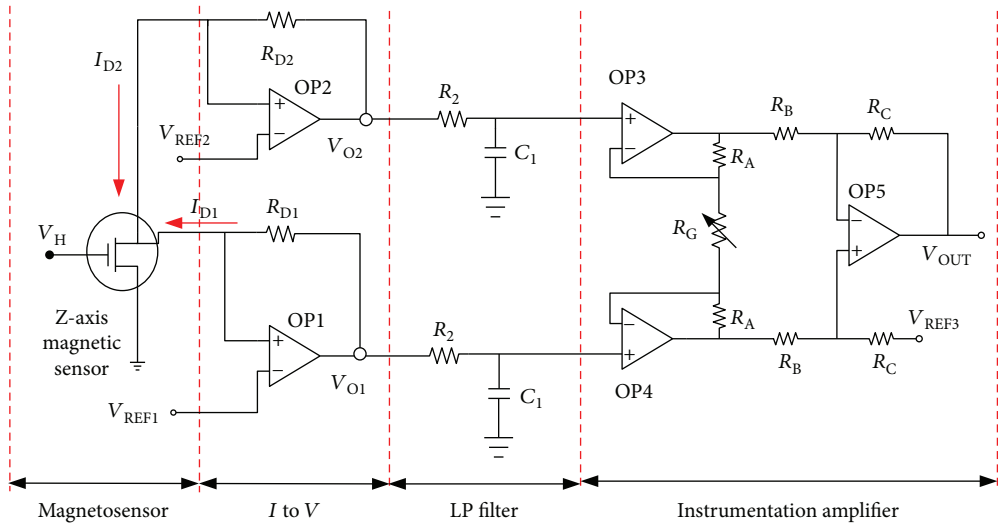

FIGURE 4: Readout circuit of the proposed 1-D hybrid magnetosensor with a readout circuit, including an I-to-V converter, LP filter, and instrumentation amplifier.

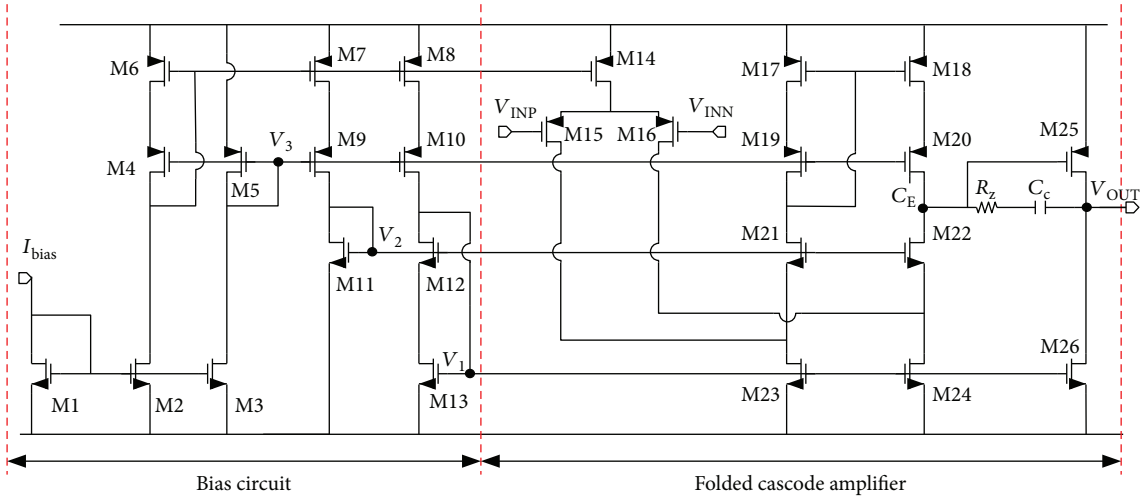

FIGURE 5: Schematic diagram of the folded cascode op amp with a cascode PMOS load, a zero-frequency modification, and a bias circuit.

As shown in Figure 5, we employ "two-stage" op amps, with the first stage providing a high gain and the second stage typically configured as a simple common-source stage to allow maximum output swings [19]. The first and second stages exhibit gains equal to A_{v1} and A_{v2}, respectively, and the swing at V_{OUT} is equal to $V_{\mathrm{DD}} - |V_{\mathrm{OD25}}| - V_{\mathrm{OD26}}$. The overall voltage gain A_v can be expressed as

$$A_{v1} \approx g_{m15}\left\{\left[\left(g_{m21}+g_{mb21}\right)r_{\mathrm{O21}}\left(r_{\mathrm{O15}}\|r_{\mathrm{O23}}\right)\right]\|\right. \left.\cdot\left[\left(g_{m19}+g_{mb19}\right)r_{\mathrm{O19}}r_{\mathrm{O17}}\right]\right\}, \quad (9)$$
$$A_{v2} \approx g_{m26}\left(r_{\mathrm{O25}}\|r_{\mathrm{O26}}\right),$$

where g_{mi}, g_{mbi}, and $r_{\mathrm{O}i}$ are the transconductance, body transconductance, and output resistance, respectively, of the ith MOSFET.

The right half plane zero is a serious concern in two-stage CMOS op amps because g_m is relatively small and the compensation capacitor C_{C} is set to be sufficiently large to position the dominant pole properly. As shown in Figure 5, the zero frequency ω_{z} can be modified by placing a resistor R_{z} in series with the compensation capacitor. The zero frequency is then given by [19]

$$\omega_{\mathrm{z}} \approx \frac{1}{C_{\mathrm{C}}\left(g_{m25}^{-1}-R_{\mathrm{z}}\right)}. \quad (10)$$

Thus, if $R_{\mathrm{z}} \geq g_{m25}^{-1}$, then $\omega_{\mathrm{z}} \leq 0$. In practice, we can move the zero well into the left half plane to cancel the first nondominant pole. This occurs if

$$\frac{1}{C_{\mathrm{C}}\left(g_{m25}^{-1}-R_{\mathrm{z}}\right)} = \frac{-g_{m25}}{C_L+C_E}. \quad (11)$$

That is,

$$R_{\mathrm{z}} = \frac{C_L+C_E+C_{\mathrm{C}}}{g_{m25}C_{\mathrm{C}}}, \quad (12)$$

where C_E denotes the capacitance at node E before C_{C} is added [19].

4. Simulated and Measured Results

In general, voltage-mode Hall devices can be biased in two modes: voltage biasing and current biasing [20]. In the current biasing mode, the current-related sensitivity S_{RI} is calculated as

$$S_{\mathrm{RI}} = \left|\frac{1}{I_{\mathrm{bias}}}\frac{\Delta V_{\mathrm{OUT}}}{\Delta B}\right|, \quad (13)$$

where the unit of S_{RI} is $\mathrm{V}\cdot\mathrm{A}^{-1}\cdot\mathrm{T}^{-1}$, I_{bias} represents the supply bias current, ΔB is the change in the applied magnetic induction, and ΔV_{OUT} is an output voltage difference of the instrumentation amplifier with and without magnetic induction B. In the voltage biasing mode, the voltage-related sensitivity S_{RV} is defined as

$$S_{\mathrm{RV}} = \left|\frac{1}{V_{\mathrm{bias}}}\frac{\Delta V_{\mathrm{OUT}}}{\Delta B}\right|, \quad (14)$$

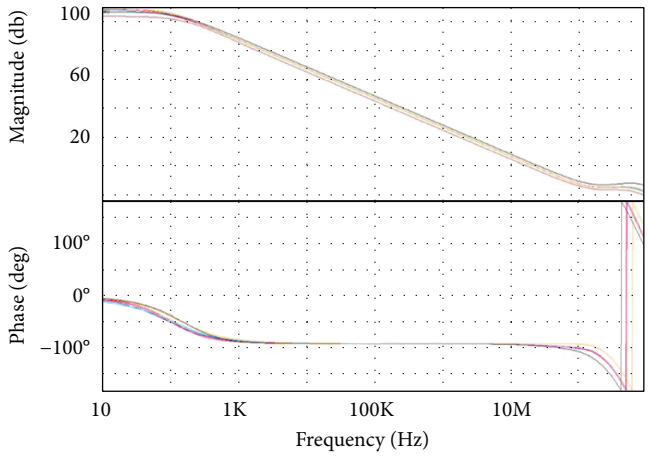

Figure 6: Simulated gain and phase variations across five designed corners versus frequency.

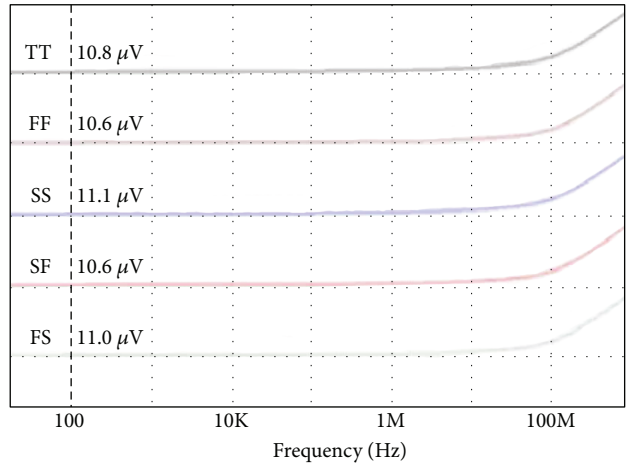

Figure 7: Simulated input-referred noises at five designed corners with respect to frequency.

Table 1: Summary of simulated input-referred noises in units of nanovolts per square root Hertz at five designed corners.

Frequencies	TT	FF	SS	SF	FS
400 kHz (nV/$\sqrt{\mathrm{Hz}}$)	17.0	16.8	17.6	16.8	17.4
1 MHz (nV/$\sqrt{\mathrm{Hz}}$)	10.8	10.6	11.1	10.6	11.0

where the unit of S_{RV} is the inverse tesla (T^{-1}) and V_{bias} is the supply bias voltage [20]. In addition, the nonlinearity error (NLE) is defined as

$$\mathrm{NLE} = \left|\frac{\Delta V_{\mathrm{OUT}} - \Delta V_{\mathrm{OUT}}^{(0)}}{\Delta V_{\mathrm{OUT}}^{(0)}}\right| \times 100\%, \quad (15)$$

where the NLE is expressed as a percentage and $\Delta V^{(0)}{}_{\mathrm{OUT}}$ is the calculated output voltage based on the slope of the straight line obtained according to the best fit to the output characteristic [20].

This study presents a high-gain, high common-mode rejection ratio (CMRR), and low-noise folded cascode op

Table 2: Comparison with previous studies of OP for simulated and measured results.

Specifications	This work		[21]	[22]	[23]
	Simulations	Measurements	Simulations	Simulations	Simulations
Technology (μm)	0.18	0.18	0.35	0.18	0.5
Voltage gain (dB)	105	71.12	89.3	67.7	45
Phase margin (°)	80	86	89.7	—	—
CMRR (dB)	110	123	136.7	92	75
Slew rate (V/μs)	2.0	2.3	—	—	—
ICMR (VPP)	2.0	1.24	—	—	—
Gain bandwidth (kHz)	1.0	1.50	0.079	1.75	5.8
UGB (MHz)	20.8	—	1.46	91.33	—
Averaged PSRR (dB)	118	123	—	—	—
Output swing (V)	1.8	1.8	—	—	—
Input-referred noise at 1 MHz (nV/Hz$^{1/2}$)	10.8	—	—	—	22
Power dissipation (mW)	0.88	0.92	0.328	0.263	0.280
Chip area of OP (mm^2)	0.0765	0.0765	—	1.49	—

Figure 8: Microphotograph of the proposed 1-D MAGFET sensor and a readout circuit without external resistors and capacitors.

amp fabricated using 0.18 μm CMOS technology for magnetic measurements. By employing the folded cascode architecture and common-mode feedback at the output, a substantial improvement was achieved in the gain and the CMRR [21]. Furthermore, a low-noise amplifier was achieved by using a differential pair and minifying the transistor size [19]. The designed folded op amp has a gain of 105 dB, phase margin of 80°, CMRR of 110 dB, slew rate of 2.0 V/μs, input common-mode range (ICMR) of 2.0 V, gain bandwidth of 1 kΩ, averaged power supply rejection ratio (PSRR) of 118 dB, output swing of 1.8 V, input-referred noise of 10.8 nV/$\sqrt{\text{Hz}}$ at 1 MHz, power consumption of 0.88 mW at a power supply of 1.8 V, and load capacitance of 10 pF in the TT design corner. Figure 6 shows the simulated AC analysis of the op amp circuit along with the phase response in five design corners exhibiting a DC voltage gain of 105 dB and a phase margin of 80° in the TT corner. The variations of simulated voltage gain and phase margin are small. Figure 7 shows the simulated input-referred noises at five design corners with respect to frequency. Table 1 summarizes the simulated input-referred noises at five design corners with respect to two frequencies: 400 kHz and 1 MHz. The op amp exhibits low noise in the FF design corner but high noise in the SS design corner. Note that the optimum representative frequency is about 1 MHz due to the gain bandwidth of 1 kHz in Table 2.

The simulated and measured results are tabulated in Table 2, and a comparison with previous studies was conducted. The simulated results such as the voltage gain, CMRR, slew rate, ICMR, gain bandwidth, PSRR, output swing, and input-referred noise are superior to those of [21–23]. The measured data verify that the designed op amp operates correctly even though the aforementioned studies have yet to prove so. Figure 8 shows the microphotograph of the proposed magnetic chip without external resistors and capacitors, which was fabricated in a 0.18 μm CMOS process. A voltage gain of 43 dB is always required for the instrumentation amplifier, whose OPs are completed with the same folded cascade topology. Figure 9 shows the magnetic induction generator that is used to generate 1-D magnetic induction B_Z.

As presented in [24], the measured Hall current is evident when the bias current I_{bias} is greater than 100 μA for the four-folded vertical Hall device. Thus, the bias current was set to 100, 200, and 300 μA in both simulation and measurement. According to the proposed SPICE model shown in the appendix, the simulated output Hall voltages are presented (Figure 10; dashed lines) as a function of the different biasing currents, from 100 μA to 300 μA in steps of 100 μA, at different magnetic inductions, from −30 mT to 30 mT in steps of 5 mT. The measured output Hall voltages are plotted using symbols denoting the three bias conditions. As shown in Figure 10, the measured data closely match the simulation data. Both the simulated and measured results were obtained with the readout circuit for the proposed magnetic chip.

After the proposed SPICE model was verified with the measurements, low magnetic induction was considered to find the minimum resolution with good linearity [25, 26]. Figure 11 shows the simulated output voltages (dashed lines) and measured output voltages (mark symbols) as a function of applied magnetic induction, from −30 G to 30 G in steps

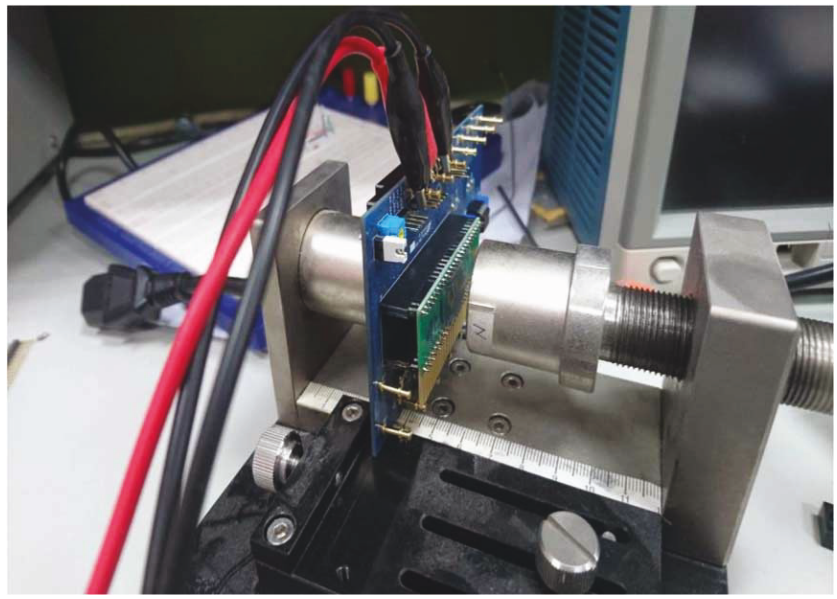

Figure 9: One-dimensional magnetic induction is generated with a magnetic induction generator.

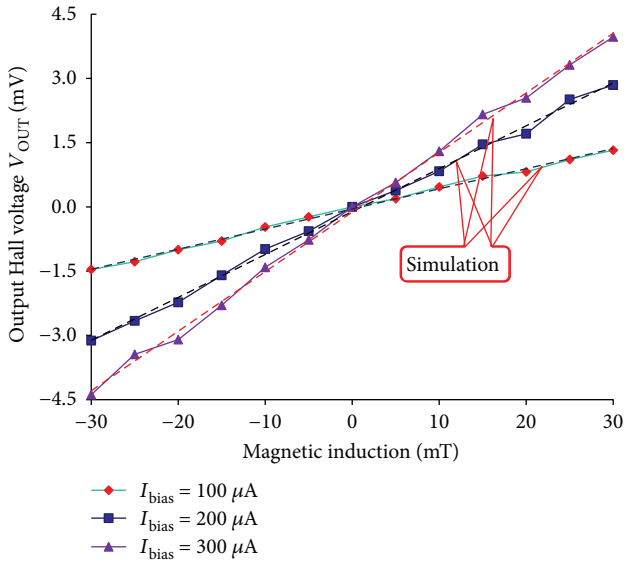

Figure 10: Simulated and measured output Hall voltages as a function of high magnetic induction for the designed 1-D magnetic chip.

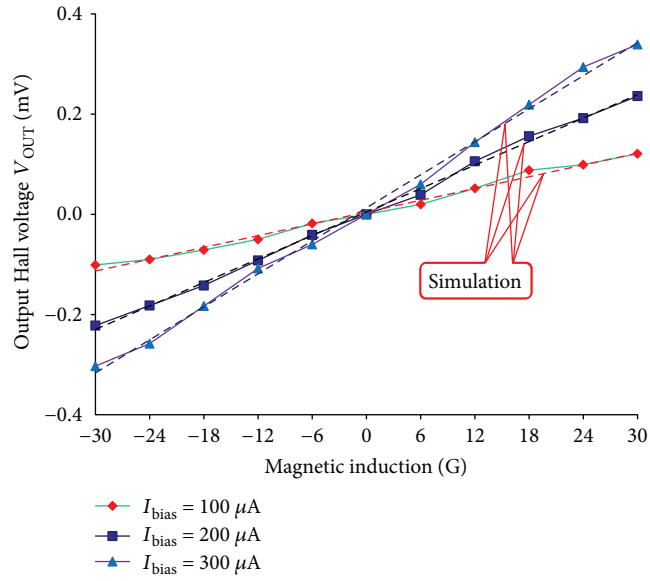

Figure 11: Simulated and measured output Hall voltages as a function of low magnetic induction for the designed magnetic chip.

of 6 G, where 1 T is equal to 10^4 G. The bias currents were selected as 100 μA, 200 μA, and 300 μA. The nonlinearity between the output Hall voltage and applied magnetic induction is poor when the bias current is low, especially for I_{bias} = 100 μA. Comparing Figure 12 with Figure 13, we find that the NLE of Figure 13 is larger than that of Figure 12. That is, the variation of NLE is large when the magnetic chip operates at low magnetic induction and low bias current.

Table 3 summarizes all the measured results of the proposed magnetic chip including the readout circuit. The NLE is inversely proportional to the bias current I_{bias}, but the measured Hall voltage V_H is proportional to the bias current. The maximum magnetosensitivity of 520.5 V/A·T or 40.04 V/V·T is obtained at the output Hall voltage of 3.123 mV, the bias current of 200 μA, and the applied magnetic induction of 30 mT. The averaged NLE is small at high magnetic induction of ±30 mT, whereas it is large at low magnetic induction of ±30 G (±3 mT). The measured results show that the proposed 1-D magnetic chip performs with good magnetosensitivity, but it exhibits poor linearity at low bias current and low magnetic induction. Table 4 summarizes all the calculated results of the proposed magnetic chip without a readout circuit. Table 5 presents a comparison between this work and the previous vertical

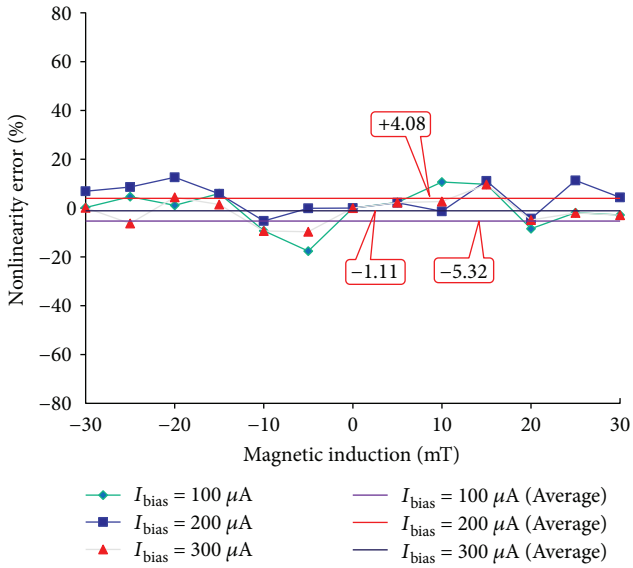

Figure 12: Simulated and measured NLEs as a function of high magnetic induction, from −30 mT to 30 mT in steps of 5 mT, and various bias currents, 100 μA, 200 μA, and 300 μA, for the designed magnetic chip.

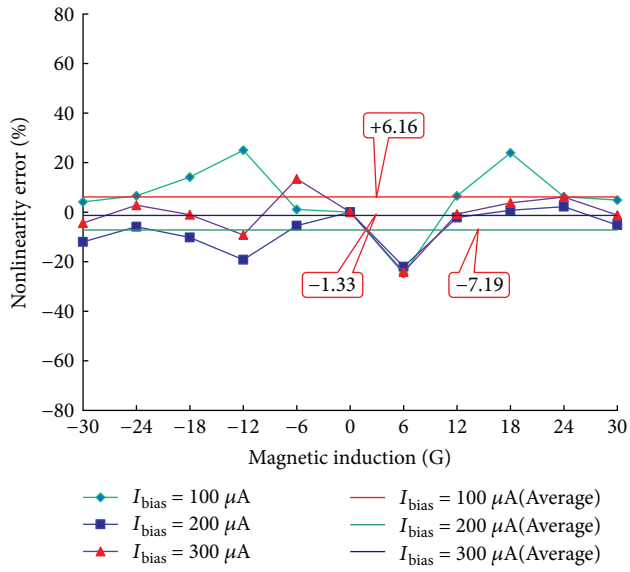

Figure 13: Simulated and measured NLEs as a function of low magnetic induction, from −30 G to 30 G in steps of 6 G, and various bias currents, 100 μA, 200 μA, and 300 μA, for the designed magnetic sensor with the readout circuit.

Hall sensors. The optimum current-related magnetosensitivity S_{RI} is 3.6855 V/A·T, which is superior to that in [29]. In addition, the optimum voltage-related magnetosensitivity S_{RV} is 0.2835 V/V·T, which is superior to that in [28, 29]. The magnetic range is large compared with that in [26, 30], and the bias current is low compared with that in [26–29]. Even though there is no measurement with respect to temperature, we predict that the temperature variation is small for MAGFET fabricated in 0.18 μm CMOS technology [31].

Table 3: Measurements of the maximum output Hall voltage V_H, optimum current-related magnetosensitivity S_{RI}, voltage-related magnetosensitivity S_{RV}, mean nonlinearity error NLE, relative bias current I_{bias}, and maximum applied magnetic induction B_Z for the proposed 1-D magnetic chip including the readout circuit.

Types	V_H (mV)	S_{RI} (V/A·T)	S_{RV} (V/V·T)	NLE (%)	I_{bias} (μA)	B_Z (mT)
1	1.462	487.3	37.49	5.32	100	30
2	3.123	520.5	40.04	4.08	200	30
3	4.381	486.7	37.44	1.11	300	30
4	0.121	403.3	31.02	6.16	100	3
5	0.236	393.3	30.25	7.19	200	3
6	0.339	376.7	28.98	1.33	300	3

Table 4: Calculations of the optimum current-related magnetosensitivity S_{RI}, voltage-related magnetosensitivity S_{RV}, relative bias current I_{bias}, and maximum applied magnetic induction B_Z for the proposed 1-D magnetic chip without a readout circuit.

Types	S_{RI} (V/A·T)	S_{RV} (V/V·T)	I_{bias} (μA)	B_Z (mT)
1	3.450	0.265	100	30
2	3.685	0.2835	200	30
3	3.446	0.2650	300	30
4	2.855	0.2196	100	3
5	2.784	0.2142	200	3
6	2.667	0.2052	300	3

5. Conclusions

A SPICE macro model is presented to facilitate comprehension of the Hall effect in the proposed 1-D hybrid magnetosensor, including a polysilicon CSHP and two identical MOSFETs, which was fabricated using standard 0.18 μm CMOS technology. The physical mechanism involves the Lorentz force pushing the positive charge right to gather it at the right side of the polysilicon CSHP, which is connected to the gate terminal of the second MOSFET. Because the equation is quadratic, the drain current I_D is amplified quadratically based on the induced Hall voltage. When the drain current signal passes through the readout circuit, the magnetosensitivity is improved effectively by amplifying the induced Hall voltage V_H in the polysilicon CSHP. By using the SPICE macro model of the proposed 1-D hybrid magnetosensor, a new Hall magnetic sensor was designed by simulating it in advance. Experimental results closely match the simulation results. The NLE is large when it operates at low magnetic induction and low bias current, even though it is a high-quality magnetic sensor. Compared with previous studies, the optimum current-related magnetosensitivity S_{RI} of 3.6855 V/A·T is superior to that in [29]. Additionally, the optimum voltage-related magnetosensitivity S_{RV} of 0.2835 V/V·T is superior to that in [28, 29]. The measured results illustrate that the proposed 1-D magnetic chip performs with good magnetosensitivity, even though it exhibits

Table 5: Performance comparison of vertical Hall magnetic sensors.

References	Technology (μm)	Mode	S_{RI} (V/A·T)	S_{RV} (V/V·T)	Magnetic range (mT)	I_{bias} (mA)	Area (μm × μm)
[26]	3.00	Voltage	31.25	—	±500	2	60 × 60
[27]	0.35	Voltage	22.85	—	±6	1.12	21 × 3
[28]	0.45	Voltage	60.50	0.025	±1.25	±50	20 × 65
[29]	0.45	Voltage	1.10	0.0056	0~3.7	115	30 × 6
[30]	0.18	Current	50.00	16	0~500	0.1	10 × 20
This work	0.18	Voltage	3.6855	0.2835	±30	0.1~0.3	120 × 180

poor linearity at low bias current and low magnetic induction. Lowering the magnetic range to ±3 mT expands the practical applications for the proposed magnetic chip.

Appendix

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* ————————————————————————————1-D Hybrid Magnetosensor————————————————————————————

* ————————————————————————————————————SPICE Model————————————————————————————————

.subckt ONE_poly Vo1 Vo2 VSource IIN IOUT mag_in sensitive='1e − 3'

MM1 Vo1 G1 VSource VSource nch W = 60uL = 60u M = 1

MM2 Vo2 G2 VSource VSource nch W = 60uL = 60u M = 1

Rin1 VIN G1 '8 + V(mag_in) ∗ sensitive'

Rin2 VIN G2 '8 − V(mag_in) ∗ sensitive'

Rout1 VOUT G1 '8 − V(mag_in) ∗ sensitive'

Rout2 VOUT G2 '8 + V(mag_in) ∗ sensitive'

RD1 VDD Vo1 50

RD2 VDD Vo2 50

VVSource VSource 0 0

.ends
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Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

The authors would like to thank the Ministry of Science and Technology, R.O.C., for financially supporting this research under Contract MOST 103-2622-E-027-014-CC3. They are grateful to the Chip Implementation Center (CIC), Taiwan, for fabricating the test chip. Samuel Johns is appreciated for his editorial assistance.

References

[1] A. D. Henriksen, B. T. Dalslet, D. H. Skieller, K. H. Lee, F. Okkels, and M. F. Hansen, "Planar Hall effect bridge magnetic field sensors," *Applied Physics Letters*, vol. 97, no. 1, article 013507, 2010.

[2] H. Heidari, U. Gatti, E. Bonizzoni, and F. Maloberti, "Low-noise low-offset current-mode Hall sensors," in *Proceedings of the 2013 9th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 325–328, Denver Colorado, USA, November 2013.

[3] A. Nathan, I. A. Mckay, I. M. Filanovsky, and H. P. Baltes, "Design of CMOS oscillator with magnetic-field frequency modulation," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 2, pp. 230–232, 1987.

[4] H. Heidari, E. Bonizzoni, U. Gatti, and F. Maloberti, "A 0.18-μm CMOS current-mode Hall magnetic sensor with very low bias current and high sensitive front-end," in *SENSORS, 2014 IEEE*, pp. 1467–1470, Valencia, Spain, November 2014.

[5] A. Ajbl, M. Pastre, and M. Kayal, "A fully integrated Hall sensor microsystem for contactless current measurement," *IEEE Sensors Journal*, vol. 13, no. 6, pp. 2271–2278, 2013.

[6] M. Pastre, M. Kayal, and H. Blanchardl, "A Hall sensor analog front end for current measurement with continuous gain calibration," *IEEE Sensors Journal*, vol. 7, no. 5, pp. 860–867, 2007.

[7] Y. J. Min, C. K. Kwon, H. K. Kim, C. Kim, and S. W. Kim, "A CMOS magnetic Hall sensor using a switched biasing amplifier," *IEEE Sensors Journal*, vol. 12, no. 5, pp. 1195-1196, 2012.

[8] L. Osberger, J. B. Schell, and V. Frick, "On optimal operation of the CHOPFET magnetic field transducer," in *2017 15th IEEE International New Circuits and Systems Conference (NEWCAS)*, pp. 137–140, Strasbourg, France, June 2017.

[9] S. I. Liu, J. F. Wei, and G. M. Sung, "SPICE macro model for MAGFET and its applications," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 4, pp. 370–375, 1999.

[10] N. Rezaei, R. Dehghani, A. Jalili, and A. Mosahebfard, "CMOS magnetic sensor with MAGFET," in *2013 21st Iranian Conference on Electrical Engineering (ICEE)*, pp. 1–5, Mashhad, Iran, May 2013.

[11] R. R. Torres, E. A. G. Dominguez, R. Klima, and S. Selberherr, "Analysis of split-drain MAGFETs," *IEEE Transactions on Electron Devices*, vol. 51, no. 12, pp. 2237–2245, 2004.

[12] Y. Yunruo, Z. Dazhong, and G. Qing, "Sector split-drain magnetic field effect transistor based on standard CMOS technology," *Sensors and Actuators A:Physical*, vol. 121, no. 2, pp. 347–351, 2005.

[13] F. C. Castaldo, V. R. Mognon, and C. A. Dos Reis Filho, "Magnetically coupled current sensors using CMOS split-drain

transistors," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1733–1736, 2009.

[14] G. M. Sung, W. S. Lin, and H. K. Wang, "A distance detector with a strip magnetic MOSFET and readout circuit," *Sensors*, vol. 17, no. 1, p. 126, 2017.

[15] E. A. G. Dominguez, M. J. Deen, and C. L. Claeys, *Low Temperature Electronics: Physics, Devices, Circuits and Applications*, Academic, New York, 2001.

[16] G. M. Sung, W. Y. Wang, and C. P. Yu, "Analysis and modeling of one-dimensional folded vertical Hall sensor with readout circuit," *IEEE Sensors Journal*, vol. 17, no. 21, pp. 6880–6887, 2017.

[17] M. Skalsky, S. Banas, and V. Panko, "A resistance model of integrated octagonal-shaped Hall sensor using JFET compact model," in *2017 IEEE International Conference on IC Design and Technology (ICICDT)*, pp. 1–4, Austin, Texas, USA, May 2017.

[18] C. H. S. Roumenin, "Bipolar magnetotransistor sensors. An invited review," *Sensors and Actuators A:Physical*, vol. 24, pp. 83–105, 1990.

[19] B. Razavi, *Design of Analog CMOS Integrated Circuits, International Edition*, McGRAW-HILL, New York, NY, USA, 2001.

[20] R. S. Popovic, "Hall-effect devices," *Sensors and Actuators*, vol. 17, no. 1-2, pp. 39–53, 1989.

[21] Y. M. Hsiao, M. S. Shiau, and K. H. Li, "Design a bioamplifier with high CMRR," *VLSI Design*, vol. 2013, Article ID 210265, 5 pages, 2013.

[22] A. Goel, "Novel high gain low noise CMOS instrumentation amplifier for biomedical applications," in *2013 International Conference on Machine Intelligence and Research Advancement*, pp. 392–396, Katra, India, December 2013.

[23] M. Goswami and S. Khanna, "DC suppressed high gain active CMOS instrumentation amplifier for biomedical application," in *2011 International Conference on Emerging Trends in Electrical and Computer Technology*, pp. 747–751, Nagercoil, India, March 2011.

[24] H. Heidari, E. Bonizzoni, U. Gatti, and F. Maloberti, "Analysis and modeling of four-folded vertical Hall devices in current domain," in *2014 10th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 1–4, Grenoble, France, 2014.

[25] G. M. Sung, "Interaction between magnetoresistor and magnetotransistor in the longitudinal and folded vertical Hall devices," *IEEE Sensors Journal*, vol. 4, no. 6, pp. 749–758, 2004.

[26] M. Paranjape, L. Landsberger, and M. Kahrizi, "A 2-D vertical Hall magnetic field sensor using active carrier confinement and micromachining techniques," in *Solid-State Sensors and Actuators, 1995 and Eurosensors IX.. Transducers '95. The 8th International Conference on*, pp. 253–256, Stockholm, Sweden, June 1995.

[27] J. Pascal, L. Hebrard, J. B. Kammerer, V. Frick, and J. P. Blonde, "A vertical Hall device in standard submicron CMOS technology," in *SENSORS, 2007 IEEE*, pp. 1480–1483, Atlanta, GA, USA, October 2007.

[28] C. Sander, R. Raz, P. Ruther et al., "Fully symmetric vertical hall devices in CMOS technology," in *SENSORS, 2013 IEEE*, pp. 1–4, Baltimore, MD, USA, November 2013.

[29] C. Sander, C. Leube, and O. Paul, "Novel compact two-dimensional CMOS vertical Hall sensor," in *2015 Transducers - 2015 18th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, pp. 1164–1167, Anchorage, Alaska, USA, June 2015.

[30] H. Heidari, U. Gatti, and F. Maloberti, "Sensitivity characteristics of horizontal and vertical Hall sensors in the voltage- and current-mode," in *2015 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp. 330–333, Glasgow, Scotland, July 2015.

[31] Y. J. Min and S. W. Kim, "A CMOS TDC-based digital magnetic Hall sensor using the self temperature compensation," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 329–332, San Jose, CA, USA, September 2008.