

Research Article

14-Bit Fully Differential SAR ADC with PGA Used in Readout Circuit of CMOS Image Sensor

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This paper proposes a 14-bit fully differential Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) with a programmable gain amplifier (PGA) used in the readout circuit of CMOS image sensor (CIS). SAR ADC adopts two-step scaled-reference voltages to realize 14-bit conversion, aimed at reducing the scale of capacitor array and avoiding using calibration to mitigate the impact of offset and mismatch. However, the reference voltage self-calibration algorithm is applied on the design to guarantee the precision of reference voltages, which affects the results of conversion. The three-way PGA provides three types of gains: 3x, 4x, and 6x, and samples at the same time to get three columns of pixel signal and increase the system speed. The pixel array of the mentioned CIS is 1026×1024 , and the pixel pitch is $12.5 \mu\text{m} \times 12.5 \mu\text{m}$. The prototype chip is fabricated in the 180 nm CMOS process, and both digital and analog voltages are 3.3 V. The total area of the chip is $6.25 \times 18.38 \text{ mm}^2$. At 150 kS/s sampling rate, the SNR of SAR ADC is 71.72 dB and the SFDR is 82.91 dB. What is more, the single SAR ADC consumes 477.2 uW with the 4.8 V_{pp} differential input signal and the total power consumption of the CIS is about 613 mW.

1. Introduction

An image sensor is a device that converts light signals into electrical signals. In recent years, the demand for an image sensor is continuously increasing, which is widely used in mobile phones, SLR digital cameras, automotive electronics, and security industry fields [1]. Mainstream image sensor technologies are roughly divided into two types: CCD image sensor and CMOS image sensor (CIS). With the advantages of high resolution and low noise, CIS gradually becomes the first choice of sophisticated and important fields. Readout circuit is the core part of CIS, whose continuous speed is normally between 50 fps and 10 Mfps while ADC is the important module in readout circuit [2, 3]. Based on the number of ADCs used in a circuit, column ADC may be the most suitable ADC applied in the large pixel array, keeping a good balance between area, power, and speed while the other types are chip ADC and pixel ADC. With the size of pixel array increasing, the mutual interference between signals will increase the complexity of the system when the pixel array studied in most researches is less than $1000 \text{ H} \times 1000 \text{ V}$ [4–

6]. Combined with the above situation, SAR ADC is employed widely when the scale of pixel array increases. Compared with other types of ADC, the balance between power consumption and speed is always the advantage of SAR ADC. In order to maximize the dynamic range of SAR ADC, a programmable gain amplifier (PGA) is the necessary part used in weak-light conditions, though it usually consumes a substantial amount of power. The performance of SAR ADC and PGA directly affects the quality of the images captured by the image sensor while the bits of SAR ADC decide the resolution and the PGA determines the dynamic range.

The pixel array of CIS presented in this paper is 1026×1024 , and the pixel size is $12.5 \mu\text{m} \times 12.5 \mu\text{m}$, which is larger than normal CIS. In order to read signal as fast as possible, column readout circuit is adopted. The resolution of SAR ADC is 14 bits, which is relatively high. Usually, a calibration algorithm is adopted in this situation while the SAR ADC used in this paper do not follow the mainstream practice, considering the power, area, and complexity. However, a reference voltage precision optimization algorithm is used to

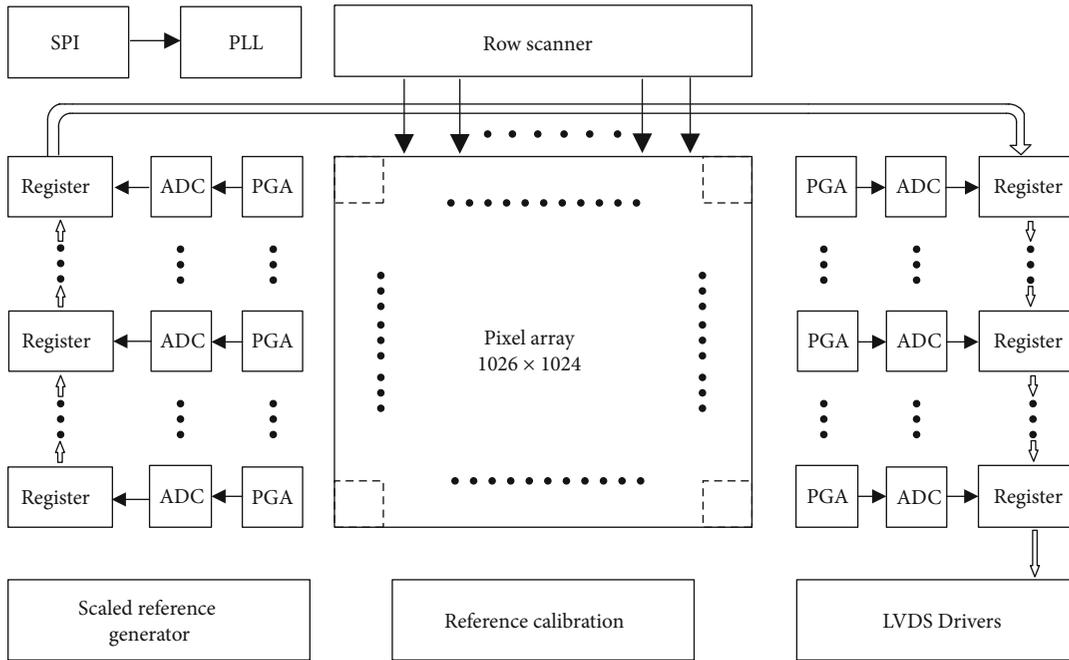


FIGURE 1: System architecture of the proposed CIS.

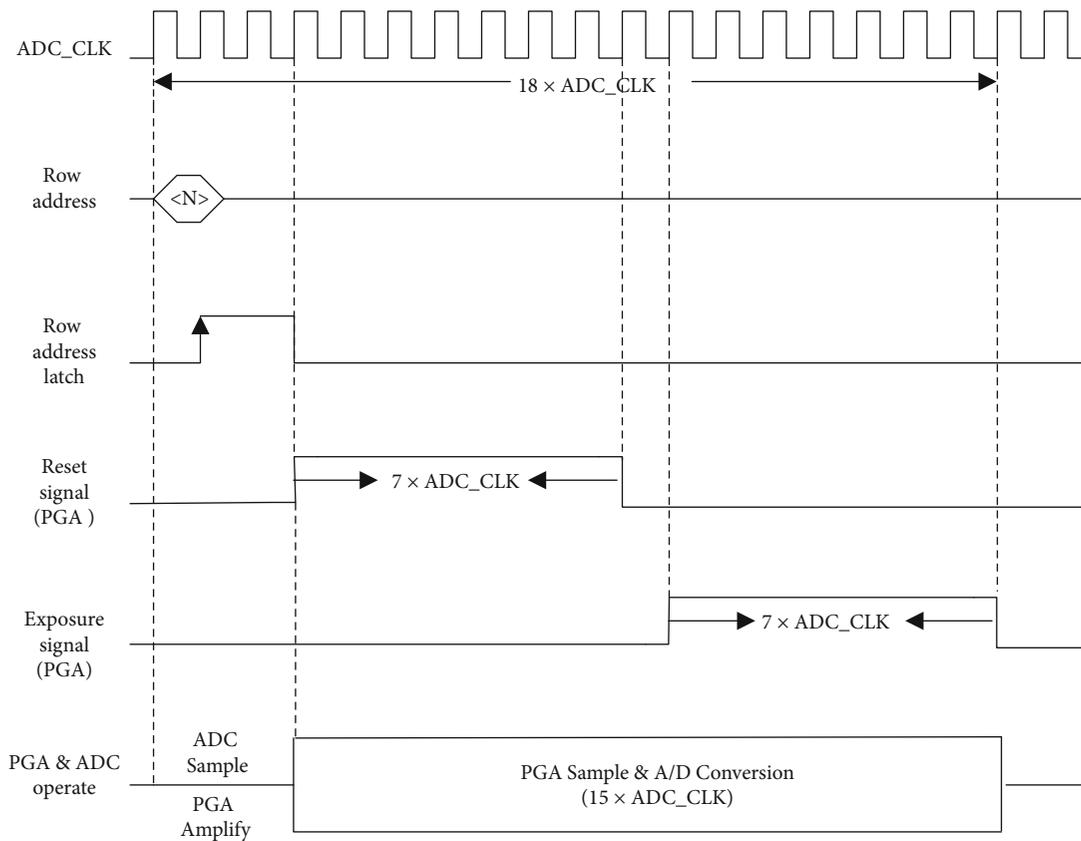


FIGURE 2: System timing of the proposed CIS.

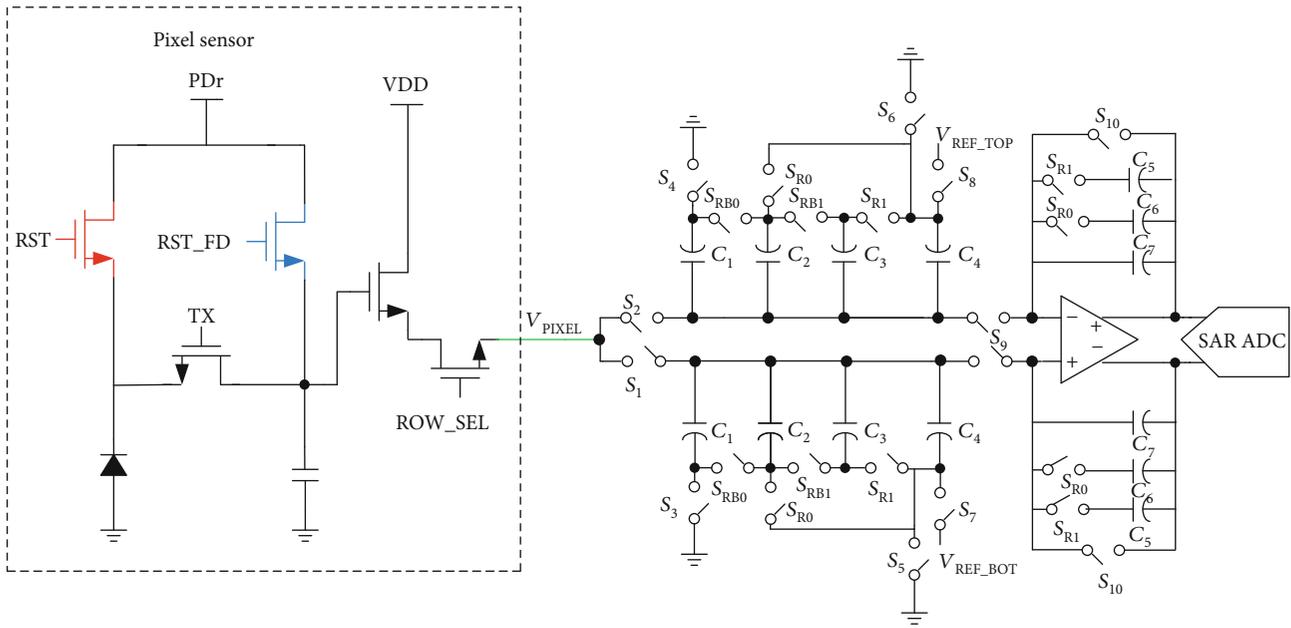


FIGURE 3: The proposed architecture of PGA samples the signal from the 5-T pixel sensor.

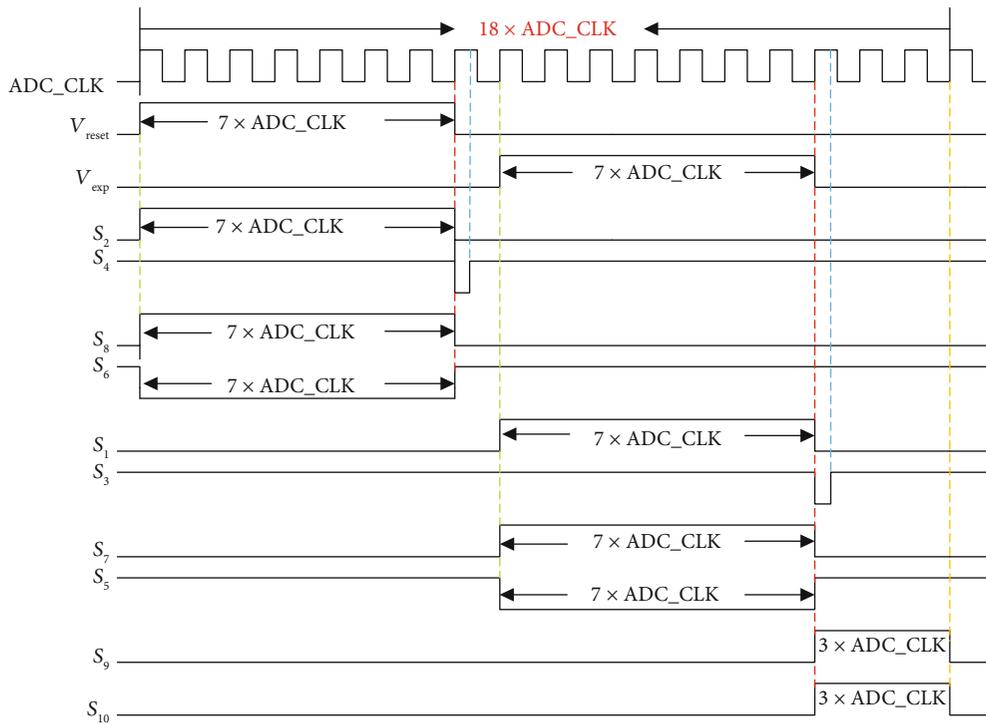


FIGURE 4: Timing diagram for the PGA.

improve the performance of SAR ADC. What is more, PGA provides the gain of 3x, 4x, and 6x, based on the input signal.

The initial shorter conference paper introduces the working principle and results of the CIS chip briefly [7]. Based on the initial paper, this paper is organized as follows, which shows more details of the CIS chip. Section 2 describes the architecture of the system. The operation principle of different modules is discussed in Section 3, including implementa-

tion details of ADC and PGA. The simulated and experimental results of the prototype are illustrated in Section 4. Section 5 concludes this paper.

2. System Architecture

Figure 1 shows the architecture of the proposed CIS, which includes pixel array, PGA, ADC, register, row scanner,

reference generator, reference calibration, Low-Voltage Differential Signaling (LVDS) drivers, and auxiliary circuits. Considering more than one million pixels and the frame rate (50 fps), a column readout circuit is used when a row scanner is applied on selecting a specific row. When the row is determined by a row scanner, a column readout circuit begins to work. The small signal is amplified by PGA and then converted into a digital signal by ADC, which is shifted into register. Finally, the LVDS driver takes on the role of output signal. The proposed CIS works at the speed of 150 KS/s, and the reference clock signal is 2.7 MHz.

During the whole process, the function of PGA is to sample exposure signal, reset signal, and provide three gains: 3x, 4x, and 6x. Owing to exposure signal lower than reset signal, which means that the calculated signal for the difference between exposure signal and reset signal is single-ended, the fixed deviation is added to the system for converting a single-ended signal into differential forms, which is consistent with SAR ADC input. What is more, in order to speed the upsampling process, three-way PGA corresponding to three columns of pixel array is adopted instead of sampling signal one by one. The gain of PGA is decided by the size of signal, which should be distinguished before transferred into SAR ADC.

14-bit fully differential SAR ADC is necessary for the proposed CIS, which directly affects the image. The high-precision reference voltage is the guarantee of SAR ADC. As a result, a scaled reference generator is used with a reference calibration module.

The system timing of the proposed CIS is shown in Figure 2. The working cycle of the chip is 18 ADC_CLKs (reference clock signal). During the first 3 ADC_CLKs, a specific row is chosen when SAR ADC samples the signal amplified by PGA. The remained 15 ADC_CLKs mainly include the following work: the conversion of SAR ADC, the signal sampling of PGA, and the data reading. During the sampling process of PGA, the reset signal is sampled first and the exposure signal follows.

3. Operation Principle and Circuit Implementation

In this section, the operation principle and circuit implementation of CIS are introduced, which consist of PGA, SAR ADC, and reference voltage self-correction algorithm. Referring to SAR ADC, principle and timing are described. What is more, the core parts of SAR ADC are presented in detail, including comparator and DAC.

3.1. PGA. In the CMOS image sensor system, a pixel sensor which demonstrates the brightness of the outside light depends on the difference between reset signal and exposure signal. The form of reset and exposure signal is voltage, which needed to be sampled and amplified into a suitable size. In order to increase the speed of the readout circuit, reset and exposure signals are sampled by different capacitors and amplified by a differential amplifier.

Based on the principle of pixel array, the reset signal is always higher than the exposure signal, which results in the

TABLE 1: The value of capacitors from C_1 to C_7 .

C_1	C_2	C_3	C_4	C_5	C_6	C_7
$33C_u$	$4C_u$	$4C_u$	$7C_u$	$4C_u$	$4C_u$	$8C_u$

unipolar difference all the time. The proposed architecture of PGA shown in Figure 3 aims at solving the problem by introducing a fixed deviation. V_{PIXEL} represents the reset and exposure signals, which is the output signal of the 5-T pixel sensor. With the help of a combination of capacitors C_1 , C_2 , C_3 , and C_4 , the unipolar difference between them is converted into bipolar form and averaged over the positive and negative half axes. The single-ended signal is transferred to a differential signal, which is more convenient for SAR ADC. The control action of switches S_{RB} and S_{R} is the opposite, which decides the gain of PGA. The switching of S_{R1} and S_{R0} changes the magnitude of the gain from 3x to 4x or 6x. What is more, $V_{\text{REF_TOP}}$ and $V_{\text{REF_BOT}}$ are the reference voltage of SAR ADC, which is applied on PGA as well. The purpose of adopting different reference voltages is to generate the needed deviation.

The working cycle of PGA is 18 ADC_CLKs, which is the same as the system and ADC working cycle. The following analysis of operation principle of PGA is based on the charge. The change on charge represents the switch of working status.

As shown in Figure 4, reset signal which is called V_{reset} is got by PGA. During the first 7 ADCs, switches S_2 , S_4 , and S_8 are on while S_6 is off on the upper capacitor array part. What is more, switches S_{RB0} and S_{R1} are on when the lower plates of capacitors C_1 and C_2 are connected to the ground and the lower plates of capacitors C_3 and C_4 are connected to the $V_{\text{REF_TOP}}$. The total charge Q_{UP} stored in capacitors C_1 , C_2 , C_3 , and C_4 on the upper part is calculated as follows:

$$Q_{\text{UP}} = (C_1 + C_2) \cdot (V_{\text{reset}} - V_{\text{GND}}) + (C_3 + C_4) \cdot (V_{\text{reset}} - V_{\text{REF_TOP}}). \quad (1)$$

At the 8th ADC_CLK, all switches on the upper part begin to change. The switches S_2 and S_8 turn off while the switch S_6 turns on. What is more, S_4 turns off first and turns on again in the half of ADC_CLK. The lower plates of C_3 and C_4 are connected from $V_{\text{REF_TOP}}$ to the ground. However, the capacitors are not connected to new power and the total charge keeps on. Considering the switch S_2 is open, the upper plate voltages of capacitors are not regular. Based on the charge conservation and the ignorance of offset, the voltage of the upper plate can be achieved by

$$Q_{\text{UP}} = (C_1 + C_2 + C_3 + C_4)(V_{\text{UP}} - V_{\text{GND}}), \quad (2)$$

$$V_{\text{UP}} = V_{\text{reset}} - \frac{C_3 + C_4}{C_1 + C_2 + C_3 + C_4} (V_{\text{REF_TOP}} - V_{\text{GND}}). \quad (3)$$

The latter 7 ADC_CLKs are from 9 to 15 ADC_CLKs. In this period, the exposure signal is sampled by the lower part

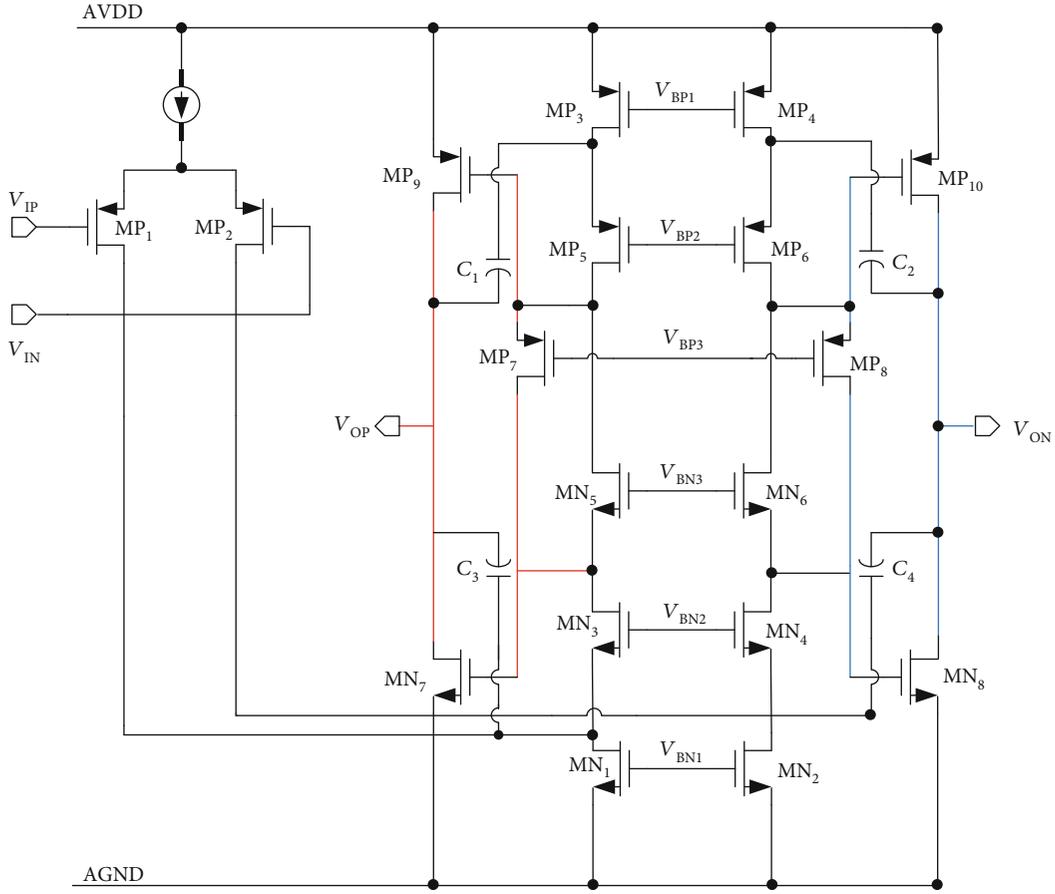


FIGURE 5: Architecture of operational amplifier.

of a circuit. The principle and process of sampling are the same as the reset signal. At the beginning, the switches S_1 , S_3 , and S_7 are closed and S_5 is open. The charge Q_{DN} sampled in this procedure is

$$Q_{DN} = (C_1 + C_2) \cdot (V_{exp} - V_{GND}) + (C_3 + C_4) \cdot (V_{exp} - V_{REF_TOP}). \quad (4)$$

And then, the switch S_5 turns on and S_1 , S_3 , and S_7 turn off. Finally, S_1 and S_7 keep off and S_3 and S_5 keep on, where the state of S_3 is from open to closed. Through this process, the following equations can be obtained:

$$Q_{DN} = (C_1 + C_2 + C_3 + C_4) (V_{DN} - V_{GND}), \quad (5)$$

$$V_{DN} = V_{reset} - \frac{C_3 + C_4}{C_1 + C_2 + C_3 + C_4} (V_{REF_BOT} - V_{GND}). \quad (6)$$

Combining equations (1)–(6), the differential signal sent into the amplifier is described by the following equations:

$$V_{IN} = V_{DN} - V_{UP}, \quad (7)$$

$$V_{IN} = (V_{exp} - V_{reset}) + \frac{C_3 + C_4}{C_1 + C_2 + C_3 + C_4} (V_{REF_TOP} - V_{GND}). \quad (8)$$

According to equation (8), apart from the difference between V_{exp} and V_{reset} , the fixed deviation is introduced as expected, which realizes the goal of making the signal spread uniformly. After sampling is finished, switches S_9 and S_{10} turn on, which lasts 3 ADC_CLK.

During the phase, the function of S_{R0} and S_{R1} is to choose different gains which is called amplify phase as well. The value of capacitors used in the PGA is shown in Table 1. The calculation formula of gain is

$$V_{IN} = \frac{C_1 + C_2 + C_3 + C_4}{C_5 + C_6 + C_7}. \quad (9)$$

If switches S_{R0} and S_{R1} both turn on, the gain of PGA is 6x. While if one of them turns off, the gain of PGA is 4x. Once both are closed, the smallest gain 3x is achieved under this situation.

As a significant part of PGA, the operational amplifier needs to be paid enough attention to. Figure 5 shows the architecture of amplifier, which needs high gain, enough bandwidth, strong driving capability, and low noise. The

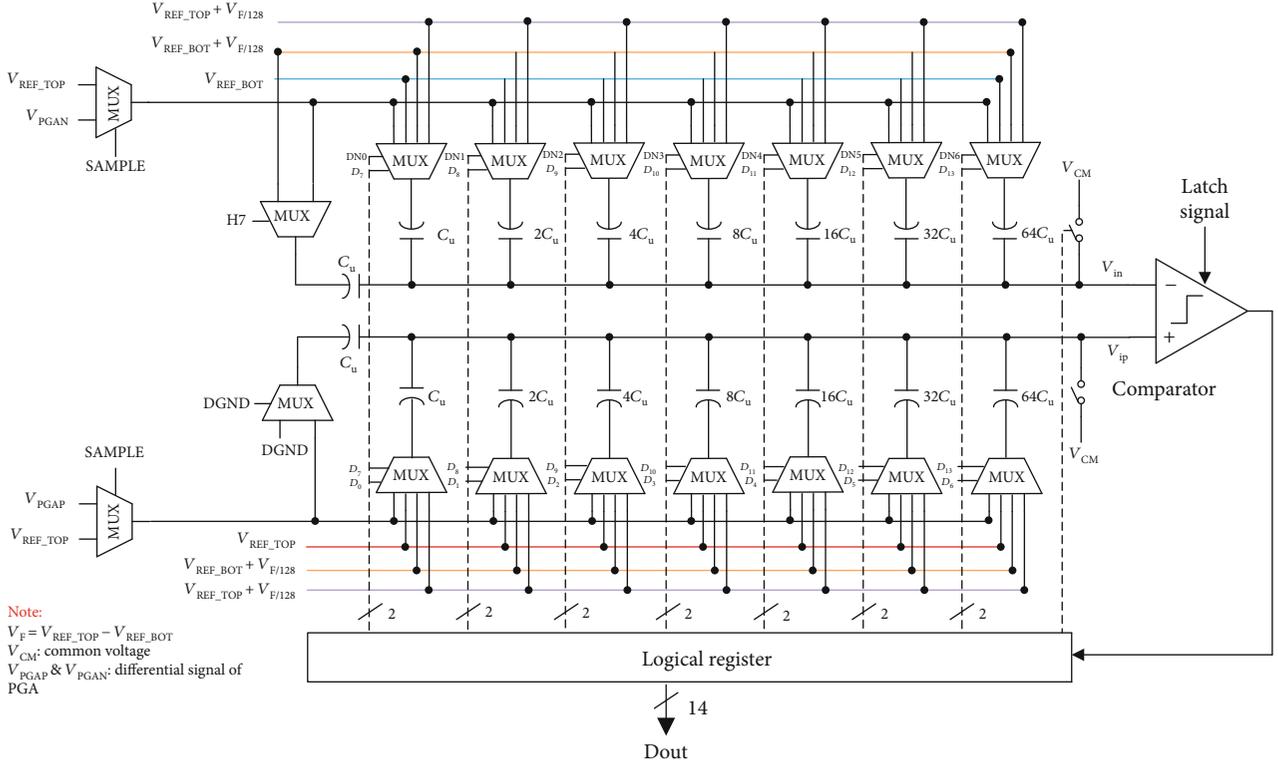


FIGURE 6: The architecture of the proposed SAR ADC.

proposed amplifier contains two stages: amplifying stage and driving stage, aimed at providing enough gain and increasing the ability of driving. Compared with other architectures of amplifier, the wider input common mode range and larger output swing are the advantages of folding cascode operational amplifier, which is applied in this situation and provides major gain. The cascode stage makes the R_{out} increase, which leads to high gain.

The driving stage is the floating-biased class AB output stage, having a strong driving ability. The size of following-up capacitor arrays used in the SAR ADC is large, which puts forward higher requirements for the driver of the input stage. Considering the high power consumption of folding cascode amplifier, the floating biased transistors MN_5 , MN_6 , MP_7 , and MP_8 are utilized to decrease and stabilize quiescent current of the output stage as analyzed in [8]. The overall gain of the two-stage amplifier is

$$A_{op} = g_{MP1} \cdot ((g_{MN3} \cdot r_{o,MN3} \cdot (r_{o,MN1} \parallel r_{o,MP1})) \parallel (g_{MP5} \cdot r_{o,MP3} \cdot r_{o,MP5})) \cdot (g_{MN7} + g_{MP9}) \cdot (r_{o,MN7} \parallel r_{o,MP9}) \quad (10)$$

When it comes to noise, the high noise is always the drawback of folding cascode amplifier, as depicted in [9]. However, the operational amplifier of this structure meets design requirements. In order to improve the performance of noise, PMOS is adopted as input, which is better than NMOS on noise. What is more, larger value of g_{MP1} and smaller value of g_{MN1} and g_{MP3} are chosen to reduce the

noise. Under the circumstance, the value of W/L needs to be weighed carefully, which is important for improving the SNR of SAR ADC.

3.2. SAR ADC. The most important module of CIS is SAR ADC, which is placed after PGA. The function of SAR ADC is to convert the analog signal amplified by PGA into the digital signal.

The sampling speed of SAR ADC required by the system is 150 KS/s, and the resolution of SAR ADC is 14 bits. Normally, the differential input method is selected to suppress the interference of common mode factors and the charge redistribution theory is applied on SAR ADC, which was first proposed by McCreary and Gray [10]. Combing the above two points, the architecture of double reference voltage SAR ADC is widely used. If the resolution of SAR ADC is beyond 10 bits, the capacitor array will be very large, taking up unexpected area in the situation. In order to avoid a huge capacitor array, the two-step scaled-reference SAR ADC is put forward, which is based on the charge redistribution theory as well. This structure was first proposed by South Korea's Shin for CMOS image sensor applications [11]. Two-step scaled reference contains four reference voltages, and the increased reference voltage is to reduce the area of the capacitor array.

3.2.1. Principle and Timing. The architecture of the proposed SAR ADC is shown in Figure 6, containing DAC, comparator, and SAR Logic. Compared with double reference voltages, two-step scaled reference keeps on the size of

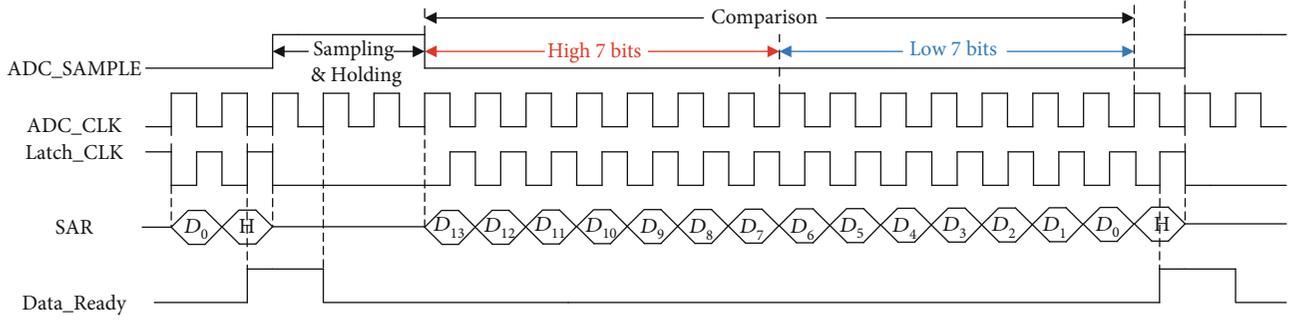


FIGURE 7: Timing diagram of SAR ADC.

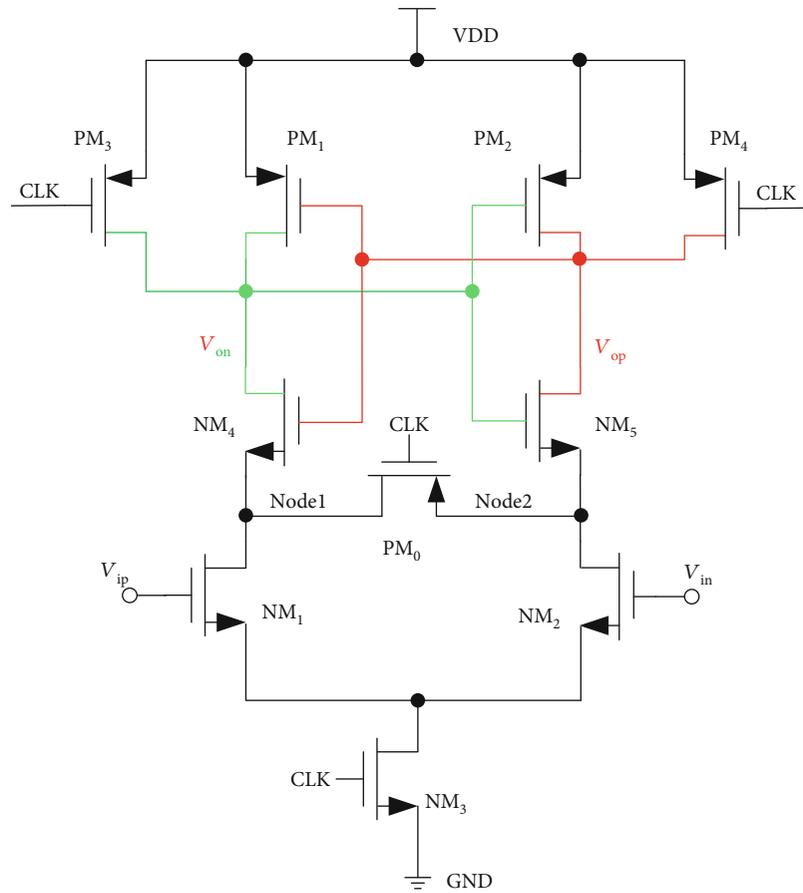


FIGURE 8: StrongARM latch topology.

capacitor array with the complex conversion process. Use the same size capacitor array, but the resolution has changed from the previous 7 bits to 14 bits, which is the core advantage of the architecture. On the other hand, the requirement of precision of reference voltage is increasing. The added reference voltages $V_{REF_TOP} + V_F/128$ and $V_{REF_BOT} + V_F/128$ need higher accuracy compared with V_{REF_TOP} and V_{REF_BOT} . V_{REF_TOP} and V_{REF_BOT} are the reference voltages used in the first stage while the $V_{REF_TOP} + V_F/128$ and $V_{REF_BOT} + V_F/128$ are applied on the second stage. The

value of V_F is

$$V_F = V_{REF_TOP} - V_{REF_BOT} \quad (11)$$

V_{PGAP} and V_{PGAN} are the output signals of PGA, which are the same as V_{OP} and V_{ON} shown in Figure 5. V_{CM} is the common voltage of the input signal of SAR ADC.

The whole process includes four parts: sampling, holding, comparison, and output. The architecture adopts lower plates of capacitors to sample. During the sampling phase,

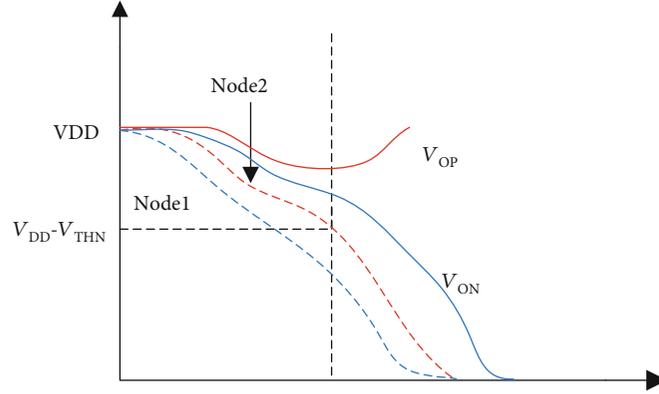


FIGURE 9: The voltage change of the whole process.

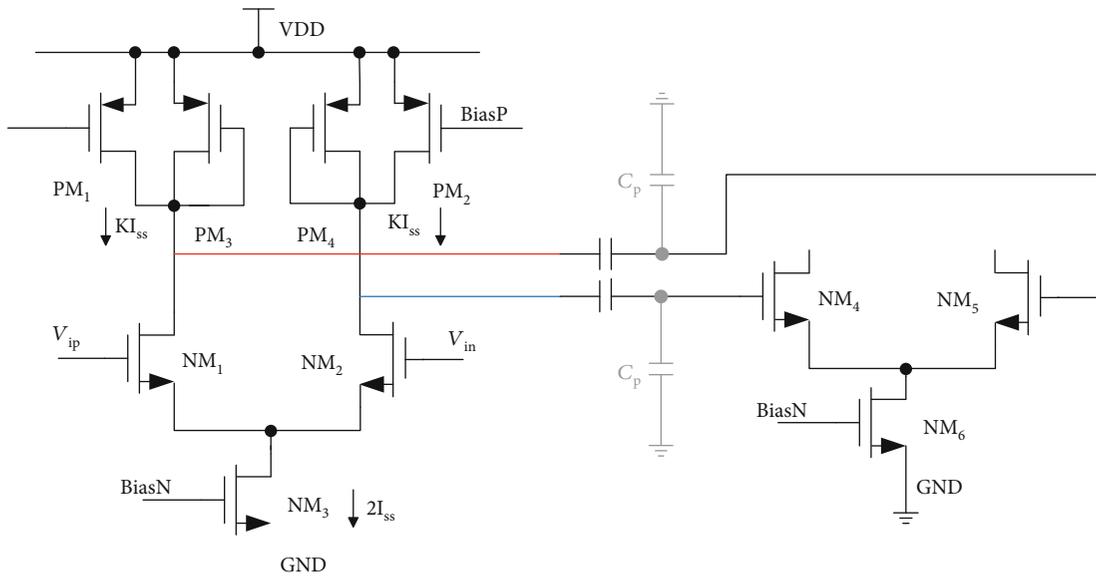


FIGURE 10: The architecture of preamplifier.

V_{PGAP} and V_{PGAN} are chosen by MUX when all upper plates of capacitors are connected to V_{CM} . The signal V_{PGAP} and V_{PGAN} are sampled by the capacitor array because all lower plates of capacitors are connected to V_{PGAP} and V_{PGAN} . The charge Q_s stored in all capacitors is calculated as

$$Q_s = -(V_{PGAP} - V_{PGAN}) * 2^7 C_u. \quad (12)$$

Converting the input voltage into the form of charge is the principle of sampling. In order to hold the sampled charge, the upper plates of capacitors do not connect to the V_{CM} . The lower plates of capacitors in the negative part are connected to the V_{REF_TOP} when the lower plates of capacitors in the positive part are connected to the V_{REF_BOT} . After finishing the procedure, according to the charge conservation theory, the following equations are obtained:

$$Q_{HP} = (V_{ip} - V_{REF_BOT}) * 2^7 C_u, \quad (13)$$

$$Q_{HN} = (V_{in} - V_{REF_TOP}) * 2^7 C_u, \quad (14)$$

$$Q_H = Q_{HP} - Q_{HN}. \quad (15)$$

Combining equations (12)–(15), the input signal of comparator is achieved:

$$V_{ip} = V_{REF_BOT} - V_{PGAP}, \quad (16)$$

$$V_{in} = V_{REF_TOP} - V_{PGAN}, \quad (17)$$

$$V_{IN} = V_{ip} - V_{in} = V_{REF_BOT} - V_{PGAP} - (V_{REF_TOP} - V_{PGAN}). \quad (18)$$

Once the holding phase is finished, SAR ADC enters the comparison phase, which contains two parts: high 7-bit conversion and low 7-bit conversion. The reference voltages of high 7-bit conversion are V_{REF_TOP} and V_{REF_BOT} while $V_{REF_TOP} + V_F/128$ and $V_{REF_BOT} + V_F/128$ are the reference voltages of low 7-bit conversion. Controlling the connection of lower plates of capacitor array to adjust the input signal of comparator and then get the corresponding code according

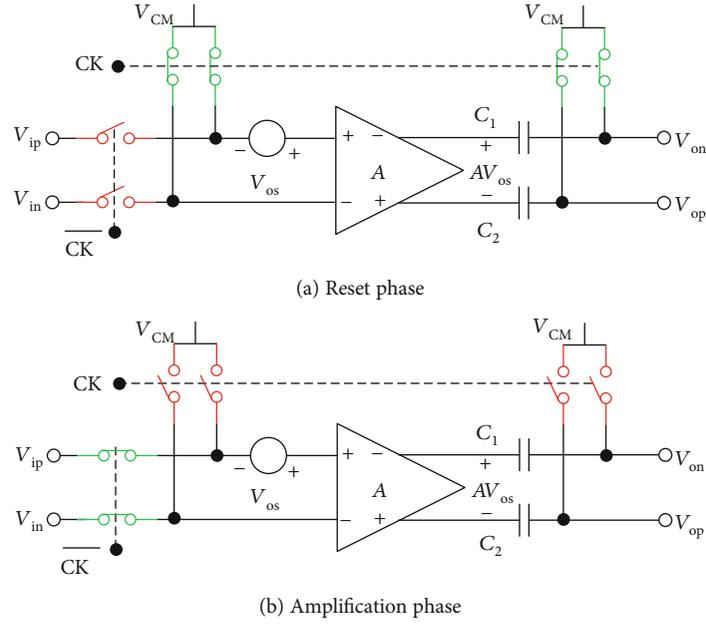


FIGURE 11: Offset cancellation circuit.

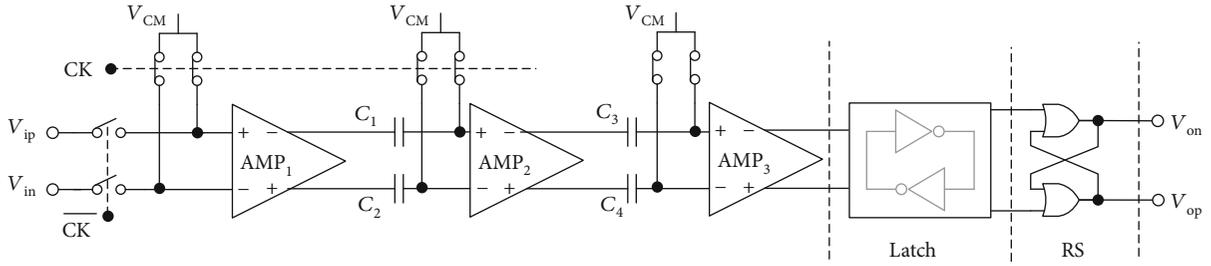


FIGURE 12: The complete structure of comparator.

to the comparison result is the core working principle of comparison.

During the high 7-bit conversion, the MSB (D_{13}) is taken for example and the others are the same working process. At the beginning, the lower plate of highest capacitance ($64C_u$) in the positive side is connected from V_{REF_BOT} to V_{REF_TOP} and the lower plate of the highest capacitor ($64C_u$) in the negative side is connected to V_{REF_BOT} . The other plates of capacitance keep on the current states. The change of charge Q_c stored in the capacitor array is calculated as follows:

$$\begin{aligned} Q_c &= (V_{REF_TOP} - V_{REF_BOT}) * 2^6 C_u - (V_{REF_BOT} - V_{REF_TOP}) \\ &\quad * 2^6 C_u = 2 * (V_{REF_TOP} - V_{REF_BOT}) * 2^6 C_u \\ &= (V_{REF_TOP} - V_{REF_BOT}) * 2^7 C_u. \end{aligned} \quad (19)$$

The input signal of comparator V_{IN} follows with Q_c :

$$V_{IN} = -(V_{PGAP} - V_{PGAN}). \quad (20)$$

If the V_{IN} is negative, the result of comparator is 0, which

means V_{PGAP} is larger than V_{PGAN} and the SAR Logic should control the switch to keep on. Otherwise, the result of comparator is 1. The lower plate of highest capacitance ($64C_u$) in the positive side is connected to V_{REF_BOT} instead of V_{REF_TOP} , and the negative side is the opposite, which also represents V_{PGAP} which is smaller than V_{PGAN} . The rest 6 bits work in the same way.

The conversion of low 7 bits is different from high 7 bits. When the conversion of the 7th bit is finished, the lower plate of dummy capacitor in the negative side is connected to $V_{REF_BOT} + V_F/128$ and the lower plates of other capacitors are connected to $V_{REF_BOT} + V_F/128$ or $V_{REF_TOP} + V_F/128$, which are determined by the original state and increases by $V_F/128$. The purpose of the switch action is to keep the value of V_{IN} on with the increasement of connected voltages of capacitors in the negative side and decrease of connected voltage of dummy capacitor. The decreased charge Q_{DEC} and Q_{INC} can be expressed as

$$Q_{DEC} = (V_{REF_TOP} - (V_{REF_BOT} - \frac{V_F}{128})) * C_u = (V_F - \frac{V_F}{128}) * C_u, \quad (21)$$

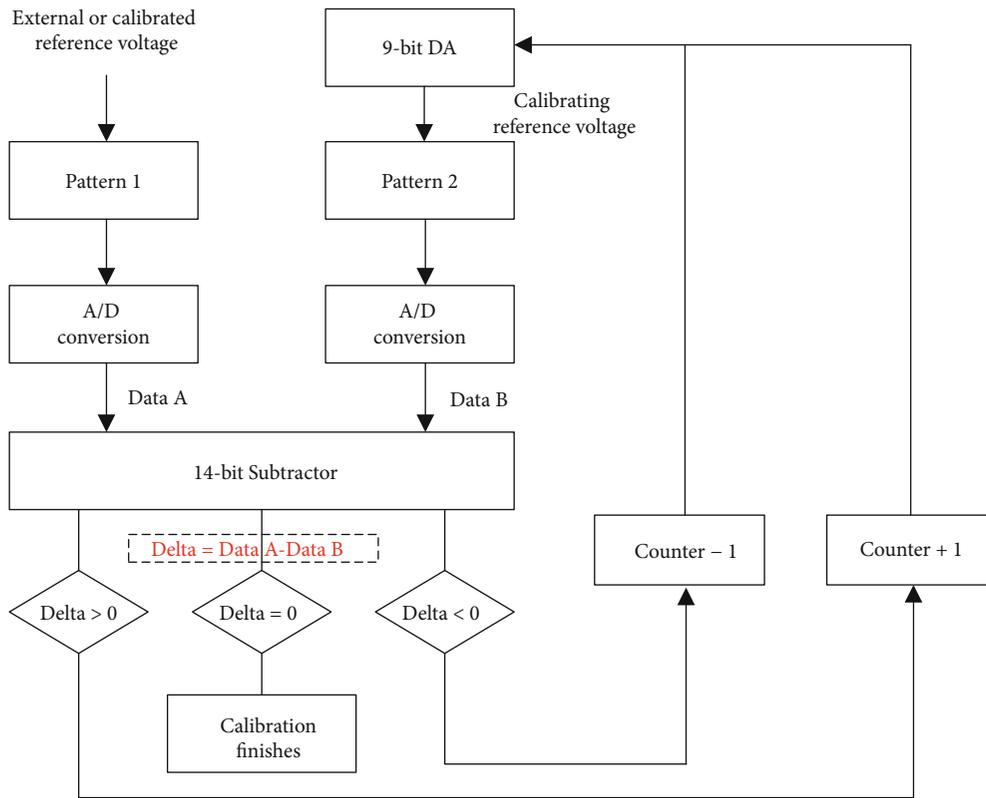


FIGURE 13: Flowchart of the self-calibration algorithm.

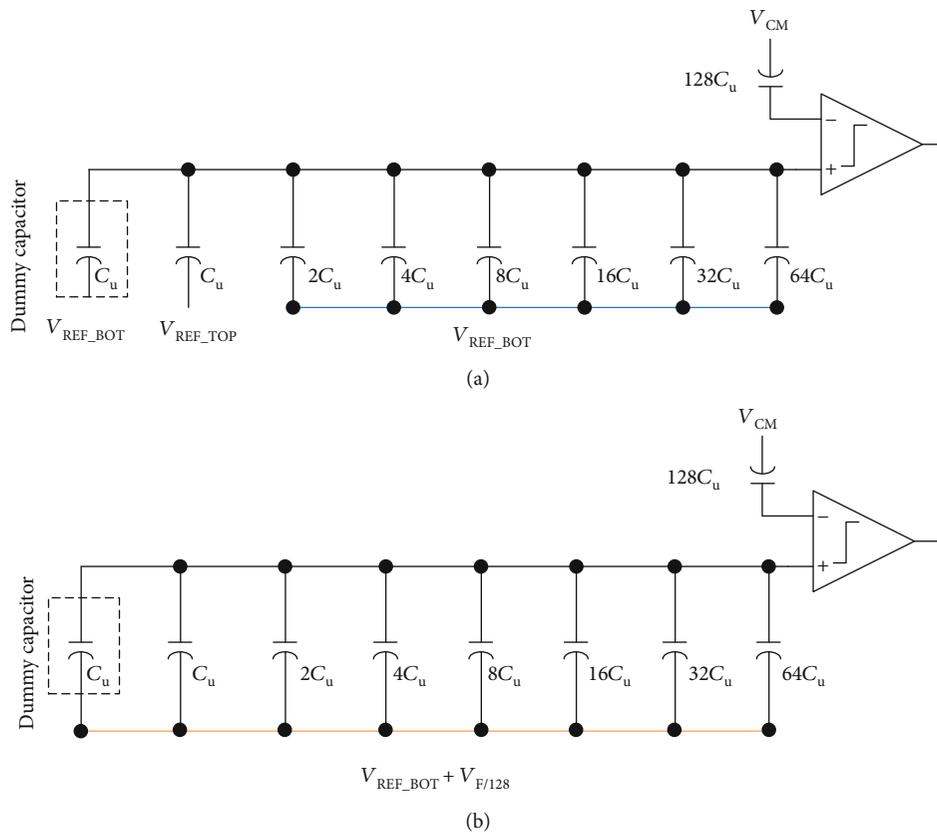


FIGURE 14: (a) $V_{REF_BOT} + V_F/128$ calibration pattern 1 and (b) $V_{REF_BOT} + V_F/128$ calibration pattern 2.

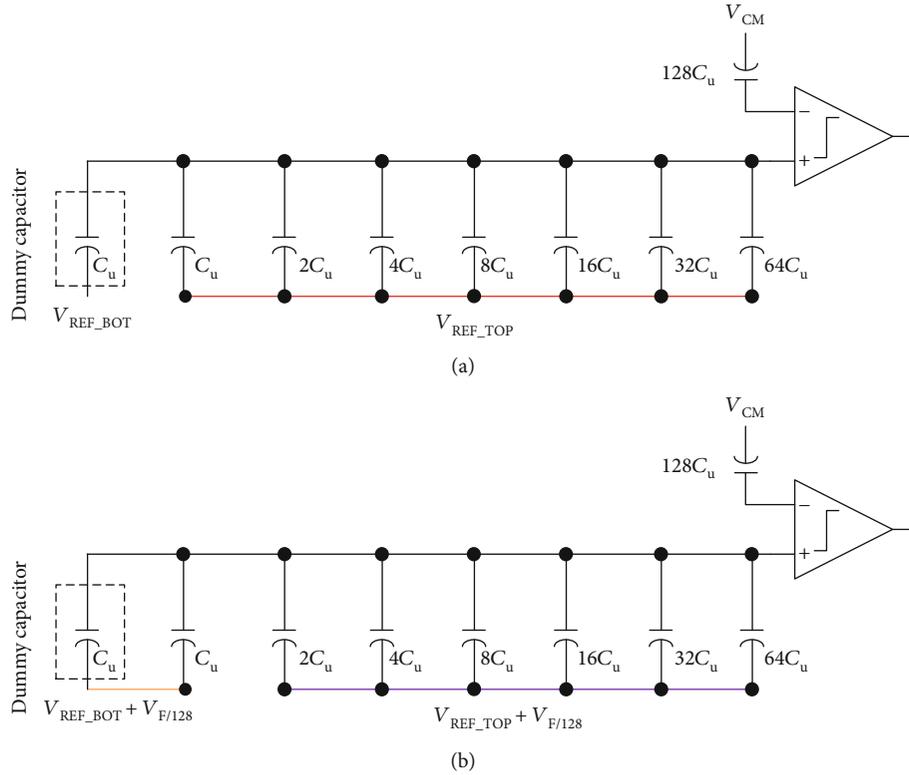


FIGURE 15: (a) $V_{REF_TOP} + V_F/128$ calibration pattern 1 and (b) $V_{REF_TOP} + V_F/128$ calibration pattern 2.

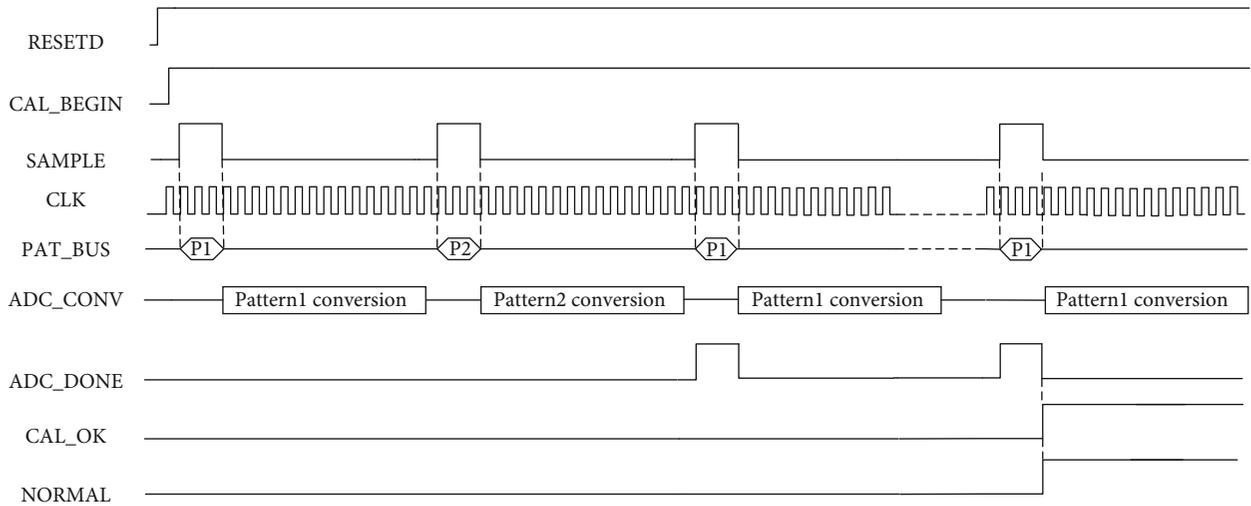


FIGURE 16: The timing block of calibration.

$$Q_{INC} = \frac{V_F}{128} \cdot \left(\sum_{n=6}^0 \frac{1}{2^n} \cdot C_u \right) = \left(V_F - \frac{V_F}{128} \right) \cdot C_u. \quad (22)$$

According to equations (21) and (22), Q_{DEC} and Q_{INC} are equal, which means the value of V_{IN} does not change. At this time, the requirements of low 7-bit conversion are met. In order to explain the process, the comparison of 6th bit is taken for example. Because the low 7-bit conversion and high 7-bit conversion use the same capacitor array, the procedure

is similar. What is more, the switch action of lower 7 bits is based on the high 7 bits. For instance, the conversion of 6th bit is related to 13th bit. If D_{13} is 0, which means the lower plate of the highest capacitance ($64C_u$) in the positive side is connected to V_{REF_BOT} and the lower plate of the highest capacitance ($64C_u$) in the negative side is connected to $V_{REF_TOP} + V_F/128$, the connection voltage of lower plate of the highest capacitance ($64C_u$) in the positive side will increase by $V_F/128$ and the connection voltage in the negative side will decrease by $V_F/128$. The increased charge

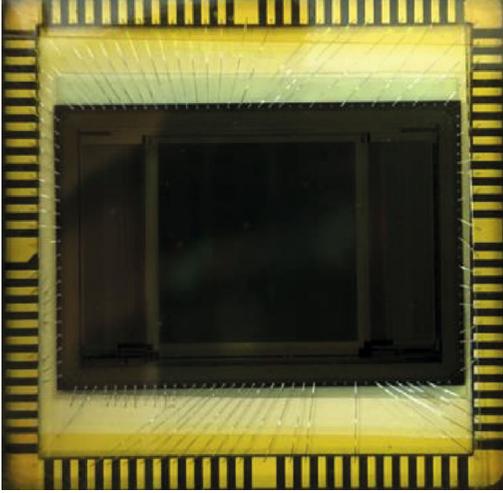


FIGURE 17: The photograph of the chip.

Q_{INC} and increased voltage of input signal ΔV are achieved:

$$Q_{\text{INC}} = \left(\frac{V_F}{128} - \left(-\frac{V_F}{128} \right) \right) \cdot 64C_u = C_u \cdot V_F, \quad (23)$$

$$\Delta V = \frac{V_F}{128}. \quad (24)$$

If D_{13} is 1, which means the lower plate of the highest capacitance ($64C_u$) in the positive side is connected to $V_{\text{REF_TOP}}$ and the lower plate of the highest capacitance ($64C_u$) in the negative side is connected to $V_{\text{REF_BOT}} + V_F/128$. The process is similar to the situation of $D_{13} = 1$. The change on charge and the input signal are the same as well. The result of comparison determines the switch actions, which has been explained above. The voltage V_{D6} represented by the capacitor array during the process is calculated:

$$V_{D6} = -V_{\text{IN}} + \left(-1 + \sum_{n=13}^6 \frac{1}{2^{D_n}} \right) \cdot (V_{\text{REF_TOP}} - V_{\text{REF_BOT}}). \quad (25)$$

The last six bits adopts the same working process. Combining the conversion of high 7 bits and low 7 bits, the analog signal sampled by PGA is converted into 14-bit digital code.

The timing diagram of SAR ADC is shown in Figure 7. The reference clock is still ADC_CLK. The whole procedure occupies 18 ADC_CLKs. The 3 ADC_CLKs are used for sampling while 14 ADC_CLKs are adopted for comparison and the function of the last ADC_CLK is to output the results. During the comparison, the comparator begins to compare at the rising edge of ADC_CLK and latch the signal at the following edge of ADC_CLK. After latching the last comparison, the signal DATA_Ready turns to a high level and keeps on before the first ADC_CLK finishes.

3.2.2. Comparator. The comparator almost decides the speed of SAR ADC. In order to speed up the comparison, the StrongARM Latch topology is used, which is explained in [12]. The

StrongARM latch topology is not only good at speed but also expert in saving power. The circuit is shown in Figure 8.

The StrongARM latch is based on positive feedback, which includes two working stages: reset phase and regeneration phase. At the beginning, the CLK is low. NM_1 and NM_2 are off while Node1 and Node2 are connected together to keep the same voltage for resetting. The output V_{op} and V_{on} are reset to the power supply voltage by PM_3 and PM_4 , respectively. What is more, PM_1 , PM_2 , NM_4 , and NM_5 are off. When in the regeneration stage, CLK is high and the current flows through NM_1 and NM_2 . Assuming that $V_{\text{ip}} > V_{\text{in}}$, the current flowing through NM_1 is larger than NM_2 , causing the voltage of Node1 to drop faster than Node2. When the voltages of Node1 and Node2 arrive at $V_{\text{DD}} - V_{\text{THN}}$, NM_4 and NM_5 turn on. Because Node1 first reaches $V_{\text{DD}} - V_{\text{THN}}$, V_{op} begins to drop, which also leads to the dropping speed of V_{op} slow down. Positive feedback is formed and V_{op} becomes V_{DD} finally. The loop gain A_p of the positive feedback loop is

$$A_p = \left(g_{\text{mn4}} + g_{\text{mp1}} \right) \cdot \left(r_{\text{on4}} \parallel r_{\text{op1}} \right) \cdot \left(g_{\text{mn5}} + g_{\text{mp2}} \right) \cdot \left(r_{\text{on5}} \parallel r_{\text{op2}} \right). \quad (26)$$

The voltage change of the whole process is shown in Figure 9.

In order to reduce the impact of input offset voltage and kickback noise, the preamplifier is adopted, the architecture of which is shown in Figure 10. The preamplifier uses Current Starving Technical [13] to increase the gain instead of using cascode structure. The small signal gain is calculated as follows:

$$A_v = \frac{g_{\text{mn2}}}{g_{\text{mp4}}} = \frac{\sqrt{2\mu_n C_{\text{ox}} (w/L)_2 I_{\text{dn2}}}}{\sqrt{2\mu_p C_{\text{ox}} (w/L)_4 I_{\text{dp4}}}} = \frac{\sqrt{\mu_n (w/L)_2}}{\sqrt{\mu_p (w/L)_4}} \cdot \frac{1}{\sqrt{1-K}}. \quad (27)$$

K represents the ratio coefficient of the current flowing through the NM_4 or NM_5 , which determines the gain of amplifier. Aimed at making the resolution of latch shown in Figure 8 reach 0.5LSB, the gain of the amplifier requires at least

$$A_v = \frac{V_{\text{OS,Latch}}}{1/2\text{LSB}}. \quad (28)$$

The gain is related to $V_{\text{OS,Latch}}$ closely. Based on the requirement of resolution and process characteristics, the three-stage operational amplifier is adopted.

The amplifier itself owns offset voltage, requiring the gain of the input stage maximized. The input offset voltage of the last two stages can be ignored when it is equivalent to the input. However, the offset voltages are still needed to be eliminated as much as possible, which is depicted in Figure 11.

The work of amplifier contains two phases: reset phase and amplification phase. In the reset phase, both input terminals are short to the common mode voltage V_{CM} through the

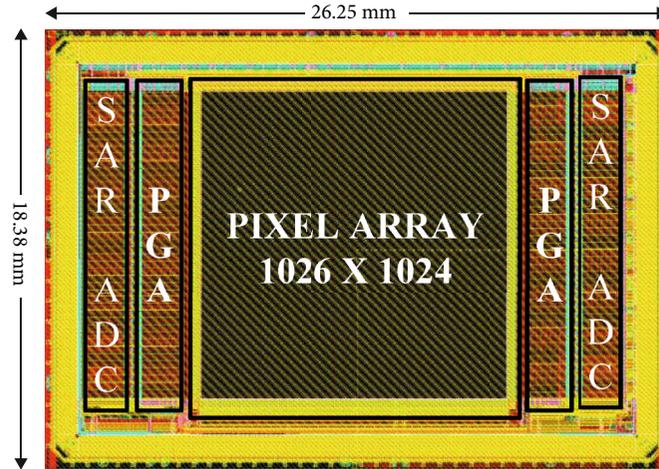


FIGURE 18: The layout of the chip.

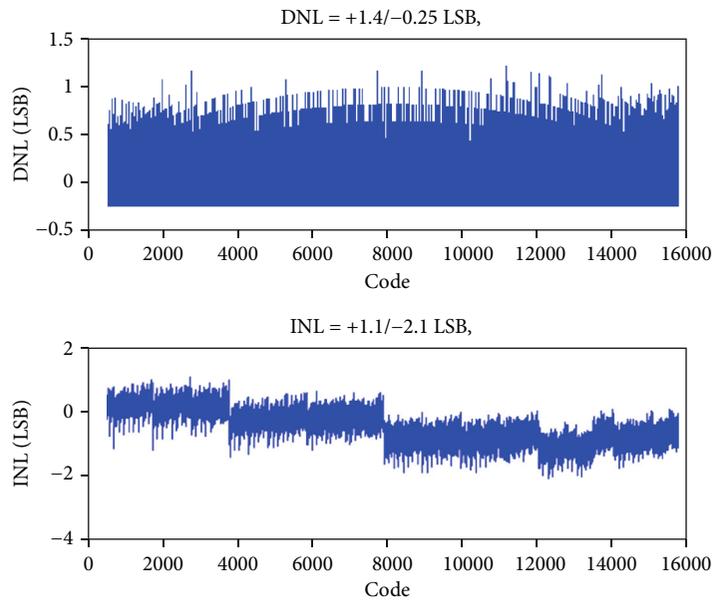


FIGURE 19: Static performance of SAR ADC.

switch when the two output terminals are also short to the V_{CM} . The output offset is stored in capacitor C_1 and C_2 , which is the opposite to the input offset:

$$V_{os,out} = -A \cdot V_{os,in}. \quad (29)$$

When the amplifier enters the amplification stage, the switches connected to V_{CM} do not keep on and input signals V_{ip} and V_{in} connect to the input of amplifier. At this time, the output signal of amplifier can be obtained:

$$V_{out} = (V_{ip} - V_{in} + V_{os,in}) \cdot A - A \cdot V_{os,in} = (V_{ip} - V_{in}) \cdot A. \quad (30)$$

According to equation (30), the output does not contain V_{os} , which means the effect of offset voltage is eliminated.

The complete comparator design is shown in Figure 12, including amplifiers, latch, and RS flip-flop. The three-stage preamplifier amplifies the input signal, and then, the amplified signal is compared by StrongARM latch quickly. The function of RS flip-flop is to output the results to the logic register.

3.3. Reference Voltage Self-Calibration Algorithm. The proposed architecture adopts a two-step scaled reference. The resolution of two reference voltages $V_{REF_TOP} + V_F/128$ and $V_{REF_BOT} + V_F/128$ is up to $V_F/128$, which is difficult for design. Once the accuracy of the reference voltage is far from the target value, the results of SAR ADC are greatly affected. The reference voltage self-calibration algorithm is applied to guarantee the required accuracy.

The proposed reference voltage self-calibration algorithm is based on the split capacitor linearity on-chip self-

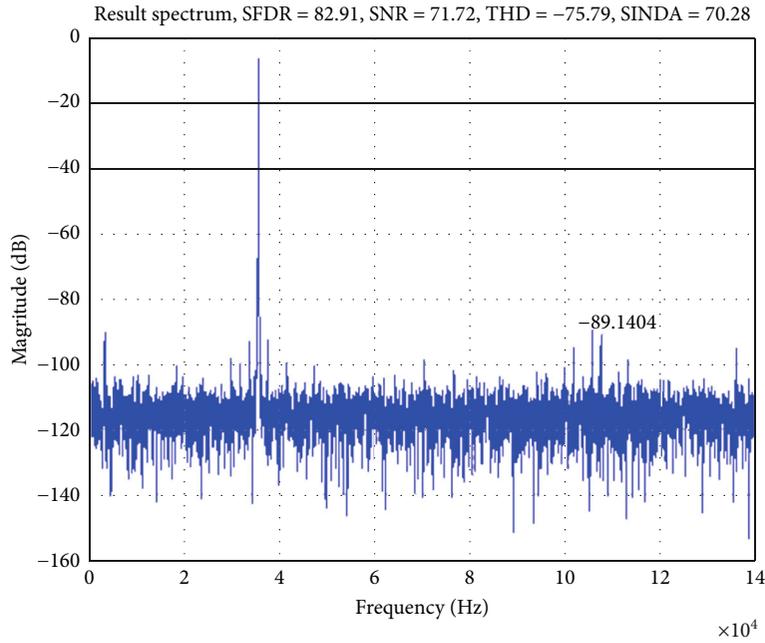


FIGURE 20: Dynamic performance of SAR ADC.

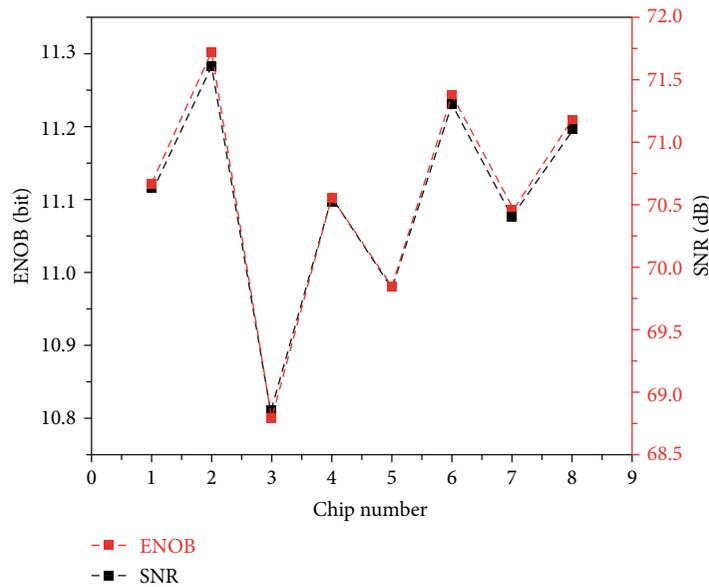


FIGURE 21: The measured SNR and ENOB of different chips.

calibration method proposed by Yoshioka et al. [14], which is to correct the output code by comparing the certain capacitors and the rest of all low capacitors. When the certain capacitance is consistent with the rest of all low capacitors, the calibration is finished.

Combining the correlated double sampling circuit technology and the above self-calibration method, the reference voltage self-calibration algorithm is proposed and the flow-chart is shown in Figure 13.

The algorithm includes two patterns. Pattern 1 provides the relatively accurate target value when pattern 2 represents

the value to be corrected. Two-step scaled reference is used in the process. The reference voltages V_{REF_TOP} and V_{REF_BOT} are the precise voltages, which generate $V_{REF_TOP} + V_F/128$ or $V_{REF_BOT} + V_F/128$ by DAC. The $V_{REF_TOP} + V_F/128$ or $V_{REF_BOT} + V_F/128$ in pattern 2 is the internally generated voltage, which is a rough value and needs to be corrected.

The precise voltages and rough voltages are converted into digital code through ADC. The difference between precise voltages and rough voltages determines the action of counter. Once the difference is equal to zero, the calibration is finished. If the difference is not equal to zero, the counter

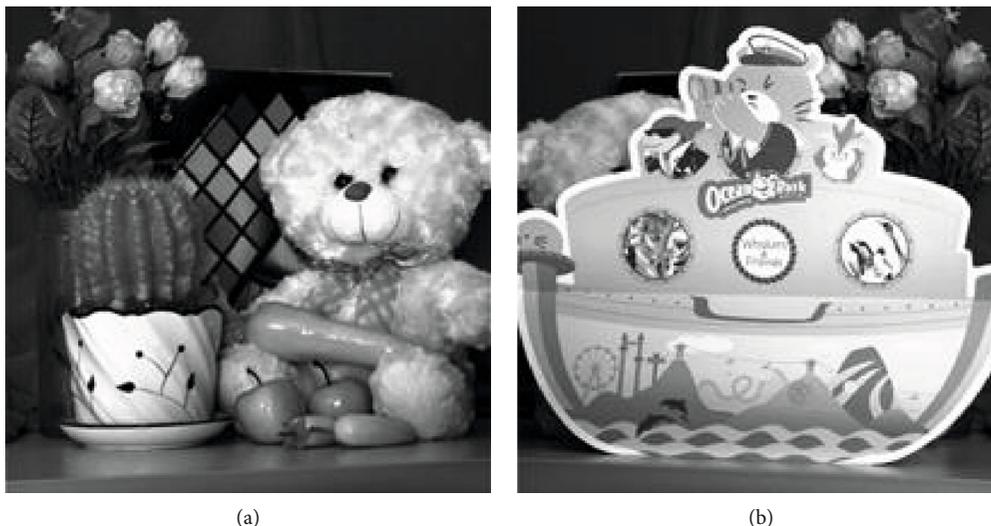


FIGURE 22: Captured photos by the CIS.

TABLE 2: Performance summary of the prototype.

Parameter	Value
Process	180 nm CMOS process
Analog supply	3.3 V
Digital supply	3.3 V
ADC	
Resolution	14 bits
Sample rate	150 kSps
Input range	-2.4 V ~ +2.4 V
DNL	+1.4/-0.25LSB
INL	+1.1/-2.1LSB
SNR	71.7 dB
SFDR	82.91 dB
SINAD	70.28 dB
Power consumption	477.2 uW
PGA	
Gain	3x, 4x, 6x
CIS	
Frame rate	50 fps
Pixel number	1026 × 1024
Pixel pitch	12.5 μm × 12.5 μm
Temporal noise	13.6 e _{rms}
Total power	613 mW

will add one or minus one and the output of DAC will get closer to the target value.

The capacitor array of $V_{REF_BOT} + V_F/128$ calibration pattern is shown in Figure 14 when the capacitor array of $V_{REF_TOP} + V_F/128$ calibration pattern is shown in Figure 15. Both work on the same principle, but the output of DAC in the $V_{REF_TOP} + V_F/128$ calibration is limited. For a differential ADC, the single-ended voltage can only reach V_{REF_TOP} . If the lower plates of capacitors are connected to

the $V_{REF_TOP} + V_F/128$, the results of ADC will exceed the conversion range, which is not accurate.

Assuming that the error of A/D conversion is ± 1 LSB, the digital code D_1 in pattern 1 is equal to 00000010000000 when correcting $V_{REF_BOT} + V_F/128$. If the reference voltage is provided from a relatively small value by pattern 2, the digital code will keep on the 00000010000000, which is not consistent with the real value. However, the D_1 is equal to D_2 , which means the calibration has finished. During the process, the reference voltage self-calibration algorithm does not take on the job, so the reference voltages should change from a large value and the calibration of $V_{REF_TOP} + V_F/128$ is the same as well.

Figure 16 shows the timing block of calibration. PAT_BUS is the bus signal that controls the DAC capacitance switch. When the system is powered on, the signal RESETD resets the digital circuit and then the signal CAL_BEGIN jumps to the high level, which means the calibration module begins to work. The timing of A/D conversion is the same as SAR ADC. A single complete calibration cycle includes 2 settings of switch mode and 2 A/D conversions. Once the second conversion is finished, the signal ADC_DONE will turn to a high level. The compared results of two conversions determine the state of calibration.

If the calibration is over, the signal CAL_OK becomes a high level, which represents the work of one reference voltage calibration has been finished. If the signal CLK_OKs of two references are high level, the whole calibration will be finished and the signal NORMAL will turn to a high level as well.

4. Experimental Results

The CMOS image sensor is fabricated in the 180 nm CMOS process, which is used in remote sensing. Referring to the capacitor array, MIM capacitors are chosen, which have a better match and less affected by temperature compared with others. The pixel array is 1026 × 1024, and the pixel pitch is

TABLE 3: The comparison of previous work.

Parameter	This work	JSSC 16 [15]	TED 16 [16]	ISSCC 18 [17]	JSSC 19 [18]
Process (nm)	180	180	90	90	65
ADC type	SAR	SAR	SAR	SAR	SAR
Supply voltage (V)	3.3	2.8/1.8	2.8/1.2	1.8/1	3.4
Number of pixel	1026 × 1024	160 × 120	1696 × 1212	2560 × 1536	792 × 528
Pixel pitch (μm)	12.5	4.4	1.12	1.5	1.5
Frame rate (fps)	50	100	60	60	170
Resolution (bit)	14	10	12	10	10

12.5 μm × 12.5 μm . The photography of the chip is shown in Figure 17 and the layout of the chip is shown in Figure 18, which are consistent. The pixel array is put in the center of the chip while the readout circuits are placed on the left and right sides. The whole area of the chip is 26.25 × 18.38 mm², where the pixel array occupies the main area.

When it comes to SAR ADC, the performance contains static performance and dynamic performance. Due to the combination of PGA and SAR ADC, the performance of SAR ADC is affected by PGA and the following presentation includes the effect of PGA. The static performance is shown in Figure 19. The DNL is +1.4/-0.25 LSB and the INL is +1.1/-2.1 LSB, which reflects the transient noise. At the sampling speed of 150 ks/s, the SNR and SFDR of the SAR ADC are 71.72 dB and 82.91 dB, respectively, when the frequency of the input signal is 33.3 kHz, which is shown in Figure 20. What is more, the THD of SAR ADC is -75.79 dB and the SINAD is 70.28 dB. In order to verify the stability performance of the proposed prototype, eight chips are tested to get the data, which is presented in Figure 21. The SNR of SAR ADC is from 68.78 dB to 71.71 dB when the ENOB is from 10.8 bits to 11.3 bits, whose performance is relatively stable. The single SAR ADC consumes 477.2 uW.

Figure 22 shows the photos captured by the proposed CIS chips, in which the edge of the subjects can be clearly recognized. What is more, the depth of the background color can be clearly identified, which means the CIS have a good resolution. The performance summary of the prototype is listed in Table 2, including SAR ADC, PGA, and the CIS. The total power consumption of the CIS is about 613 mW.

Compared with the previous works, which are depicted in Table 3, this work adopts the large pixel array and the resolution of SAR ADC is comparatively high without the help of complex calibration and the advanced technology. The proposed CIS chip keeps a balance between the area, resolution, and speed.

5. Conclusions

The 14-bit fully differential SAR ADC with PGA is proposed to apply on CIS. In this paper, the scale of pixel array is large when the three-way PGA is used to sample at the same time to increase the speed. What is more, it also provides three types of gain: 3x, 4x, and 6x. Considering the reset and exposure signal, the fixed deviation is added into the PGA, which makes the input signal distributed evenly on the positive and

negative sides. When it comes to SAR ADC, the two-step scaled-reference voltages are adopted to realize the goal of 14-bit A/D conversion with a 7-bit complementary capacitor array, which is aimed at reducing the number and the area of capacitors. In order to make the precision of reference voltage meet the requirement, the reference voltage self-calibration algorithm is used. During the whole process, the offset and matching accuracy needs to be considered as well. By finishing the above design, the readout circuit realizes the function well and the proposed CIS achieves the goal of high resolution for remote sensing, which are verified in the manufactured chips.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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