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Research Article

Lower Power Design for UHF RF CMOS Circuits Based on the Power Consumption Acuity

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Excessive energy consumption of UHF tag is the bottleneck of energy saving in its wide range of applications. To address this issue, a lower power design for UHF RF CMOS circuits based on power consumption acuity is proposed in this paper. Through in-depth analysis of the static and dynamic power generation principle of UHF RF circuits in the work, the power consumption acuity can be calculated by using the correlation of circuit power and input vector. Subsequently, under the guide of this acuity, the UHF RF CMOS circuits with better energy saving can be designed. Furthermore, according to the performance indicators of EPC CIG2 UHF RFID in UHF identification, the corresponding circuit is designed and implemented. The test results show that the design of UHF RF circuit based on the acuity of power consumption can reduce 35%–40% power consumption.

1. Introduction

Compared to other automatic identification technologies, the most prominent feature of RFID is that it is the fast noncontact technology in identification of moving objects and has high accuracy, security, and resistances to harsh environment, which can also identify multiple recognition objects and so on [1, 2]. RFID technology is widely used in industrial production and all aspects of daily life, such as dangerous goods management, supply chain management, ticketing, security, mall management, and access control [3, 4]. RFID system is different which is depending on its application. However, in general, the tag, interrogator, and processor are the basic three composed parts [5]. With the application of large-scale RF technology, the power consumption of RF chip becomes the focus in this research field [6].

The researches of UHF and microwave bands tag chip got a late start, and most of them have focused in 2003–2006. Among them, the paper about tag chip research published in the literature [7, 8] is the most representative. In Karthaus and Fischer's [9] research, the minimum input RF (radio frequency) power in UHF passive RFID tag chip is only 16.7 μW. It used the read-write EEPROM memory to support the design and the IC was implemented in a 0.5 μm digital two-poly two-metal digital CMOS technology with EEPROM and Schottky diodes. In this paper, it mainly focused on how to improve energy conversion efficiency in the RF energy acquisition, but how to achieve low-power technology in specific circuit was not addressed, and the requirements of Schottky diode did not exist in the standard COMS process. The literature [10] proposed a design of ultralow-cost UHF RFID tag chip for SCM (Supply chain management). The design process was the 0.25 μm standard CMOS, and the nonvolatile memory could be implemented by using of self-adaptive silicon approach in CMOS technology, which could greatly reduce the costs of the chip production. The power matching in the front end of RF analog, the acquisition circuit of RF energy, the energy conversion efficiency, and another key technology were studied in this paper. However, it only established a supply voltage model by using physical method to dynamically adjust the voltage. The threshold could not be changed and the effort was poor. Digital control

logic and memory were accounted for the main part cost and power consumption of RFID tag chip. In the literature [11], the implementation method for embedded memory and digital controller which is suitable for RFID tag chip was investigated. In this paper, the asynchronous circuit was applied to achieve the core of RFID tag chip. However, there is a big restriction that this method is applied in RFID tags chip, since it is not compatible with standard CMOS process and high cost. The literature [12] introduced a new nonvolatile memory to reduce the tag chip's power consumption. It was also the trend of development in future. For example, in July 2005, the memory in the RFID tags chips MB89R119 produced by Fujitsu was 256 Byte FRAM (Ferroelectric Random Access Memory). The power consumption of FRAM was lower than an EEPROM, but its production cost was higher than EEPROM, which is the main reason that FRAM is not widely used in the RFID tag chip currently. The literature designed a UHF passive tag chip, in which the antenna gain was −0.5 dB, reader transmit power was 4 W EIRP, the minimum input power of the tag was 16.7 uw, and the reading distance was about 9.25 m, but in this tag, by using the EEPROM and Schottky diodes technology, the cost of 8 chips was high and power consumption was excessive. In the literature [13], it did not contain EEPROM and digital control circuits, but the data communication rate could reach 10 Mb/s, the simulation consumption was 62.9 uw, and the calculation distance was 6.58 m, while the tape-out was not realized. The literature [14] proposed that the passive RFID system did not have a very reliable security mechanism, which could not guarantee a high reliability of data security, and the data stored within the system was vulnerable to attack mainly because the RFID chip itself and chips in the process of reading and writing data will easily be hacked. In the literature [15], the recognition rate was another problem of RFID system. For the energy intensive of liquid and metal objects, the highest accurate recognition rate of RFID tag only could be reached to around 80%. Obviously, there is a large distance before the recognition rate that can be applied in practice.

The remainder of the paper is organized as follows. Section 2 analyzes the generation principle of static and dynamic power consumption in the work of the high-frequency RF; Section 3 proposes the concept of using power acuity and the view on UHF RF circuit design on the basis of power acuity; Section 4 gives the experiment; and Section 5 is the conclusions.

2. Power Consumption of UHF RF IC Integrated Circuits

Power consumption of CMOS circuit can be divided into static and dynamic power consumption. The static power consumption is caused by the charging and discharging of large parasitic capacitance, which is considered the main source of power consumption in the circuit. The dynamic power consumption is mainly caused by the PH junction leakage current, gate leakage, and subthreshold current of the transistor; it is the important part of the overall power consumption.

2.1. The Dynamic Power Consumption of UHF RF Circuit. Dynamic power consumption is considered to be the main source of power consumption of UHF RF CMOS circuits, which is produced from the handover of tag identification circuit between two stable operating states. It consists of two parts: one is the power consumption of capacitor caused by the charging and discharging of capacitor in RF circuit reverser; the other is the power consumption of moment conduction generated by the instant conduction of tubes T_1 and T_2. Dynamic power consumption, power consumption of capacitor, and power consumption of moment conduction are represented by P_a, P_C, and P_T, respectively; therefore, the equation is as follows: $P_a = P_C + P_T$.

(1) The Power Consumption Generation Principle of Capacitor in UHF RF Circuit. As shown on Figure 1(a), UHF RF CMOS inverter tube normally consists of tubes T_1, T_2 and the load capacitance C_L, where tube T_1 is made by PMOS technology and tube T_2 is made by NMOS technology and C_L is connected to the inverter output end.

According to the working principle of UHF RF inverter, when the jump-behavior of the CMOS inverter input end v_i occurs, the charge and discharge currents will be caused. As it can be seen from Figure 1, the current generation process of charging and discharging is like this: if v_i is 1, tube T_1 turns off, and T_2 turns on, then v_0 is 0, whereas when v_i changes from 1 to 0, tube T_1 is turned from off to on and T_2 is just the opposite; consequently CMOS inverter v_0 will be changed from 0 to 1 and C_L will be charged from V_{DD} through the tube T_1. Conversely, if v_i is 0, tube T_1 turns on, and T_2 turns off, then v_0 is 1; but when v_i changes from 0 to 1, tube T_1 is turned from on to off, and tube T_2 is turned from off to on, then CMOS inverter v_0 will be changed from 1 to 0 and C_L will be charged from V_{DD} through the tube T_2.

In the process of UHF RF circuit operation, the average power consumption P_C generated by charge current i_N and discharge current i_P are shown as follows:

$$P_C = \frac{1}{T}\left[\int_0^{T/2} i_N v_0 dt + \int_{T/2}^{T} i_P \left(V_{DD} - v_0\right) dt\right]. \quad (1)$$

In the above formula, P_C is the average power when the UHF RF circuit is working, T represents a cycle of operation of the circuit, i_N represents the current when the inverter of UHF frequency circuit is charging, i_P represents the current when the inverter of UHF frequency circuit is discharging, V_{DD} denotes the pin elements inside the inverter, and v_0 is the tag in which the value is only 0 or 1; it is used to mark the beginning of the charging or discharging state.

It can be obtained from the principle of charging and discharging of the CMOS inverter: $i_N = -C_L(dv_0/dt)$, $i_P = C_L(dv_0/dt) = -C_L(d(V_{DD} - v_0)/dt)$.

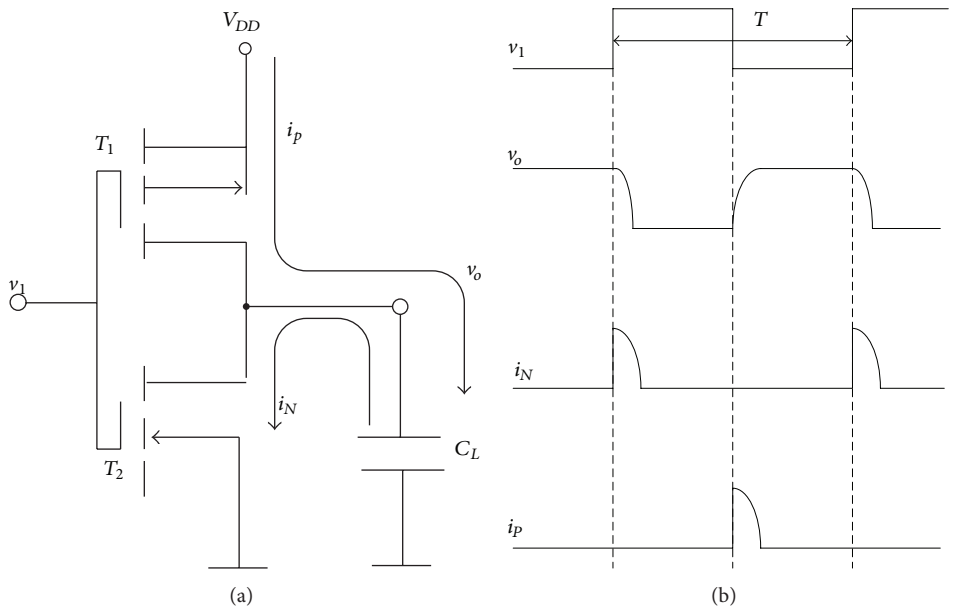

Figure 1: The charging and discharging of the load capacitance from UHF RF inverter.

Therefore, it can be obtained as (2) after i_N and i_P are substituted into (1):

$$P_C = \frac{1}{T}\left[C_L \int_{v_{dd}}^{0} -v_0 dv_0 + C_L \int_{v_{dd}}^{0} -\left(V_{DD} - v_0\right) d\left(V_{DD} - v_0\right)\right] = fC_L\left[\frac{1}{2}V_{DD}^2 + \frac{1}{2}V_{DD}^2\right] = C_L f V_{DD}^2. \quad (2)$$

In the above formula, $f = 1/T$ is the repetition frequency of v_i. From formula (2), it can be seen that the power consumption generated by the charging current or discharge current is $0.5C_LV_{DD}^2$. The power consumption of capacitor C_L is proportional to f and V_{DD}.

(2) The Generated Power Consumption of Instantaneous Conduction. If it takes $V_{DD} > |V_{TP}| + V_{TN}$ and $V_{IH} \approx V_{DD}$, then v_i has the state of $v_I > V_{TN}$, and $V_{DD} - v_I > |V_{TP}|$ in the process of change between high and low electrical levels. The instantaneous current i_T will be produced when tubes T_1 and T_2 are simultaneously turned on. The average value is shown in (3):

$$I_{TAV} = \frac{1}{T}\left[\int_{t_1}^{t_2} i_T dt + t\int_{t_3}^{t_4} i_T dt\right]. \quad (3)$$

Thus, the power consumption of instantaneous conduction is

$$P_T = V_{DD} I_{TAV}. \quad (4)$$

I_{TAV} is related to the frequency of v_i; the higher the f is, the larger the I_{TAV} is. The power consumption of instantaneous conduction P_T is related to the input signal frequency f and the voltage V_{DD}, the higher the frequency f and voltage V_{DD} are, the larger of P_T is. In addition, P_T will also be affected by the rise and fall time of v_i, the power voltage of CMOS tube, and others.

2.2. The Generated Static Power of UHF RF Circuit. When UHF RF circuit is in a steady state, the leakage current of inverter exists, which is the reason of static power generation. If P represents power consumption of inverter, P_D is the static power of inverter, then $P = P_a + P_D = P_C + P_T + P_D$.

It is the solution equation of subthreshold leakage current, while subthreshold leakage current is measured value which cannot be ignored in test circuit simulation of BSIM. BSIM is the industrial standard of test circuit simulation, which is developed by University of California in Berkley and used to test circuit simulation and development of CMOS technology. It is software simulation system based on physics and occupies the characters like preciseness, upgradability, robustness, and language, which can also provide the data of Dc analysis, transient analysis, and Ac analysis of standard circuit. It is the current between source and drain electrode when the circuit is at rest. BSIM model can accurately test the subthreshold leakage current [16], as formula (5) that is shown below:

$$I_{\text{sub}} = \mu_0 \frac{W_{\text{eff}}}{L_{\text{eff}}} v_T^2 \sqrt{\frac{q\varepsilon_s N_{\text{cheff}}}{2\phi_s}}\left(1 - e^{-(V_{ds}/v_T)}\right) \times \exp\left[\frac{V_{gs} - V_t - \gamma V_{sb} + \eta V_{ds}}{n v_T}\right]. \quad (5)$$

In this equation,in the solution process of subthreshold leakage current I_{sub}, V_{gs}, V_{ds}, and V_{sb} are the voltage between grid-source, drain-source, and source-body area of transistor,

respectively. ε_s is the dielectric constant of material of transistor, η is linearized effect factor ofthe leakage inductance of the barrier drop effect, V_{ds} is drain-source voltage, μ_0 is the carrier mobility, W_{eff} and L_{eff} are the effective width and length of transistor, respectively, γ is the linearized influence factor of body area effect, and ϕ_s is surface potential. V_t is the voltage threshold at zero bias. In the calculation process, the thermal availability voltage v_T is unknown; in order to solve the thermal availability voltage effectively, we assumed that Plank's constant is κ, the temperature of carrier is T, and the electron charge is of per unit; then the calculation formula of V_T can be shown as follows: $V_T = \kappa T/q$.

With the deepening of the process, the increasing of gate leakage current is much faster than subthreshold leakage current, which can be indicated in formula (6), where A_g and B_g are associated with the process of physical parameters and ϕ_{ox} is the barrier height of the tunneling electron (or holes).

Consider the following:

$$I_{\text{gate}} = WL_{\text{SDE}}A_g\left(\frac{V_{dd}}{T_{ox}}\right)^2 \times \exp\left\{\frac{-B_g\left[1-\left(1-V_{dd}/\phi_{ox}\right)^{3/2}\right]}{V_{dd}}T_{ox}\right\}. \quad (6)$$

When the strong electric field is formed between reverse-biased P-N junctions, it will form BTBT (Reverse Biased Band to Band Tunneling) leakage current; it can be represented by using formula (7) as follows:

$$I_{\text{BTBT}} = \sum_{k=\text{side, bottom}} WL_k A\frac{\xi_k}{E_g^{1/2}}V_{dd}\exp\left(-BE_g^{3/2}/\xi_k\right). \quad (7)$$

L_{side} and L_{bottom} refer to the sides and bottom length of the P-N junction, ξ_{side} and ξ_{bottom} mean the electric field of the side and bottom of P-N junction, and A and B are the physical parameters associated with the process [17].

3. The Saving Design of UHF RF Circuits Based on the Acuity of Power Consumption

By the preceding theory, the dynamic power of UHF RF circuit is essentially the valid statistics for jump variables of input signal. In this section, the power acuity analysis is researched in-depth. Acuity of power consumption is the correlation degree of power consumption and input vector. It is a very important character of power consumption. It also can be used in low power design. If the acuity of power consumption is considered enough in the design of UHF RF circuit, it can perform an UHF RF circuit with relatively small power consumption.

3.1. The Analysis Method of Power Acuity. The power consumption of UHF RF circuit is generally divided into static and dynamic power consumption. Dynamic power consumption is considered to be the main source of power consumption of UHF RF circuits. It is produced from the switching process of UHF RF circuit between two stable operating states, which consists of two parts: one is the power consumption of capacitor caused by the charging and discharging of capacitor in RF circuit reverser, the other one is the power consumption of moment conduction generated by the instant conduction of T_1 and T_2 tubes. In the ideal case static power should be zero, but this does not mean that the static power is really zero, and actually the static power of UHF RF circuit is due to the leakage current of circuit. The leakage current includes subthreshold current, gate leakage current, and source-drain reverse bias leakage current. The acuity of power consumption is a very important character of power consumption. It means the change degree of power consumption is compared to the input vector. For better understanding, some related definitions and theorems of power acuity are introduced.

The probability of which signal is set to 1 and signal activity are the important indicator to measure power consumption acuity. It can reflect validly the active character of circuit and reflect the power consumption acuity directly. Assume that the action of UHF RF circuit is the 0-1 process of each state, which is represented by the function $g(t)$. Therefore, in this case, the signal probability of which signal is set to 1 and the jumping of rate signal activity can be used to indicate the activities feature of digital circuit. In the time interval $(-T, T)$, T represents the activity period of UHF RF circuit; the unit is μs. The probability of which signal is set to 1 can be defined as follows.

Signal probability can be represented by formula (8) [18]:

$$P(g) = \lim_{T\to\infty}\frac{1}{2T}\int_{-T}^{+T} g(t)\,dt. \quad (8)$$

T represents the activity period of UHF RF circuit; $n_g(T)$ is the activity frequency in time interval $(-T, T)$. Signal activity is defined as follows:

$$A(g) = \lim_{T\to\infty}\frac{n_g(T)}{2T}. \quad (9)$$

By means of analysis, when the random probability of which signal is set to 1 is 1/2, signal activity is 1/2, and the effect of power consumption acuity is the best.

As the same definition, the signal activity of v_i from high level to low level is A_{10}, and the signal activity of v_i from low level to high level is represented by A_{01}. When the random probability of signal probability is 1/2, signal activity is 1/2, and A_{10} and A_{01} values are 1/4.

After defining the signal probability and signal activity, the transmission characters of signal probability and signal activity are further to define.

The transmission characters of the probability which signal is set to 1 are that the signal probability of basic logic gate output signal is represented by a function of the input signal probability. Assume that a two-input gate AND input signal probability is $P_1 \cdot P_2$, then the output signal probability is $P_1 \cdot P_2$. As to the gate OR, assuming its input signal probabilities are P_1 and P_2, respectively, then the output signal probability is $1-(1-P_1)\cdot(1-P_2)$. Propagation of signal activity is to use the transition rate of basic logic gate input signal to indicate the output signal transition rate. After a number of

logic gates, the random signal changes generally have certain regularity.

For n input gate AND, only when the other input $n-1$ is 1, the jump of the n pin can be passed out at the output side; on the contrary, if one of the logic gate values is 0 and keeps the same value, which means that this kind of jumping is blocked. So that other input jumping cannot be passed out smoothly, and 0 is the control value of gate AND, as it can be seen from Figure 2.

After the research on the character of signal probability and signal activity, the transmission characteristics of the basic logic gate transition rate are available. On the basis of this, power consumption acuity can be analyzed. In the circuit design process, the method of low-power design is based on the transmission character of jump rate: if the circuit logic gate with a larger probability is near to the control value, then the design of UHF RF circuits will be with the relatively small power consumption.

The power consumption acuity is the correlation degree of power consumption and input vector. It is a very important character of power consumption.

Power consumption acuity is the changing rate of circuit power consumption probability which is set to 1. The definition is as follows:

$$S_{P(x_i)} = \lim_{\Delta P(x_i)\to 0} \frac{\Delta \text{Power}_{\text{avg}}}{\Delta P(x_i)} = \frac{\partial \text{Power}_{\text{avg}}}{\partial P(x_i)}. \tag{10}$$

In this equation, $S_{P(x_i)}$ is the signal activity of power consumption when the signal is set to 1, $\Delta\text{Power}_{\text{avg}}$ represents the average power consumption per unit, $\Delta P(x_i)$ is the probability of which x_i is set to 1, $\Delta\text{Power}_{\text{avg}}$ represents the partial derivatives of the average dynamic power consumption for x_i, and $\partial P(x_i)$ represents the partial derivative of the transition rate for x_i.

Consider the following:

$$S_{A(x_i)} = \lim_{\Delta A(x_i)\to 0} \frac{\Delta \text{Power}_{\text{avg}}}{\Delta A(x_i)} = \frac{\partial \text{Power}_{\text{avg}}}{\partial A(x_i)}. \tag{11}$$

In this equation, $S_{A(x_i)}$ is the power consumption rate of change on the signal activity, $\Delta\text{Power}_{\text{avg}}$ represents the average dynamic power consumption per unit, and $\partial A(x_i)$ represents the probability of signal activity of x_i.

Through the previous studies on signal probability and signal activity and their transmission characteristics, a simple calculation method for power consumption acuity based on the transmission characteristics of transition rate can be obtained. Firstly, the signal probability and signal activity of given input vector can be adopted to make statistical analysis, and through the transmission character of signal probability, the signal probability of each circuits gate can be calculated. The signal activity of circuit input signal is set to the signal activity of input vectors, and then by the transmission characteristics of signal activity, the input and output signal activity value of the entire logic gate at the input terminal can be obtained. The sum of signal activity values of

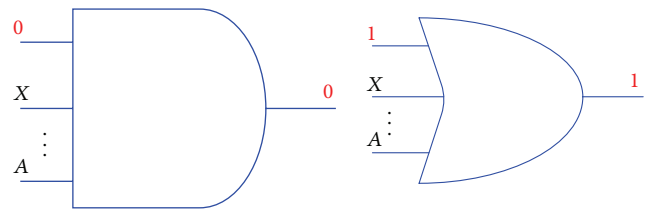

Figure 2: The hopping transfer characteristics of basic logic gates figure.

the input and output is a measure of the power consumption acuity at this terminal:

$$S_{a(x_i)} = \frac{\sum_{\text{fanout gate } g \text{ of } x_i} [\Delta A_{10}(g) + \Delta A_{01}(g)]}{\Delta_{a(x_i)}}. \tag{12}$$

Conclusion 1. The average of dynamic power consumption of UHF RF circuit is correlated with an approximate linear relationship to its signal activity of each gate. By the following derivation, it can be demonstrated that

$$\begin{aligned} P_{\text{avg}} &= \lim_{T\to+\infty} \frac{\sum_{t=1}^{T}\sum_{g=1}^{\varsigma}\{(f_g[(t-1)] \oplus f_g[t]) \cdot F(g)\}}{2T} \\ &= \lim_{T\to+\infty} \frac{\sum_{g=1}^{\varsigma}\{\sum_{t=1}^{T}\{(f_g[(t-1)] \oplus f_g[t]) \cdot F(g)\}\}}{2T} \\ &= \sum_{g=1}^{\varsigma}\left\{\lim_{T\to+\infty} \frac{\sum_{t=1}^{T}[(f_g[(t-1)] \oplus f_g[t])]}{2T} \cdot F(g)\right\} \\ &= \sum_{g=1}^{\varsigma}\left[\frac{n_g(T)}{2T} \cdot F(g)\right] = \sum_{g=1}^{\varsigma}[A_g \cdot F(g)], \end{aligned} \tag{13}$$

wherein, $n_g(T)$ is the total jumping time in the range of gate g and gate $(T, -T)$, $f_g[t]$ is status value that logic gate g is on t. So, by calculating the signal activity of each gate in the circuit, the average dynamic power consumption of circuit can be directly obtained.

Conclusion 2. The linear signal probability of the logic gate can be used to describe the average leakage power of UHF RF circuits, and the derivative process can be shown as follows:

$$\begin{aligned} \text{Leak}_{\text{avg}} &= \lim_{L\to+\infty} \frac{\sum_{i=1}^{L} \text{Leak}(V_i)}{L} \\ &= \lim_{L\to+\infty} \frac{\sum_{i=1}^{L}\sum_{j=1}^{N} I(T_j, V_{j,i}, M_j)}{L} \\ &= \sum_{i=1}^{N} \lim_{L\to+\infty} \frac{\sum_{j=1}^{L} I(T_i, V_{i,j}, M_i)}{L} \\ &= \sum_{i=1}^{N} \lim_{L\to+\infty} \frac{\sum_{j=1}^{2^{M_i}} n_{i,j} I(T_i, S_j, M_i)}{L} \end{aligned}$$

$$= \sum_{i=1}^{N} \sum_{j=1}^{2^{M_{ij}}} \left\{ \lim_{L \to +\infty} \frac{n_{i,j}}{L} I\left(T_i, S_j, M_i\right) \right\}$$

$$= \sum_{i=1}^{N} \sum_{j=1}^{2^{M_i}} \left\{ \text{prob}_{i,j} I\left(T_i, S_j, M_i\right) \right\}. \tag{14}$$

Conclusion 3. Supposing each v_i of UHF RF circuit is independently of one another, and then the circuit power consumption under specific input signal vector can be expressed by the acuity parameter equation linear of its input terminal power consumption, it is as follows:

$$P = P_{\text{avg}} + \sum_{i=1}^{I_{\text{num}}} \Delta a\left(x_{x_i}\right) S_{a(x_i)}. \tag{15}$$

In this formula, i is the variable, and x_i represents the ith logical gate. P_{avg} represents the average power consumption circuit, $S_{a(x_i)}$ is calculated by the previous measure formula, and $\Delta a(x_i)$ is the difference between $a(x_i)$ and signal activity when the a circuit obtains the average power.

3.2. The Design Process of UHF RF Circuit Based on Power Acuity. By using the acuity analysis of the power consumption, the average dynamic and static power consumption of UHF RF circuit can be calculated.

In the process of UHF RF circuit design, in order to reduce power consumption, it can be considered to reduce the power consumption acuity in low power design. If the logic gate of UHF RF circuit exists with a greater probability at the value in the control, the designed UHF RF circuit will have relatively small power consumption compared to the other. According to this conclusion, minimizing the power consumption acuity can make the circuit relatively stable in the UHF RF circuit design. Definitely, the appropriate transformations of the circuit can also lead to lower power requirement in UHF RF circuit design. The acuity in the respective input terminal of the circuit is difference, and one of the greater acuities can be selected as the control parameter, and the phase deviation of the UHF RF can be suppressed effectively. The power consumption is reduced greatly.

4. Experimental Analysis

Experiment circumstance: the experiments about acuity analysis of energy consumption are presented; the analysis is achieved by C++; the platform is VC++6.0, at the same time, running on the Precision T7610 ((Inter xeon processor E5-2620 v2 (6 cores HT, 2.1 GHz Turbo, 15 MB) Windows 7 professional 64 bit, 16 GB (4 × 4 GB) 1866 MHz DDR3 ECC RDIMM, 1 TB, 3.5 inch Serial ATA (7,200 Rpm) HDD, 2 GB NVIDIA Quadro K2000 (2DP & 1DVI-I) (2DP-DVI & 1DVI-VGA adapter))) workstation.

To validate the effectiveness and energy efficiency of the proposed design of UHF RF circuit based on the power consumption acuity, according to the performance indicators of EPC CIG2 UHF RFID and the power acuity theory, a UHF RF front-end circuit with the reset terminal which is suitable for the power-sensitive work is presented here. The general structure is shown in Figure 3; some NOT gates are not shown in the figure, wherein the gate NOT, NAND, and NOR use transmission gate logic to reduce the fosp/snfP asymmetry.

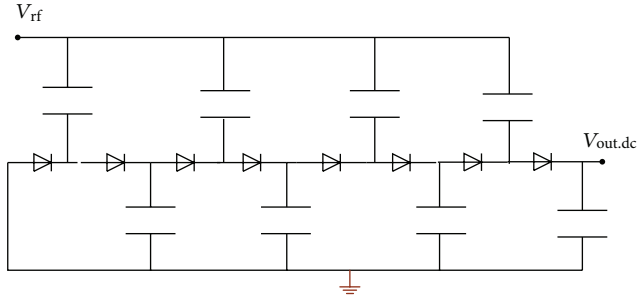

Figure 3: The in front-end rectifier of UHF RF circuit.

Compared with the conventional rectifier, the delay of rectifying portion in the front end of UHF RF is small, and the leakage is low under the same operating voltage. In order to reduce the static and dynamic power consumption of circuit, the increase of circuit drive capability makes the size of the rectifier relatively large; this is not obvious for the small-scale digital circuit. When the circuit is operating in strong inversion region, it can reflect its superiority. Figure 4 shows simulation results of the structural power consumption of the standard rectifier. The simulation is performed in the typical condition, the temperature is 20°C, and the power supply voltage is 300 mv. Figure 4(a) is the result of conventional rectifier; Figure 4(b) is the result of our designed rectifier. It can be seen from Figure 4 that the maximum transient dynamic current (7 sA) of the conventional rectifier is less than the maximum transient dynamic current (20 nA) in this paper. However, the leakage power of the former is obviously larger than the latter.

As it is shown in Table 1, the overall power consumption and the clock frequency of the different process corners and different temperatures in the two rectifier working processes are 10 kHz, respectively.

According to the theory of acuity analysis, in this paper we use the transmission gate structure and increase the width to length ratio of transistor appropriately. The delay of the rectifiers designed in this paper is smaller than the traditional structure for 9.6 us under the same supply voltage and load (the NOT gate in this paper), and the consumption decreases by around 36%.

For a long time statistical analysis, the total loss curve $U_1 - \sum P$ of the UHF RF rectifier circuit and the corresponding total loss error curve $U_1 - \delta(\sum P)$ are shown in Figure 5. As we can see from Figure 5, when the regulating voltage is below 20 V, the total loss error of circuit is increasing; when the regulating voltage is more than 20 V, the loss error of circuit is almost 0. For the reason that operating voltage of the UHF RF circuit is generally higher than 22 V, it can be calculated according to approximate solution, and the total loss is lower.

In accordance with the approximate solution and the exact solution, the optimal voltage curve $T_L - U_1^*$ varies with

Table 1: Energy consumption of different triggers.

Temp	80°C			66°C			−30°C		
Comer	*tt*	*fnsp*	*snfp*	*tt*	*fnsp*	*snfp*	*tt*	*fnsp*	*snfp*
V_{dd}	0.245*V*	0.346*V*	0.325*V*	0.345*V*	0.446*V*	0.425*V*	0.345*V*	0.456*V*	0.416*V*
P_T (DFFI)$_{\text{conventional}}$	1.77*n*	2.8*n*	3.55*n*	211.5*P*	321.44*P*	265.65*P*	234.5*P*	314.44*P*	265.65*P*
P_T (DFFI)$_{\text{thiswork}}$	1.43*n*	1.96*n*	2.77*n*	111.4*P*	223.44*P*	162.46*P*	175.4*P*	267.44*P*	162.46*P*

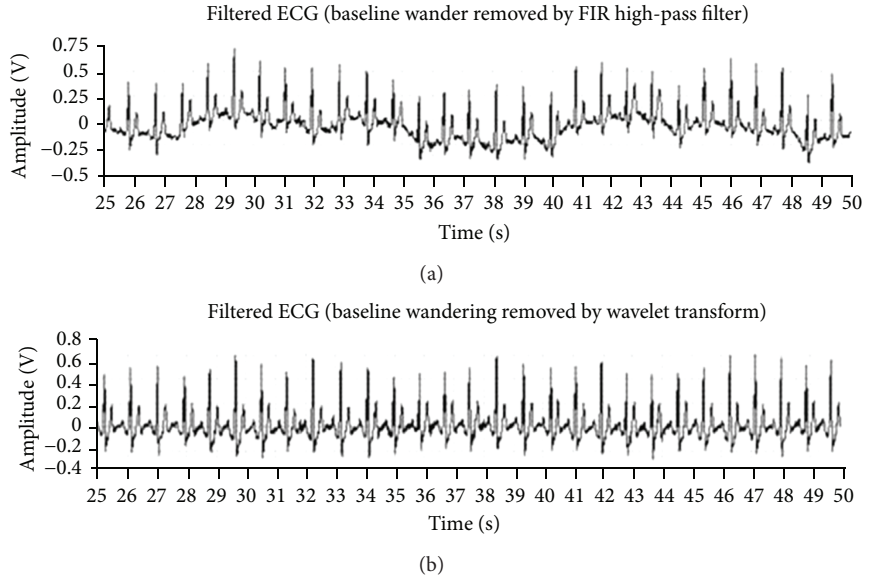

Figure 4: Comparison results of power consumption.

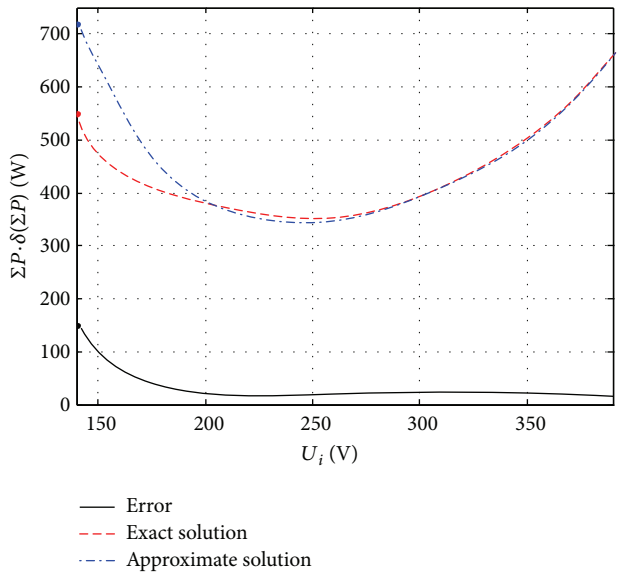

Figure 5: Comparison of minimum loss.

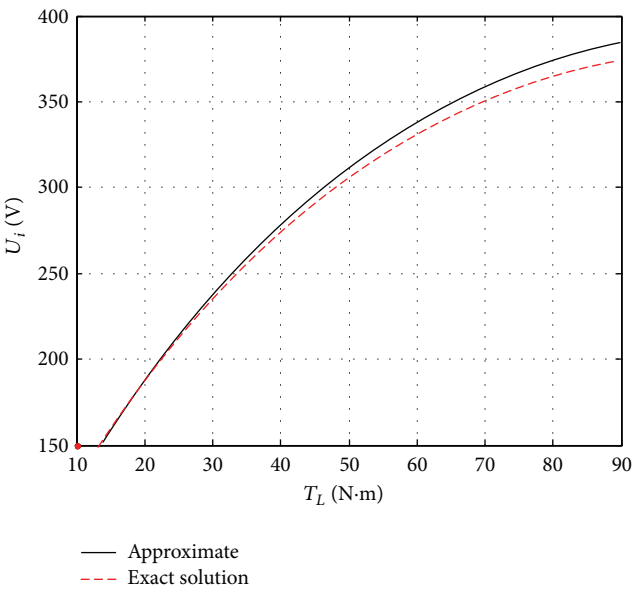

Figure 6: Comparison of optimal voltage.

load can be available. As it can be seen from Figure 6, the optimal voltage error will increase with the changes of load, but in the operating voltage range of UHF RF circuit, the optimal voltage error is calculated to be less than 7 V. Thus, the front-end of UHF RF circuit load is small and the power consumption is relatively low.

5. Conclusions

In this paper, we reviewed the design approach or procedures of UHF tags. In response to the problem of high energy consumption, we present a lower power design for UHF RF CMOS circuit based on the power consumption acuity. The simulation results show that (1) the leakage power of rectifier in this method is obviously less than the conventional rectifier; (2) the delay of the rectifiers designed in this paper is smaller than the traditional structure; (3) the total loss is lower; (4) the design of UHF RF circuit based on the power consumption acuity can reduce 35%–40% power consumption. The proposed design method can be used for various industrial productions, public management and daily life, and so forth, and it will improve the development and efficiency of its application field.

Conflict of Interests

The authors declare that they have no conflict of interests.

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