Research Article

Control Design and Loop Gain Analysis of DC-to-DC Converters Intended for General Load Subsystems

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DC-to-DC converters are usually intended for general applications where the load impedance characteristics are unknown or undefined. This paper establishes the control design procedures for DC-to-DC converters in the absence of any prior knowledge on their load impedance. The proposed control design can be universally adapted to all the DC-to-DC converters regardless of the impedance characteristics of their actual load. This paper also presents the loop gain analysis of the converter combined with an actual load whose impedance characteristics are only available afterward. A graphical analysis method is proposed, which enables us to predict the loop gain of the converter in the presence of an arbitrary load impedance. The validity of the analysis method is demonstrated using a current-mode controlled buck converter coupled with an inductive load, capacitive load, and converter load. Theoretical predictions are verified with both computer simulations and experimental measurements.

1. Introduction

For most practical applications, the load impedance of a converter is unknown or undefined until the actual load is all fabricated and integrated with the DC-to-DC converter, to operate as a complete DC-to-DC power conversion system [1–5]. Accordingly, DC-to-DC converters are to be designed and tested as a standalone module, without any prior information about the load impedance.

When the converter is later connected to the actual load, the converter's performance will be affected by the load impedance. These operational conditions present two major challenges in the control design and performance analysis of DC-to-DC converters for real applications:

- (i) The control should be designed in the absence of any knowledge on the load impedance. The resulting design should offer good performance for DC-to-DC converters as a standalone module.
- (ii) Whenever the information about the load impedance is available, the converter's performance in the real application should be assessed as accurately as possible.

The prime consideration in control design and performance evaluation is the loop gain of the converter. The loop gain carries the whole information about stability and dynamics of the converter. Both the frequency and time-domain performance criteria are all governed by the loop gain characteristics [6].

This paper first presents the control design for DC-to-DC converters whose load impedance characteristics are unspecified. The concept of a *current-sink loaded converter* is adopted in this paper, which allows DC-to-DC converters to be designed using only the DC power requirement. Based on the power stage dynamics, the control design procedures are formulated for good loop gain characteristics of the current-sink loaded converter. The control design procedures can be universally applied to all practical DC-to-DC converters regardless of the impedance characteristics of their actual load.

The later part of the paper assumes that the converter is now connected to an actual load, whose impedance information is available only afterward. The paper then investigates the impacts of the load impedance on the loop gain characteristics. The paper presents a graphical method to

FIGURE 1: Functional representation of DC-to-DC converter feeding general load subsystem.

predict the loop gain of the converter coupled with a practical load subsystem, such as an inductive load, capacitive load, or converter load consisting of a filter stage and another converter downstream.

The validity of the design method and accuracy of the analysis result are demonstrated using a current-mode controlled buck converter. Theoretical predictions are verified with both computer simulations on the small-signal model and experimental measurements on the prototype converter using an impedance analyzer.

2. Current-Sink Loaded Current-Mode Controlled PWM DC-to-DC Converters

The section reviews the concept of the current-sink loaded converter and presents the small-signal model of current-mode controlled pulsewidth modulated (PWM) DC-to-DC converters operating under the current-sink loaded condition.

2.1. Current-Sink Loaded DC-to-DC Converter. Figure 1 is a functional representation of the DC-to-DC converter feeding a general load subsystem. The load subsystem is depicted as a parallel combination of an impedance block $Z_L(s)$ and ideal current sink I_O . $Z_L(s)$ is the impedance of the load subsystem, referred to as the load impedance, and I_O corresponds to the DC output current flowing into the load subsystem.

The information about the load impedance $Z_L(s)$ is usually unavailable at the design stage of the converter. In contrast, the DC output current I_O is always predefined before designing the converter. To cope with the problem of the uncertainty in the load impedance, one can envisage a DC-to-DC converter which delivers the rated DC current to an ideal current sink, thereby implying $Z_L(s) = \infty$ in Figure 1. The resulting converter is termed as the *current-sink loaded DC-to-DC converter*. The current-sink loaded converter is designed as a standalone module and its performance can be tested using a current sink load. The performance of the converter coupled with an actual load will be treated in Section 4.

2.2. Current-Sink Loaded Current-Mode Controlled PWM DC-to-DC Converters. Current mode control is the most prevailing control scheme [7–15] for PWM DC-to-DC power converters. Figure 2(a) shows a schematic diagram of the current-mode controlled PWM converter feeding a current sink load. Figure 2(a) could represent all the three basic

PWM converters, the buck converter, boost converter, and buck/boost converter, with the respective power stage connections. The converter consists of a power stage, pulsewidth modulation (PWM) block, current sensing network (CSN) for current mode control, and voltage feedback circuit. Figure 2(b) is the small-signal model of Figure 2(a), obtained by replacing the active-passive switch pair with the PWM switch model [16] and by replacing the PWM and CSN blocks with their small-signal models [7].

Because $Z_L(s) = \infty$ for the current sink load, the power stage is terminated with the filter capacitor in series with its equivalent series resistance (esr). Nonetheless, the output current I_O flowing into the current sink is embedded into the power stage model as a DC load parameter

$$R_{DC} = \frac{V_O}{I_O} \quad (1)$$

which determines the coefficient of the dependent current source in the PWM switch model.

3. Power Stage Dynamics, Control Design, and Performance of Current-Sink Loaded Converter

Using the small-signal model in Figure 2(b), this section presents the power stage dynamics and control design of the current-sink loaded converter. The power stage dynamics of the current-sink loaded converter are discussed in comparison with those of the converter coupled with an arbitrary load impedance. This provides insights on the versatility of the proposed control design. In ensuing discussions, the converter coupled with the load impedance is referred to as an *impedance loaded converter*. This section also illustrates the theoretical and experimental performance of the current-sink loaded current-mode controlled buck converter.

3.1. Control-to-Output Transfer Function. The vital information to the control design is the control-to-output transfer function, $G_{vci}(s) = \hat{v}_o/\hat{v}_{con}$, evaluated under the condition that only the current loop is closed and the connection to the voltage feedback compensation $F_v(s)$ is broken at Point A in Figure 2(b). The knowledge of this transfer function allows us to design both the current loop and voltage feedback circuit for good loop gain characteristics. By applying the Mason's

FIGURE 2: Current-sink loaded and current-mode controlled PWM DC-to-DC converter. (a) The diagram represents the buck converter with connections $\{a - X \ p - Y \ i - Z\}$, the boost converter with $\{i - X \ a - Y \ p - Z\}$, and the buck/boost converter with $\{a - X \ i - Y \ p - Z\}$. The CSN represents the current sensing network and PWM is the pulsewidth modulation block. (b) Small-signal model: D is the duty ratio and $R_D = R_i + DD'R_e$ and $V_D = V_{ap} + (D - D')R_e I_L$ with $D' = 1 - D$, $R_e = 0$ for the buck converter, and $R_e = R_c$ for the boost and buck/boost converters. Consider $I_L = V_O/R_{DC}$ for the buck converter, $I_L = -V_O/(R_{DC}D')$ for the boost converter, and $I_L = V_O/(R_{DC}D')$ for the buck/boost converter with $R_{DC} = V_O/I_O$. R_i represents the DC gain of CSN. $H_e(s)$ is the sampling gain of CSN: $H_e(s) = 1 + s/(\omega_n Q_z) + s^2/\omega_n^2$ with $Q_z = -2/\pi$ and $\omega_n = \pi/T_s$, where T_s is the switching period. $F_m = 1/((S_n + S_e)T_s)$ is the modulator gain [7] of PWM block with S_n : on-time slope of the sensed inductor current, $S_n = V_{ai}R_i/L$, and S_e : slope of the compensation ramp. k_r/k_f represents the feedback/feedforward gain of current mode control [7]: $k_r = T_s R_i/(2L)$ for the buck converter, $k_r = (1 - D)^2 T_s R_i/(2L)$ for the boost and buck/boost converters, $k_f = -T_s R_i/(2L)$ for the boost converter, and $k_f = -DT_s R_i(1 - D/2)/L$ for the buck and buck/boost converters. $F_v(s) = Z_2/Z_1$ is the voltage feedback compensation.

gain rule to Figure 2(b) with $\hat{v}_s = \hat{i}_o = 0$, the control-to-output transfer function is determined as

$$G_{vci}(s) = \frac{\hat{v}_o}{\hat{v}_{con}} = \frac{F_m(\hat{v}_o/\hat{d})}{1 - k_r F_m(\hat{v}_o/\hat{d}) + R_i H_e(s) F_m(\hat{i}_L/\hat{d})}. \quad (2)$$

Although the $G_{vci}(s)$ expression is rather involved, it can be reduced to a simple expression [17, 18] with some practical assumptions on power stage parameters and operational conditions. By following the procedures presented in [17], $G_{vci}(s)$ is casted into the following third-order approximation:

$$G_{vci} \approx K_{vc} \frac{(1 + s/\omega_{esr})(1 - s/\omega_{rhp})}{(1 + s/\omega_{pl})(1 + s/Q_p \omega_n + s^2/\omega_n^2)}. \quad (3)$$

The noticeable feature of the transfer function is the quadratic term in the denominator. The quadratic term, originated from the sampling effects of the current mode control [7], introduces a double pole at half the switching frequency; $\omega_n = \pi/T_s$.

Table 1 shows the parameters appearing in the $G_{vci}(s)$ expression of the three basic current-sink loaded PWM converters. This table also presents the expressions of $G_{vci}(s)$ for the impedance loaded PWM converters, in order to

contrast the small-signal dynamics of the current-sink loaded and impedance loaded converters. The load impedance is denoted as $Z_L(s)$ in the $G_{vci}(s)$ expressions of the impedance loaded converters.

The structure of the transfer function and the expressions for ω_{esr} , Q_p , and ω_n are the same in both the current-sink loaded and impedance loaded converters. However, the K_{vc} and ω_{pl} expressions are different, thereby highlighting the distinct power stage dynamics of the current-sink loaded converters. The DC load parameter, $R_{DC} = V_O/I_O$, does not appear in the $G_{vci}(s)$ expressions for the buck converter. This is the unique feature of the buck converter [6], which is not the case for the boost and buck/boost converters. For the boost and buck/boost converters, R_{DC} emerges as a key parameter of power stage transfer functions.

3.2. Control Design Procedures. The most important role of $G_{vci}(s)$ lies in the control design. Referring to Figure 2(b), the loop gain of the current-sink loaded converter becomes

$$T_{mC} = G_{vci}(s) F_v(s), \quad (4)$$

where $F_v(s)$ is the voltage feedback compensation. The subscript C in T_{mC} signifies that the converter is current-sink loaded. Based on the $G_{vci}(s)$ structure, $F_v(s)$ can be designed for the loop gain offering both stability and good performance of the current-sink loaded converter.

Figure 3 shows the asymptotic plots for $|G_{vci}|$ and loop gain $|T_{mC}|$. The $|G_{vci}|$ plot is constructed with the conditions

TABLE 1: Control-to-output transfer function for current-sink loaded and impedance loaded PWM converters.

$G_{vci}(s) = K_{vc} \frac{(1 - s/\omega_{rhp})(1 + s/\omega_{esr})}{(1 + s/\omega_{pl})(1 + s/Q_p\omega_n + s^2/\omega_n^2)}$ $\text{with } \omega_{esr} = 1/CR_c, \omega_n = \pi/T_s, Q_p = 1/\pi(m_c D' - 0.5), \text{ and } m_c = 1 + S_e/S_n$		
	Current-sink loaded case	Impedance loaded case
Buck converter	$K_{vc} = \frac{L}{R_i T_s (m_c D' - 0.5)}$ $\omega_{pl} = \frac{T_s (m_c D' - 0.5)}{LC}$ $\omega_{rhp} = \infty$	$K_{vc} = \frac{L}{R_i T_s (m_c D' - 0.5) + L/Z_L}$ $\omega_{pl} = \frac{T_s (m_c D' - 0.5) + L/Z_L}{LC}$ $\omega_{rhp} = \infty$
Boost converter	$K_{vc} = \frac{L}{R_i T_s D'^2 (m_c - 0.5) + L/R_{DC} D'}$ $\omega_{pl} = \frac{T_s D'^2 (m_c - 0.5) + L/R_{DC} D'}{LC/D'}$ $\omega_{rhp} = \frac{R_{DC} D'^2}{L}$	$K_{vc} = \frac{L}{R_i T_s D'^2 (m_c - 0.5) + 2L/Z_L D'}$ $\omega_{pl} = \frac{T_s D'^2 (m_c - 0.5) + 2L/Z_L D'}{LC/D'}$ $\omega_{rhp} = \frac{R_{DC} D'^2}{L}$
Buck/boost converter	$K_{vc} = \frac{L}{R_i T_s D'^2 (m_c - 0.5) + DL/R_{DC} D'}$ $\omega_{pl} = \frac{T_s D'^2 (m_c - 0.5) + DL/R_{DC} D'}{LC/D'}$ $\omega_{rhp} = \frac{R_{DC} D'^2}{DL}$	$K_{vc} = \frac{L}{R_i T_s D'^2 (m_c - 0.5) + (1 + D)L/Z_L D'}$ $\omega_{pl} = \frac{T_s D'^2 (m_c - 0.5) + (1 + D)L/Z_L D'}{LC/D'}$ $\omega_{rhp} = \frac{R_{DC} D'^2}{DL}$

Z_L is the load impedance.

FIGURE 3: Asymptotic plots for $|G_{vci}|$ and $|T_{mC}|$ with two-pole one-zero voltage feedback compensation.

$\omega_{pl} \ll \omega_{esr} \ll \omega_n$ and $0.5 < Q_p$. The double pole at ω_n produces a peaking in $|G_{vci}|$ by the amount of $20 \log Q_p$.

The loop gain plot $|T_{mC}|$ assumes a two-pole one-zero circuit for the voltage feedback compensation

$$F_v(s) = \frac{K_v (1 + s/\omega_{zc})}{s (1 + s/\omega_{pc})}. \quad (5)$$

The compensation pole ω_{pc} is located at the right-half plane (rhp) zero, ω_{rhp} . The compensation zero ω_{zc} is placed after ω_{pl} but before the loop gain crossover frequency, ω_{cr} .

The $|T_{mC}|$ shows the desirable -20 dB/dec slope for wide frequency range and crosses the 0 dB line at high frequencies. As shown in Figure 3, the peaking of $20 \log Q_p$ also occurs in $|T_{mC}|$ at $\omega_n = \pi/T_s$. If the peaking is large, $|T_{mC}|$

could exceed the 0 dB line at ω_n , thereby destabilizing the converter [7]. Accordingly, the quality factor Q_p should be properly controlled to avoid instability due to an excessive peaking. Based on the preceding discussions, the control design procedures are formulated as follows.

Current Loop Design

- (1) Determine the CSN gain, R_i , such that $i_{L\text{peak}} R_i < V_{\max}$ where $i_{L\text{peak}}$ is the peak value of the inductor current and $V_{\max}$ is the maximum allowable input voltage of the PWM block.
- (2) Determine the slope of the compensation ramp, S_e , to provide a quality factor in the range $0.3 < Q_p < 1.3$ for the double pole at $\omega_n = \pi/T_s$.

Voltage Feedback Compensation Design

- (1) Place the compensation pole ω_{pc} at the lowest frequency among the rhp zero, esr zero, and half the switching frequency: $\omega_{pc} = \min \{\omega_{rhp}, \omega_{esr}, 0.5 \omega_s\}$.
- (2) Locate the compensation zero ω_{zc} at the frequencies higher than ω_{pl} but lower than the loop gain crossover frequency: $\omega_{pl} < \omega_{zc} < \omega_{cr}$.
- (3) Select the 0 dB crossover frequency of the loop gain and determine the integrator gain K_v required for the selected ω_{cr} . It is recommended that $\omega_{cr} = (0.3 - 1.0)\omega_{esr}$ for buck converters and $\omega_{cr} = (0.1 - 0.3)\omega_{rhp}$ for boost and buck/boost converters [6]. From Figure 3, the following relationship is formulated:

$$\left(20 \log K_{vc} + 20 \log \frac{K_v}{\omega_{pl}} \right) - 40 \log \frac{\omega_{zc}}{\omega_{pl}} - 20 \log \frac{\omega_{cr}}{\omega_{zc}} = 0 \text{ dB} \quad (6)$$

leading to the design equation for the integrator gain K_v

$$\frac{K_{vc} K_v}{\omega_{pl}} \left(\frac{\omega_{pl}}{\omega_{zc}} \right)^2 \frac{\omega_{zc}}{\omega_{cr}} = 1 \implies K_v = \frac{\omega_{zc} \omega_{cr}}{K_{vc} \omega_{pl}}. \quad (7)$$

Invariance of Control Design Procedures. The control-to-output transfer functions of the current-sink loaded converters differ from those of the impedance loaded converters. Nonetheless, when the control design procedures established for the current-sink loaded converters are adapted to the impedance loaded converters, the resulting design is practically identical to that of the current-sink loaded converter case. Furthermore, it can be shown that the control parameters are determined independently from the load impedance characteristics. This implies that the proposed control design can be universally adapted to all practical DC-to-DC converters, irrespective of the load impedance characteristics. This *invariance* of the control design procedures is justified by the following facts:

- (i) The criteria for the current loop design are independent of the load impedance and thus remain the same in both the current-sink loaded and impedance loaded cases.
- (ii) The design guidelines for the voltage feedback compensation also remain unchanged. In particular, the integrator gain K_v is selected as

$$K_v = \frac{\omega_{zc} \omega_{cr}}{K_{vc} \omega_{pl}} \quad (8)$$

for both the cases, where ω_{zc} is the desired position of the compensation zero and ω_{cr} is the target for the crossover frequency. Because the selection of ω_{zc} and ω_{cr} would be the same for the two cases, K_v will be identical if the product of K_{vc} and ω_{pl} remains invariant in the two cases.

- (iii) From the $G_{vci}(s)$ expressions in Table 1, the following relationship can be inferred:

$$K_{vc} \omega_{pl} \approx \begin{cases} \frac{1}{R_i C}, & \text{for buck converter,} \\ \frac{D'}{R_i C}, & \text{for boost and buck/boost converters} \end{cases} \quad (9)$$

for both the current-sink loaded and impedance loaded converters. The condition for the above approximations can readily be seen from Table 1. For most practical cases, the relationships of (9) are valid and all the control parameters become the same for the current-sink loaded and impedance loaded converters. Accordingly, the control parameters are all determined independently from the load impedance.

3.3. Design and Performance of Current-Sink Loaded Buck Converter. The preceding design procedures are verified using a current-sink loaded current-mode controlled buck converter. The circuit parameters and operational conditions of the buck converter are $V_s = 16 \text{ V}$, $V_O = 4 \text{ V}$, $I_O = 1 \text{ A}$, $T_s = 20 \times 10^{-6} \text{ s}$, $L = 40 \mu\text{H}$, $R_l = 0.1 \Omega$, $C = 470 \mu\text{F}$, $R_c = 0.1 \Omega$, $D = 0.25$, and $R_{DC} = 1 \Omega$. The small-signal parameters and operational conditions are $\omega_{esr} = 2\pi \cdot 3.39 \times 10^3 \text{ rad/s}$, $D = 0.25$, $\omega_s = 2\pi \cdot 50 \times 10^3 \text{ rad/s}$, $V_{max} = 5.0 \text{ V}$, and $i_{Lpeak} = 4.75 \text{ A}$. Based on these data, the control design is executed as follows:

- (1) CSN gain:

$$R_i < \frac{V_{max}}{i_{Lpeak}} = \frac{5.0}{4.75} = 1.05 \Omega \implies R_i = 0.67 \Omega. \quad (10)$$

- (2) Quality factor of double pole:

$$Q_p = \frac{1}{\pi ((1 + S_e/S_n) D' - 0.5)} = 1 \quad (11)$$

$$\text{with } S_n = 2.01 \times 10^5 \text{ V/s} \implies S_e = 1.84 \times 10^4 \text{ V/s.}$$

- (3) Compensation pole: $\omega_{pc} = \omega_{esr} = 2\pi \cdot 3.39 \times 10^3 \text{ rad/s}$.

- (4) Compensation zero: $\omega_{zc} = 2\pi \cdot 928 \text{ rad/s}$.

- (5) Loop gain crossover frequency: $\omega_{cr} = \omega_{esr} = 2\pi \cdot 3.39 \times 10^3 \text{ rad/s}$.

- (6) Integrator gain:

$$\begin{aligned} K_v &= \frac{\omega_{zc} \omega_{cr}}{K_{vc} \omega_{pl}} \quad \text{with } K_{vc} = 9.38, \quad \omega_{pl} = 2\pi \cdot 54 \text{ rad/s} \\ \implies K_v &= \frac{(2\pi \cdot 928) (2\pi \cdot 3.39 \times 10^3)}{9.38 (2\pi \cdot 54)} \\ &= 3.91 \times 10^4. \end{aligned} \quad (12)$$

(7) Voltage feedback compensation:

$$F_v(s) = \frac{3.91 \times 10^4 (1 + s/(2\pi \cdot 928))}{s(1 + s/(2\pi \cdot 3.39 \times 10^3))}. \quad (13)$$

(8) Voltage feedback circuit: $R_1 = 10 \text{ k}\Omega$

$$\Rightarrow R_2 = 92.3 \text{ k}\Omega,$$

$$C_2 = 1.86 \text{ nF}, \quad (14)$$

$$C_3 = 0.70 \text{ nF}.$$

The performance of the current-sink loaded buck converter is evaluated with both computer simulations and experimental measurements. The small-signal model in Figure 2(b) is used for the computer simulations. On the other hand, an HP4194A impedance analyzer is used for experimental measurements. The loop gain T_{mC} is displayed in Figure 4. The $|T_{mC}|$ crosses the 0 dB line at $\omega_{cr} = 2\pi \cdot 3.2 \times 10^3 \text{ rad/s}$ with a phase margin of 70° . Figure 5 shows the output impedance of the current-sink loaded buck converter, referred to as Z_{oC} hereafter. $|Z_{oC}|$ starts from a very small value and increases linearly until it saturates at $20 \log R_c = 20 \log 0.1 = -20 \text{ dB}$. The small-signal predictions show a close match with the experimental measurements at low and mid frequencies. On the other hand, there are apparent discrepancies at high frequencies. These discrepancies are due to the high-frequency switching noises and parasitic circuit components, which are ignored in the small-signal analysis but affect the experimental data. The discrepancies usually occur at high frequencies, well above the loop gain crossover frequency, and do not interfere with the evaluation of the closed-loop performance of the converter [6]. These discrepancies will be observed, only at high frequencies, in all the forthcoming transfer functions.

4. Loop Gain Analysis of Loaded Converter

When the current-sink loaded converter is coupled with a real load subsystem, the loop gain will be affected by the load impedance $Z_L(s)$. This section investigates the loop gain characteristics of the buck converter coupled with practical load subsystems.

4.1. Loop Gain Expression of Loaded Converter. The converter connected to a real load subsystem is now denoted as the *loaded converter*. Figure 6 is a small-signal functional model of the loaded converter, formulated for the loop gain analysis. The model is created by merging the current-sink loaded converter and the load impedance $Z_L(s)$. In Figure 6, the voltage feedback loop is broken for the loop gain evaluation. Therefore, Z'_{oC} represents the open-loop output impedance of the current-sink loaded converter. The loop gain of the loaded converter T_{mL} is evaluated as

$$\begin{aligned} T_{mL}(s) &= (-) \frac{\hat{v}_x}{\hat{v}_{con}} = G_{vci}(s) \frac{Z_L(s)}{Z_L(s) + Z'_{oC}} F_v(s) \\ &= \frac{G_{vci}(s) F_v(s)}{1 + Z'_{oC}/Z_L(s)}. \end{aligned} \quad (15)$$

FIGURE 4: Loop gain of current-sink loaded buck converter.

FIGURE 5: Output impedance of current-sink loaded buck converter.

By incorporating the well-known relationship among the closed-loop output impedance Z_{oC} , open-loop output impedance Z'_{oC} , and loop gain, $T_{mC} = G_{vci}(s)F_v(s)$, of the current-sink loaded converter:

$$Z_{oC} = \frac{Z'_{oC}}{1 + T_{mC}}. \quad (16)$$

FIGURE 6: Small-signal functional model of loaded converter.

FIGURE 7: Load subsystems. (a) Inductive load. (b) Capacitive load. (c) Converter load.

Expression (15) is rearranged as

$$T_{mL}(s) = \frac{T_{mC}}{1 + (1 + T_{mC})(Z_{oC}/Z_L(s))}. \quad (17)$$

The impedance ratio $Z_{oC}/Z_L(s)$ is referred to as the *equivalent loop gain*, $T_{eq}(s)$, in the previous publications [18, 19]. The loop gain expression (17) is now written as

$$T_{mL}(s) = \frac{T_{mC}}{1 + T_{eq}(s) + T_{mC}T_{eq}(s)} \quad (18)$$

using the notation of $T_{eq}(s) = Z_{oC}/Z_L(s)$. The loop gain will remain unaffected by the load impedance, $T_{mL} \approx T_{mC}$, when the conditions $|T_{eq}| \ll 1$ and $|T_{mC}T_{eq}| \ll 1$ are simultaneously met for all frequencies. However, this requirement is not always satisfied in practice and the loop gain characteristics are thus to be altered by $Z_L(s)$. Expression (18) will be used to investigate the loop gain of the experimental buck converter connected to various practical load subsystems.

4.2. Loop Gain Characteristics with Practical Load Subsystem.

Figure 7 depicts the load subsystems used for the loop gain analysis. For generality of the analysis, three different types of load subsystems are considered: an inductive load, capacitive load, and converter load. The inductive and capacitive loads are the circuit representations of practical passive loads. The converter load denotes the load subsystem consisting of a filter stage and another buck converter downstream. The converter load is frequently found in distributed power applications [1, 20–22] where cascaded converters and filter stages are employed together for an efficient and reliable power conversion. Details about the converter load and its input impedance were provided in [20, 23].

FIGURE 8: Output impedance of current-sink loaded buck converter $|Z_{oC}|$ and input impedance of load subsystems $|Z_L|$.

Figure 8 illustrates the load impedances $|Z_L|$ of the three load subsystems, in comparison with the output impedance of the current-sink loaded buck converter, $|Z_{oC}|$. All the load impedances converge to the DC load parameter, $R_{DC} = V_O/I_O = 1 \Omega$, at low frequencies. However, each input impedance shows quite a distinctive pattern at mid and high frequencies, thereby signifying different impacts on the converter loop gain.

The loop gain of the converter with the three load subsystems, $T_{mL}(s)$, and the loop gain of the current-sink

FIGURE 9: Loop gain characteristics of buck converter with different load subsystems.

loaded converter, T_{mC} , are shown in Figure 9. For each load subsystem, $T_{mL}(s)$ substantially deviates from T_{mC} and reveals very complex behavior. Nonetheless, the pattern of $T_{mL}(s)$ can be accurately predicted from loop gain expression (18).

The results of the loop gain analysis are given in Figure 10, which illustrates $|T_{mC}|$, $|T_{eq}|$, $|T_{mC}T_{eq}|$, and $|T_{mL}|$, all involved with loop gain expression (18). Referring to Figure 10, the loop gain analysis for each load subsystem is performed as follows:

- (i) *Inductive load*: Figure 10(a) illustrates the case with the inductive load. The condition $|T_{eq}| \ll 1$ is well-satisfied for all frequencies. However, $|T_{mC}T_{eq}| \ll 1$ is not met at low frequencies. For the frequencies below ω_b where the conditions $|T_{eq}| \ll 1$ and $1 \ll |T_{mC}T_{eq}|$ prevail, the loop gain is given by

$$\begin{aligned} T_{mL}(s) &= \frac{T_{mC}}{1 + T_{eq}(s) + T_{mC}T_{eq}(s)} \approx \frac{T_{mC}}{1 + T_{mC}T_{eq}(s)} \\ &\approx \frac{T_{mC}}{T_{mC}T_{eq}(s)} = \frac{1}{T_{eq}(s)}. \end{aligned} \quad (19)$$

Thus, $|T_{mL}|$ follows the mirror image of $|T_{eq}|$ reflected on the 0 dB axis, as confirmed in Figure 10(a). On the other hand, for the frequencies beyond ω_b where the conditions $|T_{eq}| \ll 1$ and $|T_{mC}T_{eq}| \ll 1$ are met, the loop gain of the loaded converter trails the loop gain of the current-sink loaded converter; $T_{mL}(s) \approx T_{mC}$. Both the theoretical and experimental loop gains closely follow the predictions of this analysis.

- (ii) *Capacitive load*: The loop gain analysis for the capacitive load is shown in Figure 10(b). For frequencies below the crossover frequency of T_{mC} , ω_{cr} , the conditions $1 \ll |T_{mC}T_{eq}|$ and $|T_{eq}| \ll |T_{mC}T_{eq}|$ hold true. The loop gain is given by

$$\begin{aligned} T_{mL}(s) &= \frac{T_{mC}}{1 + T_{eq}(s) + T_{mC}T_{eq}(s)} \\ &\approx \frac{T_{mC}}{T_{eq}(s) + T_{mC}T_{eq}(s)} \approx \frac{T_{mC}}{T_{mC}T_{eq}(s)} \\ &= \frac{1}{T_{eq}(s)} \end{aligned} \quad (20)$$

for the frequencies in the range $0 < \omega < \omega_{cr}$. For higher frequencies, the conditions $1 \ll |T_{eq}|$ and $|T_{mC}T_{eq}| \ll |T_{eq}|$ are effective. These conditions simplify loop gain expression to

$$\begin{aligned} T_{mL}(s) &= \frac{T_{mC}}{1 + T_{eq}(s) + T_{mC}T_{eq}(s)} \\ &\approx \frac{T_{mC}}{T_{eq}(s) + T_{mC}T_{eq}(s)} \approx \frac{T_{mC}}{T_{eq}(s)} \end{aligned} \quad (21)$$

thus indicating the loop gain magnitude is formed by the relationship of $|T_{mL}| = |T_{mC}| - |T_{eq}|$. The loop gain plots well support this analysis.

- (iii) *Converter load*: Figure 10(c) is the case for the converter load. For the frequencies below ω_{cr} where the conditions $|T_{eq}| \ll |T_{mC}T_{eq}|$ and $1 \ll |T_{mC}T_{eq}|$ are met, the loop gain is given by

$$\begin{aligned} T_{mL}(s) &= \frac{T_{mC}}{1 + T_{eq}(s) + T_{mC}T_{eq}(s)} \approx \frac{T_{mC}}{1 + T_{mC}T_{eq}(s)} \\ &\approx \frac{T_{mC}}{T_{mC}T_{eq}(s)} = \frac{1}{T_{eq}(s)}. \end{aligned} \quad (22)$$

The same as the previous two cases, $|T_{mL}|$ traces the mirror image of $|T_{eq}|$ for wide frequency range. For the frequencies beyond ω_{cr} , $|T_{mL}|$ tracks $|T_{mC}|$ with the conditions $|T_{eq}| \ll |T_{mC}T_{eq}|$ and $1 \ll |T_{mC}T_{eq}|$. Figure 10(c) reveals a close correspondence to this analysis.

The loop gains exhibit distinctive behavior with different load subsystems. With the inductive load, $|T_{mL}|$ follows the mirror image of $|T_{eq}|$ only at low frequencies. In contrast, with the capacitive and converter loads, $|T_{mL}|$ trails the mirror image of $|T_{eq}|$ until the crossover frequency of $|T_{mC}|$, showing complex yet predictable pattern for a wide frequency range.

5. Conclusions

Traditionally, the design and analysis of DC-to-DC converters have been performed based on the assumption that the

FIGURE 10: Loop gain analysis. (a) Inductive load. (b) Capacitive load. (c) Converter load.

converters are feeding a resistive load. However, the load of a DC-to-DC converter is commonly a combination of circuit components, electrical devices, and even other converters downstream. The load is characterized by its nonresistive impedance. Furthermore, the load impedance characteristics are unknown or undefined at the design stage of the DC-to-DC converter.

This paper presented the control design method, which relies on only the DC power requirement without any prior presumption on the load impedance. Based on the small-signal analysis, the control design procedures are formulated to achieve good loop gain characteristics. The proposed control design can be generally adapted to all the PWM converters regardless of the impedance characteristics of their actual load. Theoretical and practical details about the control

design are all demonstrated using a current-mode controlled buck converter.

The current paper also presented the loop gain analysis of the current-mode controlled buck converter, which is designed based on only the DC power requirement and later combined with various practical load subsystems. This paper established a general graphical method to predict and interpret the loop gain of the converter combined with an inductive, capacitive, or converter load. The inductive load revealed that the loop gain follows the mirror image of the equivalent loop gain only at low frequencies. In contrast, with the capacitive and converter loads, the loop gain trails the mirror image of the equivalent loop gain until the crossover frequency of the loop gain of the current-sink loaded converter.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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