Research Article

Voltage Balancing Method on Expert System for 51-Level MMC in High Voltage Direct Current Transmission

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The Modular Multilevel Converters (MMC) have been a spotlight for the high voltage and high power transmission systems. In the VSC-HVDC (High Voltage Direct Current based on Voltage Source Converter) transmission system, the energy of DC link is stored in the distributed capacitors, and the difference of capacitors in parameters and charge rates causes capacitor voltage balance which affects the safety and stability of HVDC system. A method of MMC based on the expert system for reducing the frequency of the submodules (SMs) of the IGBT switching frequency is proposed. Firstly, MMC with 51 levels for HVDC is designed. Secondly, the nearest level control (NLC) for 51-level MMC is introduced. Thirdly, a modified capacitor voltage balancing method based on expert system for MMC-based HVDC transmission system is proposed. Finally, a simulation platform for 51-level Modular Multilevel Converter is constructed by using MATLAB/SIMULINK. The results indicate that the strategy proposed reduces the switching frequency on the premise of keeping submodule voltage basically identical, which greatly reduces the power losses for MMC-HVDC system.

1. Introduction

In High Voltage Direct Current applications, high voltage long distance transmission is often constrained by the fact that the components of power electronics are limited in terms of rated voltage. The two-level VSC has been widely accepted in practical engineering applications. However, its use in high voltage and high power occasions is limited for the reason of the high switching losses and poor voltage quality. Compared with two-level VSC, MMC has much lower switching frequency and switching losses, which makes the MMC suitable for applications in HVDC. The MMC is the most promising topology for its modularity and discretion in HVDC systems. In recent years, there are many topologies of MMC, modulation, capacitor voltage balancing, circulation suppression, the research results of the fault tolerant technique, and so forth [1–5]; however, there still exist challenges in the field of control, such as capacitor voltage balancing and circulating current control [6]. In HVDC systems, the energy of DC side is storage capacitors in amounts of submodules in series,

so the DC voltage control of converter not only requires controlling the total DC voltage, but also needs capacitor voltage balance control. A method for each module, respectively, for closed-loop control voltage balancing strategies is proposed in [7]. A new structure of MMC with its modulation scheme and equalizing strategy is put forward and medium voltage ripple suppression strategies are investigated in [8]. A modified CPS-SPWM method with the reduced-switching frequency (RSF) voltage balancing algorithm is proposed in [9]; however, the modulation strategy of it requires massive calculation. An intelligent distributed control of MMC is adopted in [10]; “The Tortoise and the Hare” sorting method shows the fast response for HVDC system.

In practice, the MMC-HVDC contains hundreds of submodules for reaching high voltage; therefore, compared with the 21-level MMC in [9, 11], a 51-level converter is adopted in this paper to make the simulation closer to the engineering practice. In this paper, a voltage balancing control based on expert system for 51-level MMC is proposed, which reduces the switching frequency besides balancing the

FIGURE 1: Topology of MMC-HVDC converter.

capacitor voltage. The expert system is as a framework for voltage balancing strategies for MMC-based HVDC system.

This paper is organized as follows: In Section 2, a description of the MMC-HVDC structure and its operation is introduced. In Section 3, the modified NLC method is explained. A modified capacitor voltage balancing method based on expert system is proposed in Section 4. The simulations results are described in Section 5.

2. MMC-HVDC System

2.1. Basic Structure. A typical structure of MMC-HVDC is DC to three-phase AC converter, as shown in Figure 1 [6]. Among them, each phase consists of two bridge legs, DC system connects to the end of upper arm and the lower arm of each phase, and the three-phase AC system connects to the neutral point of each phase (a, b, and c). The three-phase MMC consists of two arms per phase-leg, where each arm comprises N series-connected, nominally identical SMs, and a series inductor L_0 . The upper (lower) arm of three phase-legs is represented by subscript “ p ” (“ n ”).

The topology shown in Figure 2 is the structure of each SM. A submodule, shown in Figure 2, consists of two IGBTs connected in a half-bridge topology with a capacitor across the devices to be used as an energy storage and supply device. Also shown is the fact that the output terminals that actually

FIGURE 2: Structure of SM.

FIGURE 3: Equivalent circuit of the MMC for phase- j .

connect to the converter are across the lower IGBT. The SM is equivalent to a controlled voltage source: when T1 is on and T2 is off, the output voltage U_{SM} is U_c ; when T1 is on and T2 is off, the output voltage is 0. The phase-leg is composed of N identical SMs in series, and its total output voltage U_{SM} is equal to the sum of the output voltage of each module unit.

2.2. Operation Principle. Figure 3 shows the equivalent circuit of the MMC for phase- j , and the mathematical relationship of the output current, circulating current, and the arm current is [10]

$$i_{p,j} = \frac{i_{dc}}{3} + i_{circ,j} + \frac{i_j}{2}, \quad (1a)$$

$$i_{n,j} = \frac{i_{dc}}{3} + i_{circ,j} - \frac{i_j}{2}, \quad (1b)$$

where $i_{p,j}$ and $i_{n,j}$ are the upper and lower current of phase- j , respectively, and $i_{circ,j}$ represents the circulating current within phase- j , i_j represents the ac-side current of phase- j , and i_{dc} is the current in the DC link.

The mathematical equations that govern the dynamic behavior of the MMC phase- j are

$$\frac{V_{dc}}{2} - v_{p,j} = L_0 \frac{di_{p,j}}{dt} + R_0 i_{p,j} + v_{jo}, \quad (2a)$$

$$\frac{V_{dc}}{2} - v_{n,j} = L_0 \frac{di_{n,j}}{dt} + R_0 i_{n,j} + v_{jo}, \quad (2b)$$

where $v_{p,j}$ and $v_{n,j}$ represent the upper and lower arm voltages and v_{jo} represents the output voltage of phase- j . The numerical value of v_{jo} is

$$v_{jo} = \frac{v_{n,j} - v_{p,j}}{2} - \frac{R_0}{2} i_j - \frac{L_0}{2} \frac{di_j}{dt}. \quad (3)$$

3. NLC Method with Voltage Balancing

3.1. The Modulation of MMC-HVDC. There are lots of modulation methods for multilevel converters; if the number of SMs is small, high frequency PWM multilevel modulation methods such as space vector modulation (SVM), phase disposition PWM (PD-PWM), and carrier phase shift PWM (CPS-PWM) are commonly used in order to meet the requirement of harmonic. However, as the SM number is increasing, the PWM modulation becomes more and more complex. Huge number of SMs of HVDC makes PWM with high frequency and increases switching losses. Compared with PWM modulation, the level modulation has lower switching frequency, so it has lower switching loss, and it is easier to realize without complex pulse width control. For 51-level MMC in HVDC system, the harmonic content of output is very low. The basic principle of NLC modulation mode has been discussed in detail [10]. The control processes of the three phase are independent, based on different reference wave. Reference wave can be obtained by comparing with existing output voltage levels. Given a voltage reference u_{ref} , the desired nearest output voltage level N_{on} can be determined with

$$N_{on} = \frac{1}{U_c} \text{round}(u_{ref}), \quad (4)$$

where U_c represents the SM capacitor voltage. The nearest integer function $\text{round}(x)$ is defined such that the integer is closest to x . The implementation of the nearest voltage level generation with voltage balancing algorithm is illustrated in Figure 4.

3.2. The Conventional Voltage Balancing Method. The principle traditional voltage balancing method is to keep the minimum voltage deviation of the submodules at any time. According to the different direction of the arm current i_{arm} , the corresponding submodules are inserted or bypassed.

If $i_{arm} > 0$, that is, the SM is charging, the N_{on} SMs with lowest voltages will be inserted. Conversely, N_{on} submodules with the highest voltages will be inserted. It does not take the former states of SMs into consideration, which makes the voltage deviation narrow in a short period of time performs well in the case that the voltage deviation

FIGURE 4: Control diagram of NLC with modified voltage balancing method.

of the submodule is much greater than the allowable value. However, the disadvantage of this method is that the frequent rotation between the SMs causes much switching losses to the converter and increases the power losses of HVDC system; the method is not adoptable in all cases.

Without considering lower device switching frequency, conventional voltage balancing control only lays emphasis on the results of the capacitor voltage sequence, which ignores the initial state of submodule. The target of conventional method is to strictly control the difference between capacitor voltage values of the submodules. In practice, the goal of balance control is not completely pursuit of the consistency of each capacitor voltage; relatively small fluctuations of capacitor voltage can be allowed.

3.3. The Design of Expert System. Define $\Delta U_{c \max}$ as the maximum voltage deviation within a phase-leg:

$$\Delta U_{c \max} = U_{c \max} - U_{c \min}, \quad (5)$$

where $U_{c \max}$, $U_{c \min}$ represent the maximum voltage and the minimum voltage of the phase-leg, respectively. Set the voltage deviation reference $\Delta U_{c \max \text{ref}}$ as the allowable maximum voltage deviation.

Knowledge Base

Step 1. IF $N_{on} = 0$, THEN switch off all the SMs; IF $N_{on} = 50$, THEN switch on all the SMs; IF $0 < N_{on} < 50$, THEN turn to next step.

Step 2. In interface engine: make comparison of $\Delta U_{c \max}$ and $\Delta U_{c \max \text{ref}}$.

IF $\Delta U_{c \max} < \Delta U_{c \max \text{ref}}$, THEN adopt modified voltage balancing method.

IF $\Delta U_{c \max} \geq \Delta U_{c \max \text{ref}}$, THEN adopt traditional voltage balancing method.

The voltage balancing method is modified as follows.

It takes the desired nearest output voltage level N_{on} , arm current i_{arm} , and the nearest output voltage level of last control cycle $N_{on \text{old}}$ for data acquisition.

IF $N_{on} = N_{on \text{old}}$, THEN keep current gate signals.

IF $N_{on} > N_{on \text{old}}$ and $i_{arm} > 0$, THEN switch on $(N_{on} - N_{on \text{old}})$ SMs with the lowest voltages among $(50 - N_{on \text{old}})$ off-states SMs.

FIGURE 5: The framework of MMC-HVDC in MATLAB/SIMULINK.

IF $N_{on} > N_{on_old}$ and $i_{arm} \leq 0$, THEN switch on ($N_{on} - N_{on_old}$) SMs with the highest voltages among ($50 - N_{on_old}$) off-states SMs.

IF $N_{on} < N_{on_old}$ and $i_{arm} > 0$, THEN switch off $|N_{on} - N_{on_old}|$ SMs with the highest voltages among N_{on_old} on-states SMs.

IF $N_{on} < N_{on_old}$ and $i_{arm} \leq 0$, THEN switch off $|N_{on} - N_{on_old}|$ SMs with the lowest voltages among N_{on_old} on-states SMs.

4. Simulation Results

To validate the effectiveness of the voltage balancing method proposed in this paper, the 51-level MMC-HVDC transmission system simulation platform in MATLAB/SIMULINK is taken, and specific parameters are as follows: the number of submodule N is 50; the converter rating for the open-loop simulation is considered as 1000 MVA with the total dc voltage V_{dc} being 400 kV. The arm inductor is 0.009 H, and the load resistance is 19.44 Ω .

The simulation framework of MMC-HVDC is shown in Figure 5 and the SM in the MATLAB/SIMULINK is shown in Figure 6. In Figure 5, the arms of three phase are represented

FIGURE 6: The SM structure in MATLAB/SIMULINK.

by “A, B, and C”. From Figure 6, it can be seen that the signals of the upper IGBT and the lower IGBT in half-bridge structure are completely opposite.

Figures 7 and 8 show the three-phase output line-to-line voltages and the output phase currents, respectively. The output of the converter is similar to sine wave with low harmonic distortion, which shows the high power quality of 51-level NLC and proves the control strategy is suitable for HVDC system.

FIGURE 7: Line-to-line voltages.

FIGURE 8: Phase currents.

Figures 9(a) and 9(b) are the capacitor voltages of the 50 SMs in the upper arm and lower arm of phase-A with different voltage balancing method. From the figure, it can be seen that the capacitor voltages in the 51-level MMC in HVDC system are with high synchronism. As can be seen, the capacitor voltages of the two different methods are homogeneous in Figures 9(a) and 9(b). The capacitor voltages are of perfect synchronism, as in Figure 9. It can be seen from Figures 9(b) and 9(c) that although the consistency of the SM capacitor voltages is lower than the traditional trigger method, the maximum voltage deviation of the submodules of the same time is within a small range.

Figures 10(a) and 10(b) are the gates signals of phase-B with conventional voltage balancing method and modified voltage balancing method based on expert system, respectively. It is proved that the proposed modified voltage balancing method based on expert system reduces the switching frequency of MMC.

5. Conclusion

This paper develops an expert system for RSF voltage balancing method for MMC-HVDC. In this paper, a 51-level MMC for HVDC is designed, whose voltage level is close to engineering practice. The output of converter is with low total harmonic distortion, where there is no need for power filters

FIGURE 9: Capacitor voltage with different voltage balancing method. (a) Conventional voltage balancing method. (b) Modified voltage balancing method based on expert system. (c) Modified voltage balancing method based on expert system (local zoom).

and the device cost of HVDC is reduced. A NLC method with conventional voltage balancing method is introduced. To reduce the switching frequency of converter, a modified voltage balancing method on expert system is proposed. The simulation results validate the fact that the modified voltage balancing method is effective, which reduces the switching frequency and balances the SM voltage. The simulation results show that the 51-level converter works effectively in HVDC systems.

Competing Interests

The authors declare that they have no competing interests.

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FIGURE 10: Gate signals of phase-B with different modulation schemes. (a) Conventional voltage balancing method. (b) Modified voltage balancing based on expert system.

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