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Research Article

Power Supply- and Temperature-Aware I/O Buffer Model for Signal-Power Integrity Simulation

Wael Dghais[1,2] **Malek Souilem**[2] **Fakhreddine Zayer**[1] **and Abdelkader Chaari**[2,3]

[1]*Department of Electronics, Institut Supérieur des Sciences Appliquées et de Technologie Sousse, Université de Sousse 4003, Tunisia*
[2]*Laboratoire d'Ingenierie des Systemes Industriels et des Energies Renouvelables (LISIER), University of Tunis, ENSIT, Tunis, Tunisia*
[3]*National Higher Engineering School of Tunis (ENSIT), University of Tunis, 5 Av. Taha Husein, BP 56, 1008 Tunis, Tunisia*

Correspondence should be addressed to Wael Dghais; waeldghais@ua.pt

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This paper presents the development and evaluation of a large-signal equivalent circuit model that accounts for the power supply fluctuation and temperature variation of I/O buffers circuit designed based on the fully depleted silicon on insulator (FDSOI) 28 nm process for signal-power integrity (SPI) simulation. A solid electrical analysis based on the working mechanisms of the nominal I/O buffer information specification- (IBIS-) like model is presented to support the derivation of an accurate and computationally efficient behavioral model that captures the essential effects of the power supply bouncing under temperature variation. The formulation and extraction of the Lagrange interpolating polynomial are investigated to extend the nominal equivalent circuit model. The generated behavioral model is implemented using the Newton-Neville's formula and validated in simultaneous switching output buffers (SSO) scenario under temperature variation. The numerical results show a good prediction accuracy of the time domain voltage and current waveforms as well as the eye diagram of the high-speed communication I/O link while speeding-up the transient simulation compared to the transistor level model.

1. Introduction

Signal and power integrity (SPI) assessment of high-speed digital communication input-output (I/O) links is important for the design analysis and verification of modern memory and chip-to-chip interfaces in order to figure out SPI problems at an early design stage [1–11]. The high-speed I/O link design has to also comply with certain specifications regarding the process, supply voltage, and temperature variation to obtain the target performance [12–16]. In fact, the temperature and power supply variations not only reduce the noise margins of digital circuits but also change the nanoscale output buffer/driver's operating point and dynamics [4, 5, 9, 10, 14]. The I/O link is composed by an active nonlinear part representing the I/O buffers that bond the die to the passive package and the printed circuit board (PCB) interconnects in order to ensure reliable high-speed digital data communication between the integrated circuits (ICs) I/O ports of the DDR memory and CPU, as depicted in Figure 1. Since, I/O buffers are designed based on transistors, they are characterized by a nonlinear dynamic behavior which is usually the main cause of signal distortions under high data rate transmission (i.e., short rise and fall time) and simultaneous switching output (SSO) buffers which generate the bouncing of the on-chip supply and ground voltages (e.g., simultaneous switching noise (SSN)) [1, 5, 8].

The SPI assessment is carried out by means of transient simulation in order to consider the interaction between the nonlinear dynamic output impedance of the semiconductor devices (i.e., I/O buffers) with the linear dynamic effect of the RLC package and the PCB traces. Transistor level (TL) models of the I/O buffers are impractical to use for evaluating the electrical performance of the high-speed digital I/O link because they reveal the detailed TL information about the design's process and their transient simulation is time-consuming in the electronic design automation (EDA) tools, [2–6, 15, 16]. Besides, the manufacturers are often reluctant to release SPICE TL models for general use [7–11]. Therefore, the effective behavioral modelling of I/O buffers is an appealing alternative that hides the intellectual property (IP) of the I/O

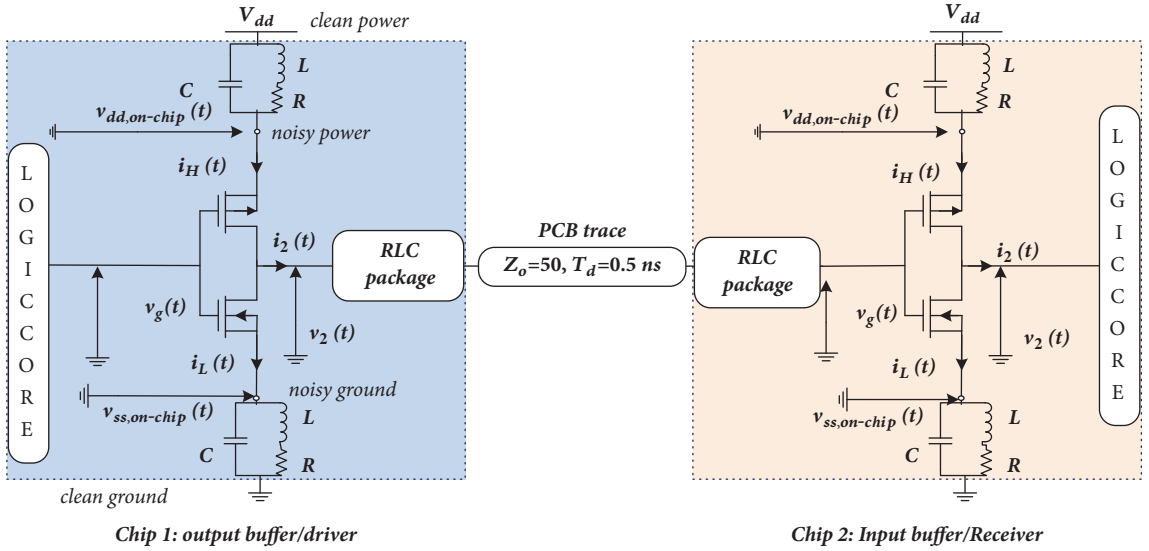

Figure 1: Active and passive main parts composing the high-speed digital communication I/O link from the transmitter (driver) and the receiver.

buffer's circuit and enables a fast and accurate SPI transient simulation of the high-speed communication I/O links, [1–16].

Recently, power-aware I/O buffer models were proposed by enhancing the nonlinear parametric and surrogate modelling approaches, [4–9] for SPI analysis. The parametric behavioral modelling algorithm proposed in [5] and the modified equivalent circuit and table-based I/O buffer information specification- (IBIS-) like model presented in [9] are valid only for a designed I/O buffer physical structure where the predriver logic and the driver's last stage are powered by separate supply and ground voltages (e.g., V_{DD}/V_{ss}). This assumption limits the validity of the proposed modelling solution and requires an a priori knowledge of the I/O device physical structure which may be difficult to access due to IP issues. Besides, the parametric models rely on the use of curve fitting techniques and nonlinear optimization algorithms (e.g., Levenberg–Marquardt) for parameters identification during the training phase [3–6, 17, 18]. They differ from the nonlinear physics-based and industry standard IBIS modelling algorithm in the model's formulation, extraction, and implementation steps [7–10]. Moreover, both modelling approaches cannot directly simulate continuous temperature variation because they rely only on the use of discrete process–supply voltage–temperature data [4, 7].

This paper proposes an extended equivalent circuit behavioral model which simultaneously considers the signal and power integrity domains and allows the incorporation of temperature variation. A general behavioral modelling framework based on the generation procedure of a nonlinear dynamic I/O buffer IBIS-like model is described while disregarding any assumption on the powering techniques (i.e., supply and ground voltages) used in the I/O buffer circuit structure. In fact, the predriver and the driver's last stage can be connected to the same power supply; therefore, the SSN affects both the predriver and driver's last stage circuits. In fact, the analysis based on the nonlinear electrical and physical mechanisms of the I/O buffers enables the effective integration of the power supply voltage fluctuation and continuous temperature variation in the equivalent circuit IBIS-like model's functions. Accordingly, the interpolated model is derived, based on Lagrange polynomial representation, to explicitly incorporate the power supply port's voltage and temperature variables. The accuracy and computational efficiency of the extended model formulation are ensured by numerically implementing the interpolating polynomials as Newton-Neville's representations.

The rest of this paper is organized as follows. Section 2 details the mathematical model structure derivation and analysis in order to effectively include both the continuous power supply fluctuation and the temperature variation through Lagrange polynomial interpolation. Section 3 presents the model implementation and numerical validation results. Finally, conclusions are drawn in Section 4.

2. Model Derivation and Extraction

2.1. Power-Aware Model. At the nominal power, V_{DD}, and ground, V_{SS}, supply voltage values, the nominal model relating the driver's output current, $i_2(t)$, to the voltage controlling variables is

$$i_2(t) = i_H\left(v_g(t), v_2(t), \frac{d}{dt}\right) + i_L\left(v_g(t), v_2(t), \frac{d}{dt}\right) \quad (1)$$

where $i_H(t)$ and $i_L(t)$ represent the pull-up (PU) and pull-down (PD) currents, respectively. The gate voltage $v_g(t)$ controls the activation of the PU and PD transistors according to the bit sequence transmitted by the logic core, $v_1(t)$. d/dt stands for the time derivative dependence of the output currents $i_H(t)$ and $i_L(t)$ on the input voltage electrical variables $v_g(t)$ and $v_2(t)$, as presented in Figure 2.

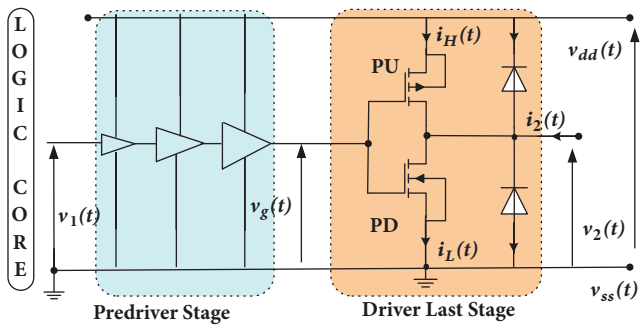

FIGURE 2: Three-port driver's circuit and its relevant electric variables.

As SSO occurs, the large voltage bouncing of the on-chip, $v_{dd}(t)$, affects the input controlling voltage differences of the PMOS transistors, for instance, $v_{sg}(t) = v_{dd}(t) - v_g(t)$. This gate–source modulation effect [9], in which the nominal IBIS model fails to predict, changes the operation regions of the PU and PD transistors network (i.e., from saturation to linear and vice versa) of the driver's last stage and also of the predriver's stage logic if they are powered by the same power/ground supply voltages, as shown in Figure 2 [5–9]. It is worth noting that $v_{dd}(t)$ continues fluctuating even after the input voltage, $v_1(t)$, reaches the steady states. In order to develop a model coupled with observable electrical variables, which provides reassurance in validating the model for packaged devices, the mathematical formulation of the extended two-piece IBIS-like model is derived based on the interpolation of multidimensional function (2). It captures the gate modulation effect to accurately predict the current and voltage waveforms at the power and ground nodes [2, 9]:

$$i_2(t) = \sum_{j=L,H} w_j\left(x_{1j}(t)\right) \cdot f_j\left(x_{2j}(t)\right) \tag{2}$$

where $x_{1H}(t) = v_{dd}(t) - v_g(t)$, $x_{2H}(t) = v_{dd}(t) - v_2(t)$, $x_{1L}(t) = v_g(t) - v_{ss}(t)$, and $x_{2L}(t) = v_2(t) - v_{ss}(t)$. $f_L(\cdot)$ and $f_H(\cdot)$ are nonlinear dynamic functions describing the driver's last stage large-signal output admittances of when its input, $v_1(t)$, is kept at high ('H') or low ('L') logic states, respectively. $f_L(\cdot)$ and $f_H(\cdot)$ functions can be parameterized by means of spline functions with finite time differences [2], rational function [3], and artificial neural networks [5, 6, 18, 19]. Then, they are fitted with the acquired input-output transient voltage and current when the output voltage excitation is connected between the power-output port and ground-output port [3–6]. Another approach consists in postulating the model as a physics-based nonlinear equivalent circuit model (3) [7–9]. This nonlinear current-charge (I-Q) output admittance model for the PU and PD driver's last stage extends the standard IBIS model and can be implemented as lookup tables (LUTs).

$$f_j(t) = G_j\left(x_{2j}(t)\right) + C_j\left(x_{2j}(t)\right)\frac{dx_{2j}(t)}{dt}; \quad j = L, H. \tag{3}$$

where $G_j(\cdot)$ function models the single-input single output (SISO) conduction output current-voltage (I-V) relationship and $C_j(\cdot)$ captures the displacement current modelled as a SISO capacitance-voltage (C-V) relationship [7–9] for the PU and PD devices under supply voltages variation. The single-valued $G_j(\cdot)$ and $C_j(\cdot)$ functions can be extracted from pulsed time domain measurements [10] or from bias-dependent scattering (S) parameters measurements [20], when the excitation voltages are connected between the power/ground and output nodes. These nonlinear capacitances capture the nonlinear delay of the power supply signals propagating from power node till the output port during and after the switching activities of the input port (e.g., after the input signal rising and the falling edges).

Once the functions modelling the driver's last stage PU and PD admittances are extracted, the step input describing functions (SDFs), $w_L(t)$ and $w_H(t)$, that describe the input port (i.e., predriver) nonlinear switching characteristics under input rising transition (i.e., bit pattern '01') and falling transition (i.e., bit pattern '10') are extracted by means of a linear inversion [2–9]. The single extracted SDFs, at the nominal power supply voltage, V_{DD}, is capable of accurately predicting the predriver's analog switching when it is powered by a separate supply voltage from the driver's last stage because the SSN will not affect the predriver's operation and its electrical characteristics [4–9].

Since the IBIS nominal model relies on the use of a fixed SISO I-V functions with a linear output capacitance under a fixed low and high dc states of the input voltage (i.e., $v_1(t)$ or $v_g(t)$), the SPI modelling task consists of including the gate modulation effects in the IBIS model formulation. For instance, the double-input single output (DISO) I-V surface characteristics of the PU and PD networks can be approximated as a multiplication of two SISO nonlinear functions for an NMOS FDSOI transistor, for instance, as

$$i_{ds}\left(v_{gs}, v_{ds}\right) = \frac{Q\left(v_{gs}\right)}{I_{sat}} \cdot G\left(v_{ds}\right) \tag{4}$$

where I_{sat} is the saturation current defined for an NMOS transistor as $i_{ds}(v_{gs} = V_{DD}, v_{ds} = V_{DD})$. The nonlinear transfer characteristic of the transistor is defined as $Q(v_{gs}) = i_{ds}(v_{gs} = V_{DD}, v_{ds})$. The transistor output characteristic is defined as $G(v_{ds}) = i_{ds}(v_{gs} = V_{DD}, v_{ds})$. The extraction of the static $Q(v_{gs})$ and $G(v_{ds})$ is detailed in [9]. The contribution of the extended IBIS-like power supply-aware model consists of proposing an interpolating based technique that approximates the gate modulation nonlinear static, $Q(v_{gs})$, and dynamic effects on both the predriver and driver's last stage. For instance, the nonlinear large-signal transfer characteristic i_{ds} vs v_{gs} of the predriver's stage, shown in Figure 3, can be approximated or interpolated by a second- or higher-order polynomial expansion for the accurate prediction of the new SDFs according to the change of the on-chip $v_{dd}(t)$ (i.e., gate modulation effect). However, the adequate selection of the polynomial order should be investigated in order to find the best compromise between the developed model's accuracy and computational cost.

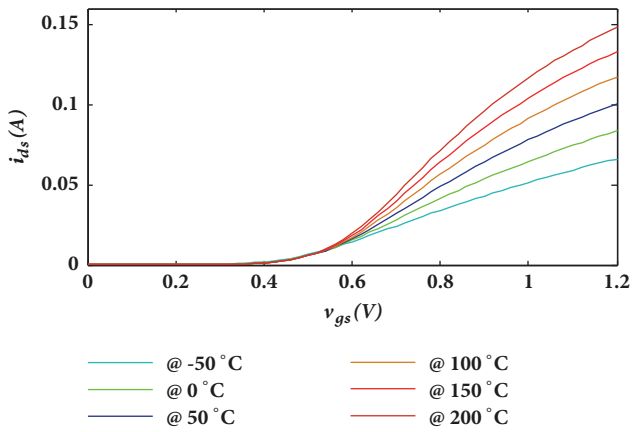

FIGURE 3: Nonlinear i_{ds} *vs* v_{gs} transfer characteristic of an n-channel FDSOI transistor at different temperature values.

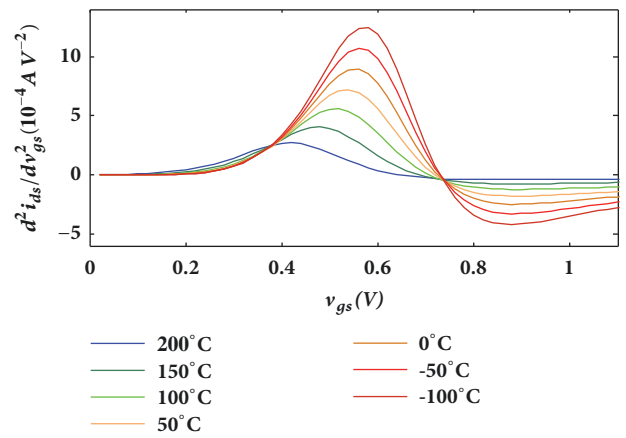

FIGURE 4: Derivative of the transconductance d^2i_{ds}/dv_{gs}^2 for different temperature values.

Since the gate voltage is not accessible (i.e., not observable), the static effect of $v_{dd}(t)$ variation on the SDFs is captured by sweeping the value of V_{DD} in order to account for large power supply variation aside from the nominal value. Therefore, the additional SDFs which are extracted, from the transient TL simulation, for different dc power supply, $V_{DD,k}$, are interpolated by means of the Lagrange polynomial. Accordingly, the new scaling coefficient of SDFs is computed during the transient simulation of the driver's circuit.

$$w_j\left(t, v_{dd}\left(t\right)\right) = \sum_{i=0}^{m} L_{i,j}\left(v_{dd}\left(t\right)\right) \cdot w_j\left(t, V_{DD,i}\right)$$

$$L_{i,j}\left(v_{dd}\left(t\right)\right) = \prod_{k=0, i\neq k}^{m} \frac{\left(v_{dd}\left(t\right) - V_{DD,k}\right)}{\left(V_{DD,i} - V_{DD,k}\right)} \tag{5}$$

$$j = L, H$$

where $w_j(t, V_{DD,i})$ stands for the extracted SDFs that capture the predriver's switching dynamics for different values of the power supply $V_{DD,i}$. $L_{i,j}(v_{dd}(t))$ is the m^{th} Lagrange polynomial order which is chosen such that

$$L_{i,j}\left(V_{DD,s}\right) = \begin{cases} 0, & s \neq i \\ 1, & s = i \end{cases} \qquad j = L, H \tag{6}$$

The Lagrange interpolation (5) leads to a nonlinear model which is explicit in $v_{dd}(t)$ for the PU and PD devices. It is used to predict the SDFs functions that emulate the gate voltage modulation under SSO. However, the a priori decided polynomial degree affects the number of required SDFs that increase the characterization and identification times while increasing the memory space and running complexity of the proposed model. Furthermore, the sampling points of the Lagrange interpolating polynomial are taken according to predriver's conductance function nonlinearity and Chebyshev nodes in order to avoid oscillation and obtain a good interpolation accuracy with a low polynomial order [15, 16].

2.2. Temperature-Aware Model. In order to efficiently integrate the temperature variation in the power supply-aware driver's model, the dependence of the threshold voltage, V_{th}, on the temperature is extracted, based on the dc simulation data of the TL model, though the second derivative of the short channel FDSOI transfer characteristics, d^2i_{ds}/dv_{gs}^2, as shown in Figure 4 [21, 22]. The determination of the dependence of the saturation current, I_{sat}, [12, 14], on the temperature is shown in Figure 5. I_{sat} is the maximum "ON" current determined when the PU and PD transistors work in the saturation region. For instance, I_{sat} is the current value defined when $v_{gs} = V_{DD}$ and $v_{ds} = V_{DD}$ for an NMOS transistor [12, 14]. Obviously, the second derivative method cannot be directly applied without digital preprocessing of the acquired measurement noisy data. Since the derivative amplifies the noise, this method [21, 22] becomes impractical and fails in identifying the exact threshold voltage. As shown in Figure 5, the temperature variation linearly affects I_{sat} and nonlinearly affects V_{th} [12, 14, 20, 21].

Therefore, a nonlinear interpolating model should be derived in order to capture these effects and incorporate them in the nominal power supply-aware model which is formed by the I-Q model for the driver's last stage and the SDFs timing functions capturing the predriver's stage nonlinear dynamics. Consequently, the Lagrange interpolating polynomials is used to accurately approximate the nonlinear dynamic effects of the temperature variation on the predriver's SDFs (7) and the driver's last stage PU and PD I-V and C-V functions (8).

$$w_j\left(t, T\right) = \sum_{i=0}^{p} B_{i,j}\left(T\right) \cdot w_j\left(t, T_i\right)$$

$$B_{i,j}\left(T\right) = \prod_{k=0, i\neq k}^{p} \frac{\left(T - T_k\right)}{\left(T_i - T_k\right)}; \tag{7}$$

$$j = L, H$$

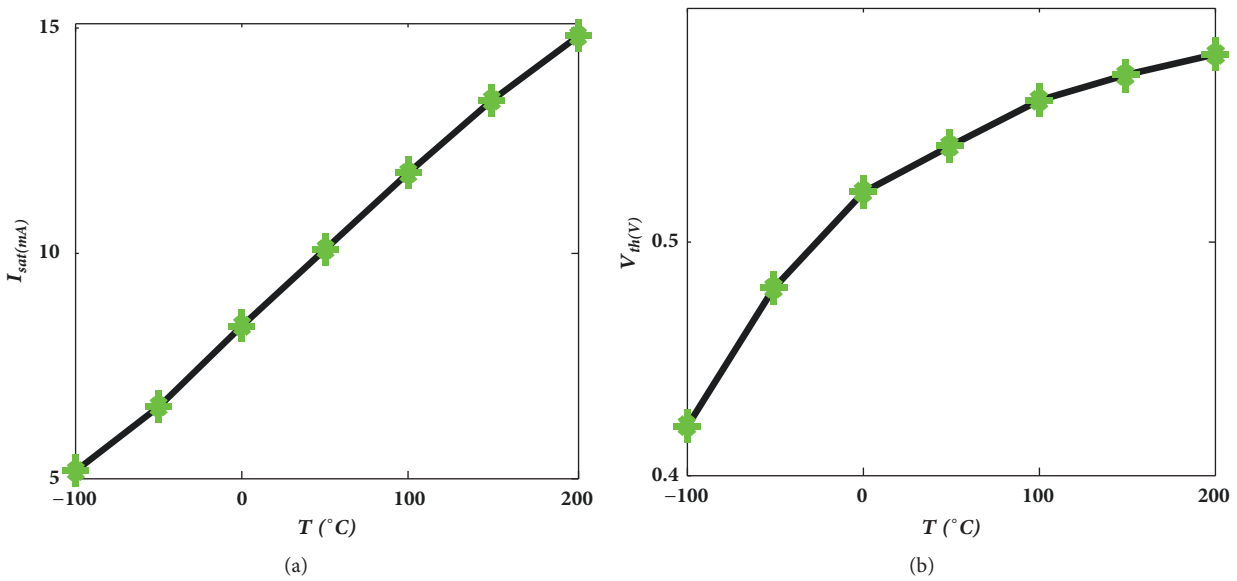

Figure 5: Variation of the saturation current (a) and threshold voltage (b) of the PD device versus temperature.

where $w_j(t, T_i)$ stands for the extracted SDFs for different values of the temperature T_i. $B_{i,j}(T)$ is the p^{th} order interpolating Lagrange polynomial.

$$f_j(t,T) = \sum_{i=0}^{g} R_{i,j}(T) \cdot f_j(t,T_i)$$

$$R_{i,j}(T) = \prod_{k=0,i\neq k}^{g} \frac{(T-T_k)}{(T_i-T_k)}; \quad (8)$$

$$j = L, H$$

where $f_j(t, T_i)$ represents the extracted $G_j(\cdot)$ and $C_j(\cdot)$ nonlinear functions of the driver's last stage for different values of the temperature T_i. $R_{i,j}(T)$ is the g^{th} Lagrange polynomial that captures the dependence of the driver's last stage nominal output admittance on the temperature variation.

3. Validation of Model's Extraction and Implementation

3.1. Model Extraction Results. Several Lagrange polynomial orders have been tried to interpolate the proposed nominal IBIS-like model in order to capture the power supply and temperature variations. Considering the analysis and the observation of i_{ds} vs v_{gs} nonlinearity of the previous sections and, taking into account the computational running complexity of the generated behavioral model, the third-order (e.g., $m = 3$) Lagrange polynomial is selected for the power supply-aware model. The prediction accuracy of the interpolated SISO I-V characteristic by a cubic Lagrange polynomial to predict the DISO I-V characteristic (i.e., gate modulation effect) at the nominal temperature is compared with the dc simulation of the driver's TL model as shown in Figure 6. Moreover, the interpolation accuracy of the third-order Lagrange polynomial of the extracted $C_H(\cdot)$ function is shown in Figure 7. The PU nonlinear capacitance, $C_H(\cdot)$, seen between the power-output port, is extracted from bias-dependent scattering S-parameters [20], when the excitation signal is now connected between the power supply and output nodes [4–6]. The good prediction of the interpolated single-valued SISO I-V and C-V relationships confirms that the cubic Lagrange polynomial is an adequate choice for including the effect of the PU and PD transistor's turn-on at the subthreshold voltage region. Similarly, the effects of the temperature variation on the behavioral model functions, $w_j(\cdot)$ and $f_j(\cdot)$, are properly incorporated through the cubic Lagrange polynomial.

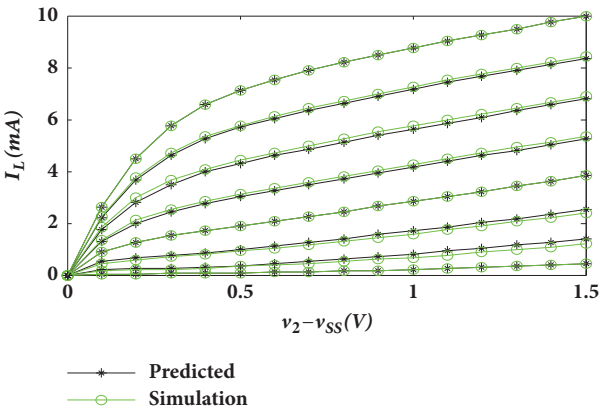

Figure 6: Comparison between the I-V characteristic for the PD device, I_L, when $v_g - v_{ss}$ varies between 0.5 V and 1.2 V with 0.1 V step at 27°C.

Although the second-order Lagrange interpolating polynomial is more practical to use with the IBIS specification that already provides the (min, typ, max) data for capturing

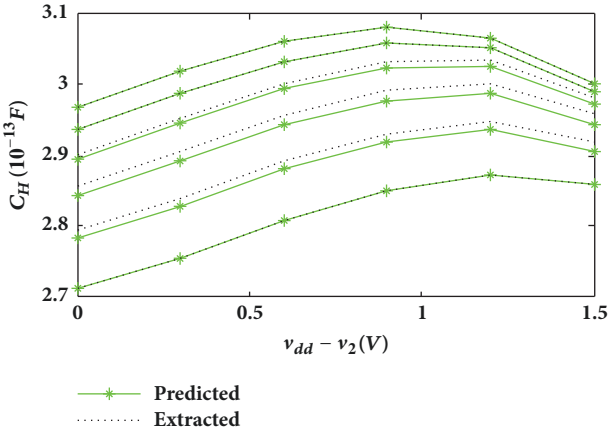

Figure 7: Comparison between the C-V characteristic for the PU device, C_H, when $v_{dd}(t) - v_2(t)$ varies between 0 V and 1.5 V with 0.3 V step at 27°C.

the effect of continuous and dynamic variations of the temperature and supply voltage variables, these I-V and voltage time (V-t) data which are sampled at three temperature and supply voltage, V_{DD}, points have to cover the wide working range of the power supply voltage and temperature variables in order to avoid a large polynomial extrapolation error [14–16]. Moreover, it was tested that the fitting accuracy of the cubic interpolating Lagrange polynomial is better than the quadratic case in approximating the nonlinear relationship, V_{th} versus T, therefore capturing the temperature variation on the predriver's stage (i.e., $p = 3$) and driver's last stage (i.e., $g = 3$). For these reasons, additional V-t curves for V_{DD} and T values have to be added to the IBIS specifications and library in order to enable higher-order Lagrange polynomial interpolation for the accurate power supply- and temperature-aware model prediction [7, 15, 16].

3.2. Model Implementation and Validation. Besides accuracy, the model's computational cost is an important factor to consider during the numerical model's implementation step because real applications such as bus simulation require the transient simulation of many I/O devices [3–9]. The SISO I-V and C-V LUTs, seen between the power-output port and ground-output port of the driver's last stage, respectively, are required for the accurate prediction of $v_{dd}(t)$ bouncing. The extracted C-V functions, $C_H(\cdot)$ and $C_L(\cdot)$, are integrated to retrieve the charge-voltage (Q-V) for more computationally efficient I-Q model implementation [10]. The polynomial implementation based on the Lagrange representation has a high number of floating points operation (FLOPs) (i.e., $O(n^2)$, $n = 2$) which are required for additions and multiplications. Therefore, it would be better to construct and store the tabular function as Newton or Neville's formula that speeds up the evaluation of the unique interpolating polynomial with $O(n)$ FLOPs. Moreover, the addition of another sampled I-V, Q-V, or SDFs for higher-order interpolation with respect to temperature and power supply variations, in the Newton construction, avoids the recalculation of the previous coefficients of the polynomials.

Table 1: Maximum timing error between the predicted signals of Figures 10 and 11.

	$i_{dd}(t)$	$v_{dd}(t)$	$v_{far-end}(t)$	
Temperature	60°C	60°C	−20°C	120°C
MTE_r (ps)	35	43	60	52
MTE_f (ps)	15	27	40	40

The implemented model architecture, using Newton-Neville's formula that captures the effects of power supply bouncing and temperature variation, is shown in Figure 8. The validation circuit, shown in Figure 9, describes three drivers which are simultaneously switching. The SSO buffers lead to the fluctuation of the on-chip power supply due to the package parasitic inductance $L_p = 1.5\,nH$ and resistance $R_p = 50\,\text{m}\Omega$.

The single driver is formed by four cascaded inverter stages with increasing driving capability designed based on CMOS FDSOI 28 nm technology from STMicroelectronics. Each output buffer drives a transmission line ($Z_0 = 50\,\Omega$, $T_d = 0.5\,ns$) loaded by a parallel circuit composed of $R_L = 80\,\Omega$ and $C_L = 2\,pF$. The required data used for the extraction of the model's functions was recorded from the driver's circuit simulations described by the TL model BSIMSOI in Cadence. The model was generated and implemented in the advanced design system (ADS) from Keysight Technologies. The normalized mean square error (NMSE) is used to quantify the prediction accuracy between the TL and proposed model's signals:

$$NMSE_y = 10\log_{10}\left[\frac{\sum_{k=1}^{K}\left(y(k)-\widehat{y}(k)\right)^2}{\sum_{k=1}^{K}\left(y(k)\right)^2}\right] \quad (9)$$

where signals $y(k)$ and $\widehat{y}(k)$ correspond to the voltage or current waveforms predicted by the TL model and the proposed power- and temperature-aware behavioral model, respectively. The good agreement between the predicted $v_{far-end}(t)$ and power supply signals, $v_{dd}(t)$ and $i_{dd}(t)$, of the TL and the proposed interpolated models at the second driver, while all the output buffers are driven by the bit pattern "01100101010" at 800 Mbps speed and equal rise/fall time of 0.1 ns, is shown in Figures 10 and 11, respectively.

The maximum timing error of the rising, MTE_r, (e.g., L to H) and falling, MTE_f, (e.g., H to L) transitions are presented in Table 1 in order to quantify the accuracy of the output switching transitions at the RC parallel circuit which emulates the receiver's impedance of the high-speed digital communication I/O link. For instance, the MTE of $v_{far-end}(t)$ waveform at the rising and down transitions are about 60 ps and 40 ps, respectively, at the temperature values $T = -20$°C and $T = 120$°C.

An improved modelling accuracy can be achieved by using higher interpolating points with respect to the power supply, v_{dd}, and temperature T which lead to a longer identification (e.g., characterization) time along with more data for storing the interpolating SDFs and I-Q functions in the EDA tools which consequently affects the model's computational cost. While the signal prediction of the proposed model in

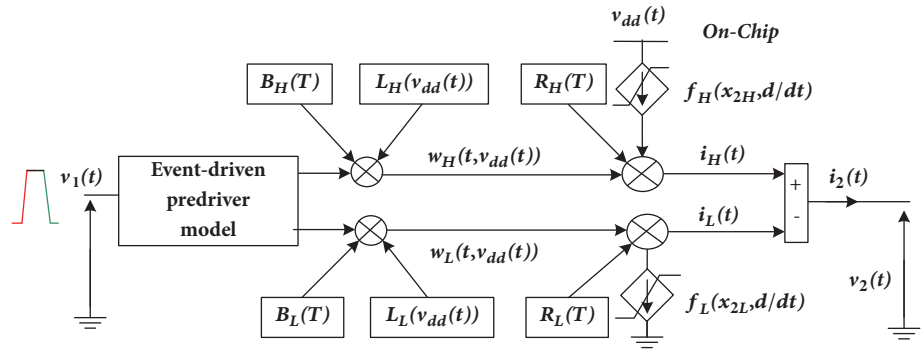

Figure 8: Implementation of the interpolated model for power supply and temperature variations.

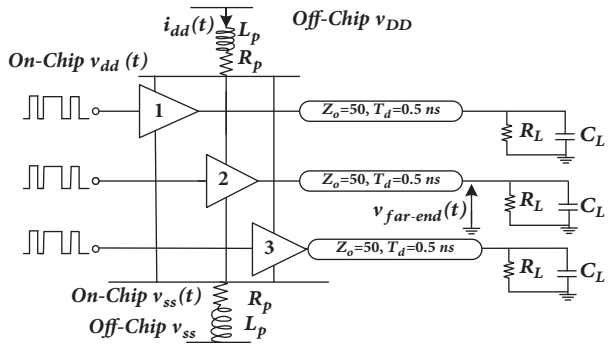

Figure 9: Validation circuit with three simultaneously switching drivers.

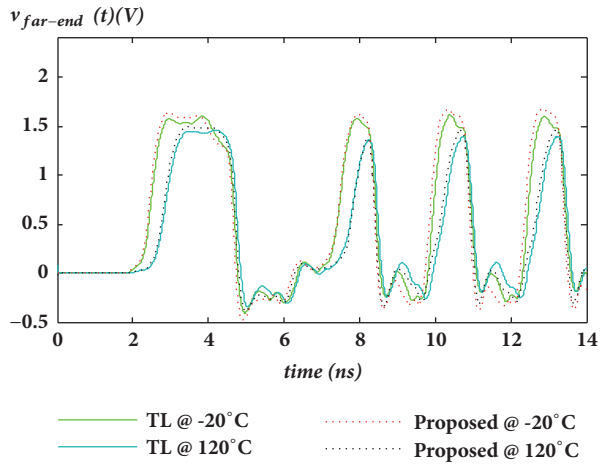

Figure 10: Comparison between the predicted $v_{far-end}(t)$ between TL and proposed model at -20°C and 120°C.

Figures 10 and 11 is not as accurate as the nominal two-port model which is used only for the signal integrity assessment, the selected interpolating (i.e., sampling) points (e.g., $m = g = p = 3$) are minimized in order to alleviate the running computational complexity without sacrificing the accuracy of the extended IBIS-like model in predicting the SPI propagating signals at the I/O and power terminals at different temperature values. In fact, the extension of the

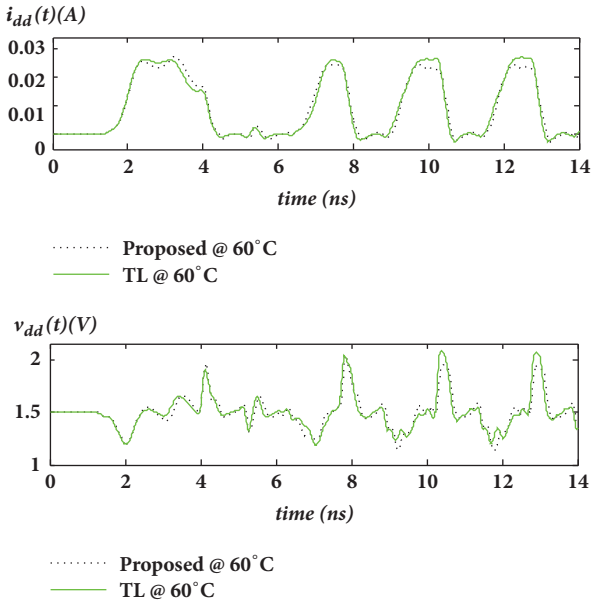

Figure 11: Comparison between the predicted power supply voltage and current fluctuation at 60°C of the TL and the proposed model.

two-port IBIS-like model to capture the power supply and the temperature effects is optimized in order to balance the tradeoff between the model's accuracy along with the identification time and running complexities.

Furthermore, the eye diagram prediction of the $v_{far-end}(t)$ signal after the transient simulation of the setup described in Figure 9, where the three drivers described by the TL and the proposed IBIS-like driver's models simultaneously transmit a random 1024-bit stream at the temperature -20°C, 60°C, and 120°C, is depicted in Figure 12 where the eye opening parameters, the width, ΔW, and the height, ΔH, are also defined. As seen, the proposed power supply- and temperature-aware model accurately predicts the input-output distortion effects under SSO and temperature variation when compared with the TL response. The achieved accuracy and model simulation efficiency using an i7 PC at 2.4 GHz, with 8 GB of RAM, are compared in Table 2. The computation time is estimated as the mean of the total stopwatch times of the transient simulator.

Table 2: Performance of the transient simulation for eye diagram prediction of the proposed IBIS-like and TL models.

Model	$NMSE_{i_{dd}}$	$NMSE_{v_{dd}}$	$NMSE_{v_{far}}$	Time (s)
TL	-	-	-	155.98
Proposed Model	-33.4 dB	-23.6 dB	-24.45 dB	24.76

Table 3: Comparison of the eye width, ΔW, and height, ΔH, parameters of the TL and the proposed IBIS-like behavioral model.

	$T = -20^{\circ}C$		$T = 60^{\circ}C$		$T = 120^{\circ}C$	
	ΔH (V)	ΔW (ns)	ΔH (V)	ΔW (ns)	ΔH (V)	ΔW (ns)
TL	0.75	0.77	1.07	0.80	1.18	0.93
Proposed Model	0.69	0.72	0.96	0.82	1.11	0.90

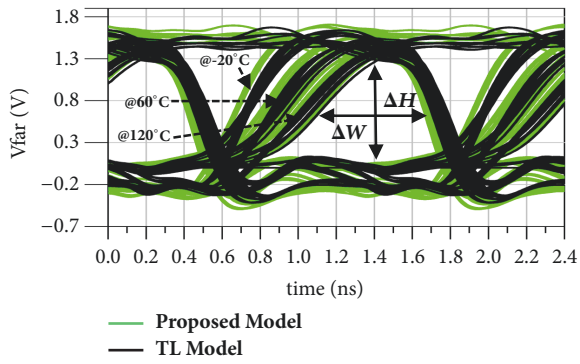

Figure 12: Eye diagram prediction of the TL and the proposed power supply- and temperature-aware model at different temperature values -20°C, 60°C, and 120°C.

The prediction accuracy of the eye diagram is quantified by comparing the eye opening parameters for different temperatures as presented in Table 3.

The relative error between the TL and the proposed behavioral model of the eye width, $(\Delta W^{TL} - \Delta W^{Model})/\Delta W^{TL}$, is about 6.49%, 2.44%, and 3.23% while the relative error of eye height, $(\Delta H^{TL} - \Delta H^{Model})/\Delta H^{TL}$, is about 8.00%, 10.28%, and 5.93% at $T = -20^{\circ}C$, $T = 60^{\circ}C$, and $T = 120^{\circ}C$, respectively. Accordingly, the proposed behavioral model is accurate in predicting the eye opening parameters with an error less than 6.5% in the eye width and an error less than 10.28% in the eye height at different temperature values. The prediction error can be reduced by selecting more sampling points while generating the power- and temperature-aware models. Therefore, additional nonlinear I-Q functions and SDFs need to be stored in the EDA library and a higher polynomial order is required for performing the interpolation which will affect the simulation time.

4. Conclusions

This paper has presented the generation of a power supply-aware I/O buffers model accounting for temperature variation in order to enhance the SPI simulation capabilities of the nonlinear equivalent circuit IBIS-like model. The extended model accurately predicts the coupling of the SSN in data signals while considering temperature variation. The model's numerical implementation (i.e., FLOPs) was optimized by means of Newton construction of the interpolated third-order polynomials of the LUTs I-V, Q-V, and SDFs functions implementation. The accuracy and the computational efficiency of the proposed solution were verified and quantified and a significant speed-up of 6× of the simulation time is achieved in predicting the eye diagram of the high-speed communication I/O link.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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