Research Article

Neurospace Mapping Modeling for Packaged Transistors

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This paper presents a novel Neurospace Mapping (Neuro-SM) method for packaged transistor modeling. A new structure consisting of the input package module, the nonlinear module, the output package module, and the S-Matrix calculation module is proposed for the first time. The proposed method can develop the model only using the terminal signals, instead of the internal and physical structure information of the transistors. An advanced training method utilizing the different parameters to adjust the different characteristics of the packaged transistors is developed to make the proposed model match the device data efficiently and accurately. Measured data of radio frequency (RF) power laterally diffused metal-oxide semiconductor (LDMOS) transistor are used to verify the capability of the proposed Neuro-SM method. The results demonstrate that the novel Neuro-SM model is more accurate and efficient than existing device models.

1. Introduction

With the development of electronic technology, the accurate computer-aided design (CAD) models of transistors play a decisive role in the circuit/system design with high performance and reliability [1, 2]. The transistor in the circuit system contains not only the active cells, but also the passive devices such as the encapsulated package circuit. As the operating frequency increases, the presence of package components cannot be neglected due to the fact that the package parasitics influence the transistor performance [3, 4]. In order to predict the electrical performance of the packaged transistor, the CAD model must accurately reflect the characteristics of the active cells and the packaged circuit.

Package modeling for active/passive devices have been a field of strong interest in recent years [5, 6]. The equivalent-circuit-based model of metal-ceramic packages which was described in terms of inductances, resistances, and capacitances was used in radio frequency (RF) and microwave transistors [6, 7]. When the equivalent-circuit parameters are simultaneously optimized by the device data, the exact relationship between the voltage and current of packaged transistor can be obtained. As the device structure becomes complicated, it is inaccurate and time consuming to construct

packaged transistor model in equivalent-circuit modeling manner due to slow trial-and-error processes. Electromagnetic (EM) modeling approaches become essential to realize design accuracy [8, 9]. A modeling method based on EM theory was presented in [10] to predict the EM feature of the three-dimensional construction of a high-power RF transistor with internal matching networks. Tedious calculation of EM simulation is prohibitively expensive, especially when a significant number of the geometric and material parameters have to be adjusted repeatedly [11–13].

Recently, Neurospace Mapping (Neuro-SM) techniques have been recognized as useful alternatives to conventional approaches in microwave modeling [14–16]. The Neuro-SM model can not only accurately represent the input and output relationship of the device/circuit, but also calculate quickly reducing the circuit/system simulation cycle [17]. Circuit-based Neuro-SM was proposed firstly in 2003 and then received wide attention from academia and industry [18]. An evolutionary Neuro-SM modeling technique with high computational efficiency was proposed in literature [19] which considered not only the voltage mappings but also the current mappings. Reference [20] used a dynamic neural network as the mapping network, and two mapping networks with analytical equations were added on the existing model

FIGURE 1: Block diagram of the proposed packaged transistor model.

in [21]. These existing Neuro-SM methods mainly focus on modeling for the active cells of transistor. The problem of package modeling is not addressed in these existing works.

In this paper, we proposed a new modeling method for packaged transistor based on Neuro-SM. The proposed method roughly divides the packaged transistor into three parts: the input package circuit, the nonlinear circuit, and the output package circuit, and they are built, respectively. In addition, an advanced training method making the novel model match the device data effectively is developed, which can avoid the mutual interference of the optimized parameters for the different performance of model. To verify the availability of the proposed modeling approach, a practical example on modeling RF power LDMOS transistor is presented.

2. Proposed Neuro-SM Modeling for Packaged Transistors

2.1. Proposed Neuro-SM Model Structure. Packages of transistors typically contain a metal flange and a dielectric window frame. The transistor is bonded to the die-bond area inside the cavity of the window frame. Metal leads are provided at the input and output sides of the window frame to allow for connection to external circuitry. Based on the physical structure of packaged transistor, we propose to roughly divide the total structure into three parts: the input package circuit, the nonlinear circuit, and the output package circuit. The proposed Neuro-SM modeling method creates the CAD modules for the three parts, respectively, and an additional S -Matrix calculation module is required to associate the three CAD modules as a whole.

There are 4 modules in the novel Neuro-SM model of the packaged transistor: the input package module, the nonlinear module, the output package module, and the S -Matrix calculation module, as shown in Figure 1. The input/output package module represents the performance of the package circuits which consist of passive components

such as bond wires, MOS capacitors, integrated capacitor, and so on. Because the input/output package circuit consists of linear components, the unique input signal of the input/output package modules is the frequency, and the output signals are the real and imaginary parts of S_{11} , S_{12} , and S_{22} . The nonlinear module represents the characteristic of the multiple active cells in the packaged transistors. The nonlinear module is constructed by the existing Neuro-SM modeling method in literature [22]. Both DC characteristic and the S -parameter performance of packaged transistors are affected by the nonlinear module. For the nonlinear module, bias voltages and frequency are the input signals, and the real and imaginary parts of 4 S -parameters are the output signals. S -Matrix calculation module plays an important role in calculating the S -parameter matrixes of the input package module, nonlinear module, and the output package module. The output signals of the S -Matrix calculation module are the S -parameters of the modeled object.

Scattering-matrix analysis is applicable to any general microwave circuit configuration when all the circuit components are modeled in terms of their scattering parameters. The S -Matrix calculation module is constructed based on the literature [17]. S^i represents the S -parameters of the i th component. For the packaged transistor model we proposed, i equals 1, 2, and 3 representing the input package module, the nonlinear module, and the output package module, respectively.

$$S^i = \begin{pmatrix} S_{11}^i & S_{12}^i \\ S_{21}^i & S_{22}^i \end{pmatrix} \quad (1)$$

W called the connection-scattering matrix represents the relationship between the incident wave and reflected wave. The main diagonal elements in W are the negative of the reflection coefficients at the various component ports. The other (nondiagonal) elements of W are negative of the transmission coefficients between different ports of the individual

FIGURE 2: Block diagram of the proposed package module. (a) Block diagram of the proposed input package module. (b) Block diagram of the proposed output package module.

components. For the proposed model in Figure 1, W can be written as represented in

$$W = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -S_{11}^1 & -S_{12}^1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -S_{21}^1 & -S_{22}^1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -S_{11}^2 & -S_{12}^2 & 0 & 0 & 0 \\ 0 & 0 & 0 & -S_{21}^2 & -S_{22}^2 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -S_{11}^3 & -S_{12}^3 & 0 \\ 0 & 0 & 0 & 0 & 0 & -S_{21}^3 & -S_{22}^3 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}_{8 \times 8} \quad (2)$$

Setting $M = W^{-1}$, we can obtain the total S -parameters of the input package module, the nonlinear module, and the output package module, that is, the output of the S -matrix calculation as represented in

$$S = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} = \begin{pmatrix} M_{11} & M_{18} \\ M_{81} & M_{88} \end{pmatrix} \quad (3)$$

2.2. Proposed Package Module Structure. There are two reasons for employing package circuit for RF/microwave transistors. The first one is the environmental ruggedness and the mechanical strength which can protect the internal circuit of transistor. The second one is to ease external matching-circuit design and improve device performance by adding an internal matching circuit into the package circuit. To achieve high gain or efficiency, lots of active cells are added to the transistor, which result in more bond wires; MOS capacitors and integrated capacitor are used to make electrical connections. The complex structure of package circuit greatly increases the difficulty of modeling. The package modeling method we proposed can be applied to arbitrary packaging structures, because the advanced package module is achieved only using the terminal signals, instead of the internal and physical structure information of the package circuit.

The block diagram of the package module is shown in Figure 2. The frequency is the unique input signal of the

package module which is not excited by the bias voltage. The real and the imaginary parts of the S -parameters which are represented by prefix R and I , respectively, are the output signals of the package module. The subscripts i and o represent the input package and output package, respectively. In the package modules, the S_{21} is not selected as an output because the dual network has the relationship $S_{21} = S_{12}$, which can reduce the output dimension of the input/output module and simplify the model structure.

In the proposed package module, B is a free variable and θ is the phase of the S -parameter. The subscript indicates the port number of the input/output packaged circuit and the superscript i and o represent the input package and output package, respectively. The neural networks are used to represent the nonlinear relationship between the frequency and the 4 outputs of the neuronnet as represented in (4) and (5).

$$(B^i, \theta_{11}^i, \theta_{12}^i, \theta_{22}^i) = f_{ANN}(freq, \mathbf{w}_1) \quad (4)$$

and

$$(B^o, \theta_{11}^o, \theta_{12}^o, \theta_{22}^o) = h_{ANN}(freq, \mathbf{w}_2) \quad (5)$$

where f_{ANN} and h_{ANN} represent multilayer feedforward neural network and $\mathbf{w}_1$ and $\mathbf{w}_2$ are vectors containing all internal synaptic weights of the neural network f_{ANN} and h_{ANN} , respectively.

Let A represent the amplitude of the S -parameters of the package circuit. The subscripts indicate the port number of the package circuit. The proposed package module adopts a free variable B to calculate the amplitude of the S -parameters, which make sure that the value of A_{11} is between 0 and 1 whatever the value of B is. A_{11} is computed as represented in

$$A_{11} = \frac{1}{1 + e^{-B}} \quad (6)$$

In the proposed method, the package circuit is supposed to be lossless and satisfies that quadratic sum of Return Loss

model cannot meet the modeling requirements, the Neuro-SM model including the coarse model and mapping networks is used to best match the fine model by automatically mapping the nonlinear relationship between signals of the coarse model and the fine model. Compared with other modeling methods based on space mapping, the Neuro-SM model does not require complex parametric extraction to obtain the next iteration point, which greatly reduces the time required for model development. In the novel Neuro-SM model we proposed, the nonlinear module is constructed as the structure shown in Figure 3.

In the nonlinear module, when the coarse model operates with the signals $(v_{gc}, v_{dc}, freq)$ instead of the signals $(v_{gf}, v_{df}, freq)$, the output current i_{dc} and the S-parameters of coarse model can match that of fine model accurately. The neural network is used to describe the nonlinear relationship between the signals of the coarse model (v_{gc}, v_{dc}) and the signals of the fine model (v_{gf}, v_{df}) as represented in

where g_{ANN} represents a multilayer feedforward neural network and $\mathbf{w}_3$ is a vector containing all internal synaptic weights of the neural network g_{ANN} .

2.4. Proposed Training Method. Precise models rely on reasonable parameters except for the correct model structure. The most important step during neural network modeling is to find a suitable set of weights by the training process. Let the training error measure the learning performance of the proposed model. Let the test error measure the predictive ability of the proposed model. The training process is performed until both the training error calculated with the training data and the test error calculated with the test data

2.3. Nonlinear Module Structure. In order to perform the nonlinear characteristic of active cells in packaged transistor, Neuro-SM modeling method in literature [22] is used. Let the fictitious model that accurately matches the new measured/simulated data of transistors be called the fine model. Let the existing empirical/equivalent-circuit model be called the coarse model. When the accuracy of the coarse

TABLE 1: Training data and test data for DC and S-parameter modeling of LDMOS transistor.

		V_{gf} (V)	V_{df} (V)	$freq$ (GHz)
DC Simulation	Training Data	2.6:0.1:3.2	0:2:32	
	Test Data	2.6:0.1:3.2	1:2:31	
S-Parameter Simulation	Training Data	0:1:1	8:4:24	
		2.5:0.1:2.8	30	1.7:0.028:3.1
		0:0.2:2.2	28	
		2.3:0.1:2.8		
	Test Data	0:1:1	10:4:26	
		2.5:0.1:2.8		
		0.1:0.2:1.1		1.7:0.028:3.1
		1.5:0.2:2.1	28	
		2.45:0.1:2.75		

meet the accuracy requirements. The same error function of DC and S-parameters as represented in (9) and (10), respectively:

$$E_{DC}(\mathbf{w}) = \frac{1}{2} \sum_{n=1}^N \|I(V_{gf}^n, V_{df}^n, \mathbf{w}_3) - I_D^n\|^2 \quad (9)$$

$$E_S(\mathbf{w}) = \frac{1}{2} \sum_{n=1}^N \|S(V_{gf}^n, V_{df}^n, freq^n, \mathbf{w}_1, \mathbf{w}_2) - S_D^n\|^2 \quad (10)$$

where I_D and $I(\cdot)$ represent the DC responses of the packaged transistor data and the proposed model, respectively. S_D and $S(\cdot)$ represent the S-parameters of the packaged transistor data and the proposed model, respectively. The superscript n represents the training or test data index, and N represents the total number of the training or test data.

The optimized parameters in the proposed model consist of $\mathbf{w}_1$ in the input package module, $\mathbf{w}_2$ in the output package module, and $\mathbf{w}_3$ in the nonlinear module. The advantage of the proposed modeling approach is modular modeling, which make different parameters control different characteristics. However, the existing training methods optimize all parameters of neural networks at the same time, which cannot get appropriate parameters for the proposed model easily. In order to improve the optimizing efficiency of the proposed model, the proposed training method complete the construction and training of the packaged transistor model by using the following four steps.

Step 1. Send the bias voltage of the fine model to the mapping network in the nonlinear module. Initialize the weight $\mathbf{w}_3$ making (v_{gc}, v_{dc}) equal to (v_{gf}, v_{df}) , which ensure that the performance of the Neuro-SM model will not get worse than the coarse model.

Step 2. Adjust the weight $\mathbf{w}_3$ of the mapping network in nonlinear model by solving (9). Obtain the bias voltage of coarse model v_{gc} and v_{dc} by solving (8), which make the Neuro-SM model match the fine model in the DC simulation.

Step 3. Adjust the weights $\mathbf{w}_1$ and $\mathbf{w}_2$ of the neural networks in package modules by solving (10). Obtain the appropriate

parameters $B, \theta_{11}, \theta_{12}$, and θ_{22} by solving (4) and (5), which make the proposed Neuro-SM model match the fine model in the S-parameter simulation.

Step 4. Train the proposed Neuro-SM model with DC and S-parameter data simultaneously. Fine tune the weights $\mathbf{w}_1, \mathbf{w}_2$, and $\mathbf{w}_3$ improving the performance of the proposed model further.

The proposed training method enhances the advantage of the existing training method by adjusting the parameters in steps. The proposed method controls the DC/AC performance of the Neuro-SM model with different weight parameters, which reduce the mutual interference of the optimized parameters for the different performance of model and avoid changing the optimized parameters repeatedly.

3. Examples

RF power LDMOS transistor is the technology of choice, due to its low power consumption, high mechanical hardness, and the inherent economic advantages that silicon wafer manufacturing offers. To verify the accuracy and feasibility of the proposed Neuro-SM modeling method, the I-V and S-parameter characteristics of packaged LDMOS transistor are modeled [23]. Measurement data of LDMOS transistor with packages are obtained as the training data and test data. The range of the training data and test data used in this example is showed in Table 1. The proposed Neuro-SM model learns the training data by adjusting automatically the weight of the neural networks. Test data which are different with the training data are used to validate the accuracy of the constructed model.

In this example, Angelov model is used as the existing coarse model. At present, Angelov model which can match many types of transistors is considered to be the great nonlinear model. Choosing Angelov model as the coarse model improve the general applicability of the new modeling method. The mismatch between the coarse model and the measured data of the LDMOS transistor cannot be ignored even by optimizing the parameters in the coarse model as much as possible. Then, the input/output package modules

TABLE 2: Accuracy comparison of coarse model and proposed models for DC and S-parameter simulation.

Parameter	Coarse Model Test Error (%)	Proposed Model Test Error (%)
I_{ds}	1.01	0.85
$real(S_{11})$	21.61	2.18
$imag(S_{11})$	25.87	3.12
$real(S_{12})$	23.81	3.97
$imag(S_{12})$	36.68	3.79
$real(S_{21})$	10.29	2.02
$imag(S_{21})$	4.99	2.07
$real(S_{22})$	24.18	2.01
$imag(S_{22})$	40.40	2.19

FIGURE 4: I-V comparison between measured data, coarse model, and proposed model for the LDMOS example.

and mapping network are applied. The new model is trained as the four steps introduced in Section 2. The proposed model adjusts the weights of neural networks with the training data until the error between the fine model and the proposed Neuro-SM model operating with test data meet the design requirements. Table 2 gives the test error of the coarse model and the proposed model. This result demonstrates that the novel Neuro-SM method improves the current capabilities of the coarse model.

In order to further show the detail results, the I-V comparison of the coarse model and the proposed model is shown in Figure 4. Due to the low nonlinearity of DC characteristic, both the coarse model and the proposed model can match the measured data well. However, the accuracy of the proposed model is much higher than the coarse model in S-parameter simulation as shown in Figure 5. These models work at bias voltage ($v_g = 2.75V$, $v_d = 28V$) which is

never used in training data. The magnitude and phase of S-parameters from the proposed Neuro-SM model vary versus frequency in the exactly same way as that from the measure data. Because the 4 S-parameters of the coarse model are controlled by the same set of parameters, it only provides a roughly approximation to the fine model. In the proposed model, the package module can respond to the frequency and the active module can respond to the bias voltages. The parameters in the proposed modules are independent and control different performance of the packaged transistor. Therefore, the proposed model contains more free variables and matches 4 S-parameters of the fine model well simultaneously.

After being trained with DC data and S-parameter data, both the coarse model and the proposed model are operated in harmonic balance (HB) simulation to further verify the effectiveness of the advanced modeling methodology. Those models work at bias voltage ($v_g = 2.75V$, $v_d = 28V$), fundamental frequency ($freq = 1.805GHz$), source impedance ($Z_S = 1.535 - j4.232\Omega$), and load impedance ($Z_L = 1.403 - j3.748\Omega$). The range of the input power P_{in} is from 4.5 to 18.5dBm and the step of that is 2dBm, which allows the LDMOS transistor in this example to work in a linear region. The comparison results of the gain and the power added efficiency (PAE) between the coarse model and the proposed model are shown in Figure 6, demonstrating that the HB response of the proposed Neuro-SM model is much closer to the measured data than that of the coarse model. This result provides a good foundation for the large signals modeling in the future work.

4. Conclusions

A new Neuro-SM modeling approach has been proposed for packaged transistors. The novel model structure can accurately reflect the characteristics of both the active cells and the packaged circuit. This allows existing models to exceed their current capabilities. The advanced training method avoids repetitive adjustment of the optimization parameters improving the modeling efficiency. Good results are verified by the practical example. In the future, we can extend the proposed modeling method to further improve the larger-signal characteristic of the package transistors. Another potential future direction is to apply the proposed method in this work to the trapping behaviors of the gallium nitride transistors, meeting the needs of contemporary technology.

Data Availability

The data used to support the findings of this study comes from the author herself and may not be available for publication for the time being.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

FIGURE 5: Comparison of S-parameters between measured data, coarse model, and proposed model for the LDMOS transistor at the typical work bias point ($v_g = 2.75V$, $v_d = 28V$): (a) magnitude of S_{11} , (b) phase of S_{11} , (c) magnitude of S_{12} , (d) phase of S_{12} , (e) magnitude of S_{21} , (f) phase of S_{21} , (g) magnitude of S_{22} , and (h) phase of S_{22} .

FIGURE 6: Plot of the gain and PAE between measured data, coarse model, and proposed model for the LDMOS transistor.

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