Research Article

Emulator Based on Switching Functions for a Dual Interleaved Buck-Boost Converter

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Under the unavailability of some components of a complex system, the Hardware In the Loop (HIL) tool allows the emulation of other subsystems. When these devices are not available, a customized emulator can be developed based on the Piecewise Linear Model (PWLM) and a numerical method for solving the differential equations system. However, these implementations require the use of a Field Programmable Gate Array (FPGA) with extensive hardware resources. In this article we propose the use of switching functions for the modeling of power converters of a Hybrid Power System (HPS), allowing the reduction of hardware resources of the FPGA, and the number of steps per switching cycle is increased. The results are compared with SABER simulations and a PWLM evaluated with the Euler method.

1. Introduction

Frequently during the development of a complex system there are multiple subsystems under study; this represents a challenge for the rapid evolution of large projects. With the help of an emulator, multiple components can be developed quickly and efficiently; these tools are called Rapid Control Prototyping (RCP) or HIL. The HIL simulation is a form of simulation of real time; its initial use was in flight simulators and in missile guides, and nowadays its use has been extended to power electronics [1]. HILs are based on two technologies: microprocessors and FPGA. The disadvantage of the microprocessor-based emulators is that sequential logic would require clocks of the order of 10^{12} Hz to match the FPGA concurrence with clocks of the order of 10^6 Hz that would perform the same number of operations [2]. The applications in power electronics are the development of the train power system [3], ships [4], electric vehicles [5, 6], and microgrids [7–9], achieving in the best of cases a step size of the order of 10 ns, if the numerical representation is sufficiently accurate to reduce the error by truncation.

It is observed that the development of a HIL requires the mathematical model that describes the behaviour of the system; that in the case of power converters refers to

the equations that solve the electrical network. The hardware resources of the FPGA depend on the model to be implemented, the synthesis procedure, and the format of the arithmetic: in Fixed Point (FXP) or Floating Point (FP). In [10] to model an NPC converter, the network equations were described with the Modified and Augmented Node Analysis (MANA), obtaining the state equations. In [11] to model a three-phase inverter, the network equations were described under the Associated Discrete Circuit (ADC). In [12] the average value method was used to calculate the output value of a three-phase interleaved converter. In [3, 13–19], equations are used in the state space to describe the behaviour of different topologies of power converters. However, in order to be implemented, an FPGA with wide range of resources is required; around 65000 Look Up Tables (LUT) to obtain a step size of the order of 5 ns, in some cases multiplex arithmetic operations can reduce the size between 15000 and 6000 LUT, with a cost of increasing the step size to 250 ns [18]

In this article, the model based on Switching Functions (SF) for a Dual Interleaved Buck-Boost Converter (DIBBC) with interphase transformer (IPT) was developed, and the hardware implementation was made for an FPGA of limited resources. Likewise SABER simulations results were compared with a PWLM and this proposal. It was observed

FIGURE 1: Scheme of a Dual Interleaved Buck-Boost Converter (DIBBC).

that the difference between models is minimal; however, in the hardware implementation the difference is drastic. In addition, it was noted that the step size is only restricted to the core speed of the FPGA.

2. Switching Functions Model for DIBBC

2.1. The DIBBC. Figure 1 shows the diagram of a DIBBC composed of a DC voltage source, v_s , a switch bridge Q_1 , Q_2 , D_1 , D_2 , an (IPT) that includes L_1 and L_2 where $L_1 = L_2$, a common inductor L_{COM} , an output capacitor C , and a load R [20].

2.2. Operation Principle. The circuit operates under the state of transistors Q_1 and Q_2 , presenting two possible permanent state operation regions: $D < 0.5$ and $D > 0.5$; the main waveforms are depicted in Figure 2, in (a) - (k) corresponding to $D < 0.5$ and in (l) - (v) to $D > 0.5$. In (a) and (l) the signals of the states of the transistors Q_1 and Q_2 and v_{G1} and v_{G2} are observed for the fixed frequency ($1/T$) and a phase shifted between them of $T/2$ and a balanced duty cycle, D . (b) and (m) show the voltages in the nodes v_{AG} and v_{BG} . In (c) and (n) is the differential voltage $v_{AB} = v_{AG} - v_{BG}$. v_{AB} produces the current in the differential inductor $i_{L_{DIFF}}$ or IPT (d) and (o). (e) and (p) correspond to the voltage in the common inductor $v_{L_{COM}}$. The currents in the common inductor $i_{L_{COM}}$ are shown in (f) and (q), the currents in L_1 and L_2 are (g) and (h), and the currents in diodes i_{D1} and i_{D2} are shown in (h) and (s). The currents of Q_1 and Q_2 are shown in (i) and (v). The currents i_D in (j) and (u) are the sum of the currents in diodes D_1 and D_2 , and the current in the capacitor in (k) and (v).

Figure 3 shows the nine possible configurations of the DIBBC. The configurations from I to IV, Figures 3(a)–3(d), correspond to Continuous Current Mode (CCM), the other

five configurations are presented in the DCM, and the Discontinuous Current Mode (DCM) configurations V to IX are shown in Figures 3(e)–3(i); the DCM occurs when $i_{L1} = 0$ or $i_{L2} = 0$; under these conditions $i_{D1} = 0$ or $i_{D2} = 0$.

2.3. Switching Functions Model for a DIBBC. In each configuration of the circuit, the voltages of the nodes v_{AB} and v_{BG} , which depend only on v_s and v_o , can be established by the product of

$$\mathbf{v}_H = M_V \mathbf{v}_S \quad (1)$$

The vectors $\mathbf{v}_H$ are the voltages in the v_{AG} and v_{BG} nodes: $[v_{AG} \ v_{BG}]^T$, and the vector $\mathbf{v}_S$ is the supply voltage v_s and the capacitor voltage v_o : $[v_s \ v_o]^T$. M_V is a transformation matrix for each configuration that is called Voltage Switching Matrix. For the currents of transistors Q_1 and Q_2 there is a current vector $\mathbf{i}_Q$: $[i_{Q1} \ i_{Q2}]^T$, and for the currents of the diodes, $\mathbf{i}_D$ is $[i_{D1} \ i_{D2}]^T$. The current vector of the inductors $\mathbf{i}_L$ is $[i_{L1} \ i_{L2}]^T$; after $\mathbf{i}_L$, $\mathbf{i}_Q$, and $\mathbf{i}_D$ it can be obtained through the Current Switching Matrices M_{IQ} and M_{ID} shown in (2) and (3), respectively. Equation (1) is called voltage switching function (F_{SWV}) and (3) is called current switching function (F_{SWI}):

$$\mathbf{i}_Q = M_{IQ} \mathbf{i}_L \quad (2)$$

$$\mathbf{i}_D = M_{ID} \mathbf{i}_L \quad (3)$$

Table 1 shows the M_V and M_{ID} matrices for each configuration of the circuit; it indicates that the conditions for each configuration are presented and shade the configurations of the CCM. M_Q is excluded because at the moment it is not of interest for this work.

The current in L_{COM} can be divided into two when applying the superposition principle: the current that produces the

FIGURE 2: Steady-state waveforms of the DIBBC.

FIGURE 3: DIBBC configurations.

voltage in node A: $v_{L_{COMA}}$ and the current that produces the voltage in node B: $v_{L_{COMB}}$. The voltages in CCM for L_{COMA} , L_{COMB} , L_1 , and L_2 , are given by (4), (5), (6), and (7), respectively, and are obtained from the node analysis between A, B, COM, and GND of the circuit of Figure 1, for which $L_1 = L_2$ must be considered.

$$v_{L_{COMA}} = \frac{1}{2} v_{AG} \quad (4)$$

$$v_{L_{COMA}} = \frac{1}{2} v_{BG} \quad (5)$$

$$v_{L_1} = \frac{1}{2} (v_{AG} - v_{BG}) \quad (6)$$

$$v_{L_2} = \frac{1}{2} (v_{BG} - v_{AG}) \quad (7)$$

In DCM the voltages in L_{COMA} , L_{COMB} , L_1 , and L_2 are given by (8), (9), (10), and (11), respectively:

$$v_{L_{COMA}} = \frac{L_{COM}}{L + L_{COM}} v_{AG} \quad (8)$$

$$v_{L_{COMB}} = \frac{L_{COM}}{L + L_{COM}} v_{BG} \quad (9)$$

$$v_{L_1} = \frac{L}{L + L_{COM}} (v_{AG} - v_{BG}) \quad (10)$$

$$v_{L_2} = \frac{L}{L + L_{COM}} (v_{BG} - v_{AG}) \quad (11)$$

Equations (4) to (11) are the interactions in the voltage in the inductor network between nodes A, B, COM, and GND, and they are called XFRM_v. The network of inductors is formed by an interphase transformer (IPT) with the branches L_1 and

TABLE 1: Voltage switching function in A and B nodes and current switching function in diodes 1 and 2.

Configuration	Q_2	Q_1	v_{AG}	v_{BG}	M_V	i_{Q1}	i_{Q2}	i_{D1}	i_{D2}	M_{ID}
I	0	1	v_S	$-v_O$	$\begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$	i_{L1}	0	0	i_{L2}	$\begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}$
II	1	0	$-v_O$	v_S	$\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$	0	i_{L2}	i_{L1}	0	$\begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}$
III	0	0	$-v_O$	$-v_O$	$\begin{bmatrix} 0 & -1 \\ 0 & -1 \end{bmatrix}$	0	0	i_{L1}	i_{L2}	$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$
IV	1	1	v_S	v_S	$\begin{bmatrix} 1 & 0 \\ 1 & 0 \end{bmatrix}$	i_{L1}	i_{L2}	0	0	$\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$
V	0	1	v_S	0	$\begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}$	i_{L1}	0	0	0	$\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$
VI	1	0	0	v_S	$\begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix}$	0	i_{L2}	0	0	$\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$
VII	0	0	$-v_O$	0	$\begin{bmatrix} 0 & -1 \\ 0 & 0 \end{bmatrix}$	0	0	i_{L1}	0	$\begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}$
VIII	0	0	0	$-v_O$	$\begin{bmatrix} 0 & 0 \\ 0 & -1 \end{bmatrix}$	0	0	0	i_{L2}	$\begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix}$
IX	0	0	0	0	$\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$	0	0	0	0	$\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}$

L_2 and a common inductor, L_{COM} , the current proper to the IPT i_{LS} is obtained by means of (12) where $\mathbf{v}_L$ is the vector $[v_{L1} \ v_{L2}]^T$ and L^{-1} is the inverse matrix of the inductances of the transformer and i_{LS} is the vector $[i_{LS1} \ i_{LS2}]^T$.

$$\mathbf{i}_{LS} = L^{-1} \int \mathbf{v}_L dt \quad (12)$$

$i_{L_{COMA}}$ and $i_{L_{COMB}}$ are given by (13) and (14), respectively,

$$i_{L_{COMA}} = \frac{1}{L_{COM}} \int v_{L_{COMA}} dt \quad (13)$$

$$i_{L_{COMB}} = \frac{1}{L_{COM}} \int v_{L_{COMB}} dt \quad (14)$$

The currents i_{L1} and i_{L2} are given in (15) and (16), respectively. This set of equations are the interaction of the currents in the inductor network and are called XFRM_i:

$$i_{L1} = i_{LS1} + i_{L_{COMA}} \quad (15)$$

$$i_{L2} = i_{LS2} + i_{L_{COMB}} \quad (16)$$

In the DCM, L_1 and L_2 stop behaving like a transformer and become an inductor when leaving one of its branches at high impedance, so we can do $v_{L1} = v_{L2} = 0$. Observing the sets of (4) and (8), (5) and (9), (6) and (10), and (7) and (10), we have the common factors v_{AG} , v_{BG} , $v_{AG} - v_{BG}$, and $v_{BG} - v_{AG}$, respectively, and we can summarize (4) to (11) in Table 2, where we have the common factor for each inductor voltage and G_{XFRMV} gain factor.

The balance of the current i_D is described by (17) and (18); (17) corresponds to the current coming from diodes D_1 and D_2 and (18) corresponds to the current injected into the RC output network.

$$i_D = i_{D1} + i_{D2} \quad (17)$$

$$i_D = i_C + i_R \quad (18)$$

TABLE 2: XFRM_v factors.

	CCM G_{XFRMV} (Config. I to IV)	DCM G_{XFRMV} (Config. VI to IX)	Common factor
$v_{L_{COMA}}$	$\frac{1}{2}$	$\frac{L_{COM}}{L + L_{COM}}$	v_{AG}
$v_{L_{COMB}}$	$\frac{1}{2}$	$\frac{L_{COM}}{L + L_{COM}}$	v_{BG}
v_{L1}	$\frac{1}{2}$	0	$v_{AG} - v_{BG}$
v_{L2}	$\frac{1}{2}$	0	$v_{BG} - v_{AG}$

If $i_R = v_O/R$ and $i_C = C(dv_O/dt)$ are substituted in (18) and the equation is reordered, then (19) is obtained:

$$\frac{dv_O}{dt} = \frac{i_D}{C} - \frac{v_O}{RC} \quad (19)$$

If (19) is integrated, (20) is obtained, which would be the expression for modeling the output voltage v_O

$$v_O = \frac{1}{C} \int i_D dt - \frac{1}{RC} \int v_O dt \quad (20)$$

Equations (1) to (20) and Tables 1 and 2 describe the system model; if you see each equation as a function of input output you can build a block diagram. This diagram is shown in Figure 4.

2.4. System Discretization. The system of Figure 4 is in the time domain; the Laplace transform must be applied to convert it to the domain of the complex variable s . In this diagram, with the exception of the integrators, all are arithmetic operators or gains, so the discretization consisted of replacing the integrators with discrete integrators of the block diagram. The discrete integrator that was used in this

FIGURE 4: Block diagram of the DIBBC described by switching functions.

work has a delay physically feasible, and the transfer function of integration is given in equation (21):

$$H(s) = \frac{1}{s} \quad (21)$$

Equation (21) is discretized by applying the z -transform, obtaining the transfer function of an integrator shown in (22), where T_s is the sampling period:

$$z \left[\frac{1}{s} \right] = \frac{T_s}{1 - z^{-1}} \quad (22)$$

Equation (22) corresponds to an integrator without delay; an integrator with delay according to the delay theorem of the z transform is shown in

$$H(z) = \frac{T_s z^{-1}}{1 - z^{-1}} \quad (23)$$

In Figure 5 a block diagram of the discrete model of the circuit of Figure 1 is shown.

3. Hardware Implementation

For implementation there is a card with a low-end FPGA Altera Cyclone IV E model EP4CE22F17C6N with 22320 LUT. The manufacturer provides the tool to develop systems called Quartus Prime, which allows the implementation of logic and arithmetic, in two languages of hardware description: VHDL and Verilog.

3.1. Arithmetic. Using the tool for IP development (Intellectual Property) of Quartus Prime called LPM Mega Wizard, the additions, subtractions, and multiplications of the model of Figure 4 were implemented. It was decided to use fixed point arithmetic with the format Q (64.32), having 32 bits for the integer part and 32 for the fractional part. The advantage of using fixed point is that the implementation in hardware does not require sequential operations and allows all operations to be performed concurrently. The

decision to use the fixed point format was made taking into account the dynamic range of the signals and the error of the representation of the constants of the system. With this format, the truncation error of the representation of the constants is less than 0.0005%. In Results, an error analysis will be shown over time.

3.2. Switching Functions. Only in the case that there are two possible states such as that of the switches, in hardware you can replace that switch represented by a product in the switching function by a multiplexer, like the functions of (1) to (3). Figure 6 shows how the switching function was implemented. It is observed that the products are replaced by multiplexers, which are controlled by the configuration multiplexers, which allow the input of the coefficients of the $m_{X_{mn}}$ switching matrices. A 64-bit multiplier in hardware for the CYCLONE IV occupies a space of 4352 LUT, while a 64-bit multiplexer occupies only 64 LUT, which represents a reduction of 68 times the hardware space.

4. Results

Four simulations were carried out, the first using a simulator for physical systems, which in this case was SABER 2.4, the second simulation using PWLM evaluated by the Euler method in MatLAB 2015a, the third being the switching functions using a SIMULINK 2015a model and evaluated by the Euler method, and the fourth being the embedded model of the switching functions with the RTL simulation tool included in Quartus Prime 18.00. Table 3 shows the values of the simulation parameters. SABER is a very accurate simulator so it will be the reference to calculate the error. The state variables of the PWLM are i_{L1} , i_{L2} , and v_O , so the graphs for them are displayed. Figures 7, 8, and 9 show the results of the simulations for the time from 0 ms to 10 ms: (a) corresponds to the four simulations, (b) corresponds to the error of the PWLM, the SF evaluated in SIMULINK, and SF evaluated by the FPGA all with respect to SABER, (c) is a zoom between 9.50 ms to 9.55 ms, and (d) is a zoom of the

FIGURE 5: Discrete model of a DIBBC.

FIGURE 6: Hardware implementation for a switching function.

error for the interval of (c). When the system is in steady state it is observed that the errors between the SFs overlap without diverging. The error for i_{L1} at $t = 9.526$ ms for the PWLM is under 1.09%, for both SFs it is 1.22%, the error for i_{L2} at $t = 9.526$ ms for PWLM is 0.83%, and for SFs it is 0.63%; the error for v_O at $t = 9.526$ ms for PWLM is 0.45% and for SFs it is

TABLE 3: Simulation parameters.

Parameter	Value
V_s	350 V
F_{sw}	75 kHz
F_{st}	150 MHz
D	45%
R	4 Ω
L	38 μ H
L_{com}	7 μ H
C	95 μ F

0.44%. It should be noted that the circuit enters the DCM in two regions: when the circuit is turned on at $t = 0$ s and during the transient in the interval $t = 159\mu$ s to $t = 413\mu$ s. The system reaches the steady state at $t = 3.5$ ms.

In terms of hardware implementation, a PWLM for the DIBBC would occupy a space of 79552 LUT in a Cyclone IV. In the case of the switching function model it deals with 9738 LUT (43.63% of the resources of the available card), depending on the Quartus Prime synthesis reports. Other embodiments were made for the PWLM by multiplexing the multipliers: one was multiplexing one row of equation and another was multiplexing rows of matrix. The results are shown in Table 4.

5. Discussion

In order to implement a HIL based on a PWLM whose step size is less than 10 ns in an FPGA, extensive hardware resources are required. It is observed that when using a model based on switching functions and fixed point arithmetic with a high resolution, the space in hardware for its implementation is drastically reduced, allowing the use of a FPGA with few resources and with accuracy similar to that of other implementations and the step size is restricted to the core speed of the FPGA. This implementation is intended to be used for the development of a hybrid power system, since it

FIGURE 7: Analysis of the error of i_{L1} between SABER and PWLM, SF Simulink and SF FPGA. FIGURE 8: Analysis of the error of i_{L2} between SABER and PWLM, SF Simulink and SF FPGA.

FIGURE 9: Analysis of the error of v_O between SABER and PWLM, SF Simulink and SF FPGA.

TABLE 4: Comparison between different implementation strategies.

Implementation	Sampling Frequency	Number of steps per switching cycle F_{sa}/F_{sw}	Multipliers	Resources FPGA (CYCLONE 4 22K)
PWLM multiplier multiplexed in equation row	52.5 MHz	700	3	14.67%
PWLM multiplexer multiplexed in matrix row	105 MHz	1400	9	89.60%
SFM	150 MHz	2000	5	43.63%

is required to embed in a FPGA the models of several power converters, sources, and loads. This implementation can be extended for use in microgrids. The switching functions allow seeing in the systems how the flow of the power is in a natural way so that the power balance does not require a very complex mathematical description that increases the hardware resources of a HIL.

Data Availability

The simulation data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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References

- [1] C. Buccella, C. Cecati, and H. Latafat, "Digital control of power converters—a survey," *IEEE Transactions on Industrial Informatics*, vol. 8, no. 3, pp. 437–447, 2012.
- [2] F. Ji, H. Fan, and Y. Sun, "Modelling a FPGA-based LLC converter for real-time hardware-in-the-loop (HIL) simulation," in

- Proceedings of the 8th IEEE International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia '16)*, pp. 1016–1019, IEEE, China, May 2016.
- [3] C. Liu, R. Ma, H. Bai, Z. Li, F. Gechter, and F. Gao, "Hybrid modeling of power electronic system for hardware-in-the-loop application," *Electric Power Systems Research*, vol. 163, pp. 502–512, 2018.
 - [4] M. Milton, A. Benigni, and J. Bakos, "System-level, FPGA-based, real-time simulation of ship power systems," *IEEE Transactions on Energy Conversion*, vol. 32, no. 2, pp. 737–747, 2017.
 - [5] L. Herrera, C. Li, X. Yao, and J. Wang, "FPGA-based detailed real-time simulation of power converters and electric machines for EV HIL applications," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1702–1712, 2015.
 - [6] J.-M. Timmermans, J. Van Mierlo, P. Lataire, F. Van Mulders, and Z. McCaffree, "Test platform for hybrid electric power systems: development of a HIL test platform," in *Proceedings of the European Conference on Power Electronics and Applications (EPE '07)*, Denmark, September 2007.
 - [7] Z. Jiang, R. A. Dougal, R. Leonard, H. Figueroa, and A. Monti, "Hardware-in-the-loop testing of digital power controllers," in *Proceedings of the 21st Annual IEEE Applied Power Electronics Conference and Exposition (APEC '06)*, pp. 901–906, IEEE, USA, March 2006.
 - [8] H. Li, M. Steurer, K. Shi, S. Woodruff, and D. Zhang, "Development of a unified design, test, and research platform for wind energy systems based on hardware-in-the-loop real-time simulation," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 4, pp. 1144–1151, 2006.
 - [9] P. Vlado, A. Evgenije, G. Stevan, V. Marko, and R. Milan, "Precise PV active power - converter control rapid prototyping framework," in *Proceedings of the 19th International Symposium on Power Electronics (Ee '17)*, pp. 1–6, Serbia, October 2017.
 - [10] F. Montano, T. Ould-Bachir, and J. P. David, "An evaluation of a high-level synthesis approach to the FPGA-based sub-microsecond real-time simulation of power converters," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 636–644, 2018.
 - [11] M. Dagbagi, A. Hemdani, L. Idkhajine, M. W. Naouar, E. Monmasson, and I. Slama-Belkhouja, "ADC-based embedded real-time simulator of a power converter implemented in a low-cost FPGA: application to a fault-tolerant control of a grid-connected voltage-source rectifier," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 2, pp. 1179–1190, 2016.
 - [12] R. Kang, S. Kim, I. Yang, K. Jeong, C. Kang, and G. Kim, "The use of FPGA in HIL simulation of three phase interleaved DC-DC converter," in *Proceedings of the IEEE Vehicle Power and Propulsion Conference (VPPC '12)*, pp. 772–776, IEEE, Republic of Korea, October 2012.
 - [13] H. Kidokoro and M. Nakahara, "FPGA-based hardware-in-the-loop simulator of high switching frequency power converters," in *Proceedings of the IEEE International Telecommunications Energy Conference (INTELEC '15)*, IEEE, Japan, October 2015.
 - [14] C. Dufour, H. Blanchette, and J. Bélanger, "Very-high speed control of an FPGA-based finite-element-analysis permanent magnet synchronous virtual motor drive system," in *Proceedings of the 34th Annual Conference of IEEE Industrial Electronics*, pp. 2411–2416, IEEE, Orlando, Fla, USA, November 2008.
 - [15] P. Le-Huy, S. Guerette, L. A. Dessaint, and H. Le-Huy, "Real-time simulation of power electronics in power systems using an FPGA," in *Proceedings of the 2006 Canadian Conference on Electrical and Computer Engineering*, pp. 873–877, IEEE, Ottawa, Canada, May 2006.
 - [16] C. Liu, R. Ma, H. Bai, F. Gechter, and F. Gao, "A new approach for FPGA-based real-time simulation of power electronic system with no simulation latency in subsystem partitioning," *International Journal of Electrical Power & Energy Systems*, vol. 99, pp. 650–658, 2018.
 - [17] S. Ben Said, K. Ben Saad, and M. Benrejeb, "HIL simulation approach for a multicellular converter controlled by sliding mode," *International Journal of Hydrogen Energy*, vol. 42, no. 17, pp. 12790–12796, 2017.
 - [18] T. Ould Bachir, C. Dufour, J. Bélanger, J. Mahseredjian, and J. David, "A fully automated reconfigurable calculation engine dedicated to the real-time simulation of high switching frequency power electronic circuits," *Mathematics and Computers in Simulation*, vol. 91, pp. 167–177, 2013.
 - [19] R. Razzaghi, M. Mitjans, F. Rachidi, and M. Paolone, "An automated FPGA real-time simulator for power electronics and power systems electromagnetic transient applications," *Electric Power Systems Research*, vol. 141, pp. 147–156, 2016.
 - [20] F. Gomez-Olguin, I. Araujo-Vargas, T. Granados-Luna, P. Velazquez-Elizondo, K. Cano-Pulido, and A. Villarruel-Parra, "Design and assessment of a 30 kW/75 kHz DC-DC, two-phase dual interleaved buck-Boost converter," in *Proceedings of the 2nd IEEE Texas Power and Energy Conference (TPEC '18)*, pp. 1–6, IEEE, USA, February 2018.