

Research Article

Improved Error Correction Methods for Filterless Digital Class D Audio Power Amplifier Based on FCLNF

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Aiming at correcting the error caused by the nonlinear and power supply noise of the bridge-tied-load (BTL) power stage of the filterless digital class D power amplifier, an error correction method was proposed based on feedforward power supply noise suppression (FFPSNS) and first-order closed loop negative feedback (FCLNF) techniques. This method constructed the first-order LCLNF loop for the power stage and further reduced the impact of the power supply noise on the power amplifier output by using FFPSNS technology to introduce the power supply noise into the feedback loop at the same time. The 0.35 μm CMOS process is used for analysis and comparison in Cadence. Cadence simulation results indicate that PSRR at the power supply noise frequency of 200 Hz is improved with 36.02 dB. The power supply induced intermodulation distortion (PS-IMD) components are decreased by approximately 15.57 dB and the signal-to-noise ratio (SNR) of the power amplifier is increased by 17 dB. The total harmonic distortion + noise (THD + N) of the power amplifier is reduced to 0.02% by FCLNF + FFPSNS.

1. Introduction

In recent years, the country has promoted high-efficiency and energy-saving technologies and encouraged the strengthening of high-efficiency and energy-saving technological transformations and key technological breakthroughs. With the rise of audio and video equipment for low-power applications, filter-free digital class D audio power amplifiers have high power efficiency and easy interface with digital audio sources, which are favored by researchers in the industry [1]. And in the 11 key technologies evaluated by IEEE Spectrum in the past ten years, it is predicted that high-efficiency class D audio amplifiers will eventually unify the audio amplifier market [2]. However, its own nonideal state and power supply noise can cause serious distortion of the output signal of the power amplifier.

Digital class D power amplifiers have received increasing attention due to their advantages of high power efficiency, easy system transplantation, and resistance to external interference [3]. The traditional digital class D power amplifier is usually composed of a digital switching signal modulator,

a power stage, and an inductive capacitor (LC) analog low-pass filter. The digital switching signal modulator mostly uses uniform-sampling pulse width modulation (UPWM) technology realization. The LC low-pass filter of the traditional digital class D power amplifier occupies about 75% of the volume of the entire power amplifier system and consumes about 30% of the cost, which severely hinders the portable application of digital class D power amplifiers [4]. The filter-free digital class D power amplifier, as a new type of digital class D power amplifier, can drive the loudspeaker to work without the need of an LC low-pass filter through a special modulation technique and maintain high power efficiency to meet the needs of digital audio with the development of equipment miniaturization; the filter-free digital class D power amplifier has become a research hotspot in the current power amplifier field [5].

In order to enable the digital class D audio power amplifier to achieve high power supply rejection ratio (PSRR), power supply-induced intermodulation Distortion (PS-IMD), signal-to-noise rate (SNR), and total harmonic distortion + noise (THD + N), two large error sources need

to be corrected for the nonidealities and the power level source noise introduced by the power level [6].

For filter-free digital class D power amplifiers, the errors introduced by the nonlinearity and nonideal working conditions of the power stage, especially the errors introduced by the power supply noise of the power stage, seriously affect the output performance of the power amplifier [7, 8]. Although the power amplifier's power supply rejection ratio (PSRR) can theoretically reach infinity when the upper and lower half bridges of the bridge-tied-load (BTL) power stage of the power amplifier are completely matched, the power supply interference is caused by the power supply noise. The modulation distortion (PS-IMD) is still large. In response to this problem, Donida et al. [7] and Mostert et al. [8] introduced the output signal of the power amplifier to the input of the power amplifier by establishing a global closed-loop negative feedback loop including a digital switching signal modulator and a power stage. Precorrection is performed in the terminal or switching signal modulator to achieve the purpose of correcting the power level error, but an additional analog-to-digital converter (ADC) is required, which leads to a substantial increase in system cost. Chen et al. [9] and Cellier et al. [10] built a local closed loop negative feedback (LCLNF) loop containing only the power level to correct the power level error. This method is ensuring the system. In a stable condition, the ability to suppress the noise of the power level power supply is weak. In summary, there are currently fewer error correction methods for the power stage of the filter-free digital class D power amplifier, and the existing digital class D power amplifier power stage error correction method may have a higher cost of implementation, or the power stage power error. The correction ability is weak.

Aiming at the above two major error sources, Dong Jun Lee and Jinho Noh et al. used the local negative feedback technology to establish a power-level noise suppression module between the switch signal modulator and the power level, but it would cause an increase in the power level switching frequency [11, 12]. There are also the use of analog negative feedback control loop schemes and the use of power-level power supply noise feedforward precorrection technology [13–15]. The scheme is complex and requires the use of ADC to convert power source noise into digital signals. In [16], a feedforward noise technology for class D audio amplifier with single end (SE) output structure is proposed, but this method is applied to class D audio amplifier with SE output structure, and the system contains an off-chip LC low-pass filter. This paper designs a first-order closed-loop negative feedback (FCLNF) error correction method for the filter-free digital class D audio power amplifier bridge-tied-load (BTL) power stage and the FCLNF suitable for the filter-free digital class D audio power amplifier BTL power stage plus feedforward power supply noise suppression (FCLNF + FFPSNS) error correction method.

2. FCLNF + FFPSNS Error Correction

Class D power stage is one of the key modules of the filter-free digital class D amplifier. Its function is to amplify the weak PWM signal to drive the low impedance speaker. Its

input signal and output signal are both digital PWM signals. Since the ripple noise contained in the power supply and the nonideal state of the power stage itself affect the quality of the output signal, it is necessary to perform error correction on the open loop power stage.

Filter-free digital class D audio power amplifier is mainly composed of digital UPWM modulator and BTL power stage. The former is a digital part and the latter is an analog part. Its structure is shown in Figure 1. It can be seen from Figure 1 that the filter-free digital class D audio power amplifier can be divided into UPWM modulator, open-loop BTL power stage, and loudspeaker as a whole. The UPWM modulator is a digital circuit, and the open-loop BTL power stage is an analog circuit. UPWM modulator consists of the digital interpolation filter, in-phase and inverted unity gain buffer, Sigma-Delta modulator, and UPWM generator.

2.1. Principle Analysis of FCLNF Error Correction. FCLNF circuit is composed of compensation module, remodulation module, BTL power level, and some passive components [3, 17]. Its circuit and equivalent model are shown in Figure 2. There V_{IN_P} and V_{IN_N} are, respectively, the input signals and V_{CM} is the common mode voltage or reference voltage.

F_1 and F_2 are transfer functions from the input signal of V_{IN_P} and V_{IN_N} to the inverting input of the integrator. G_{int1} and G_{int2} are the integrator gains of the upper and lower bridges, respectively. H_1 and H_2 are the feedback factors of the upper and lower bridges, respectively. G_{M1} and G_{M2} are the combined linear gain of the power level and the remodulation module.

Under ideal conditions,

$$G_{M1} = G_{M2}, V_{IN_P} = V_{IN_N} = 0, \quad (1)$$

if the deviation between the two feedback paths is ε .

The mismatch factor between resistances is r ($0 < r < 1$), mismatch factor between capacitors is c ($0 < c < 1$), and ε is equivalent to $r + c$,

The PSRR of power amplifier using the FCLNF method is

$$PSRR_{FCLNF} = 20 \lg [LG_2(s)] - 20 \lg (r + c). \quad (2)$$

2.2. Principle Analysis of FCLNF + FFPSNS Error Correction. FFPSNS feeds the power stage power supply noise forward to the power stage front-end module for precorrection through certain means. The feedforward control network subtracts the feedforward power supply noise from the PWM input signal and then quantifies the power supply noise through the comparator. The power supply noise is converted into the effective duty cycle of PWM signal, so as to achieve the purpose of correcting the power supply noise. This proposal is composed of FCLNF module, FFPSNS module, remodulation module, and BTL power level [18, 19]. Its schematic diagram and equivalent model are shown in Figure 3.

There V_{IN_P} and V_{IN_N} are, respectively, the input signals of the upper and lower half bridges of the power port in the power amplifier. V_{CM} is the common mode voltage or

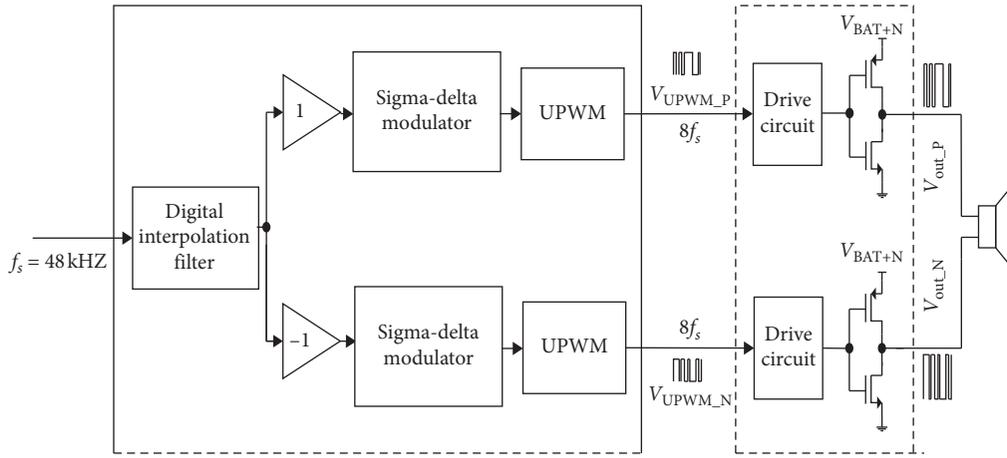


FIGURE 1: Block diagram of filterless digital class D power amplifier.

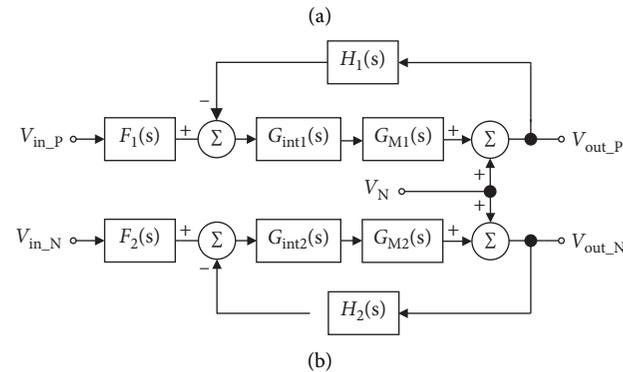
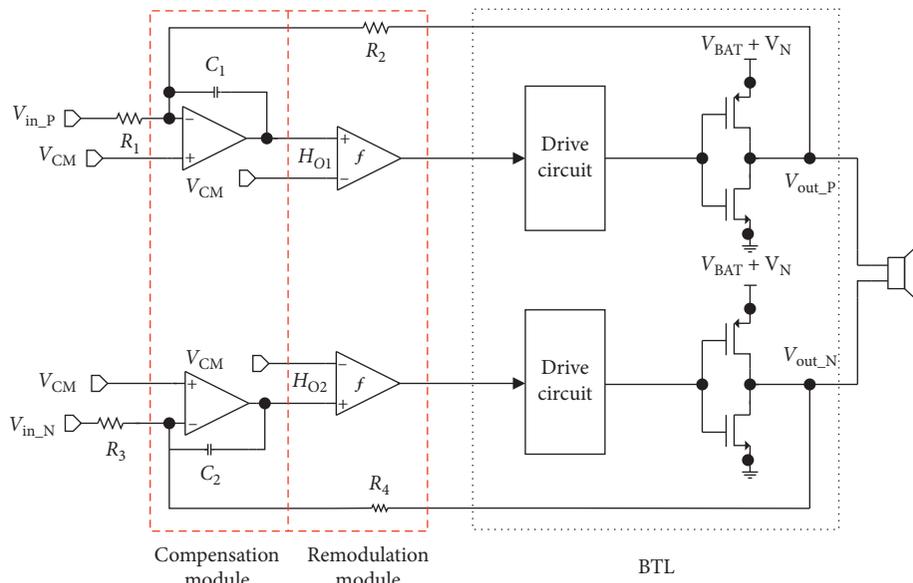


FIGURE 2: Diagram of FCLNF correction circuit. (a) Block diagram of FCLNF correction. (b) Mathematical model diagram of FCLNF correction.

reference voltage. R_f is feedback resistance. V_{A1} and V_{A2} are the output signals of the integrator. V_{F1} and V_{F2} are the output signals of FFPSNS module. $R_1 - R_5$, R_f , R_i , C_1 and $R'_1 - R'_5$, R'_f , R'_i , C'_1 have the same physical meaning and value.

F_1 and F_2 are transfer functions from the input signal of V_{IN_P} and V_{IN_N} to the inverting input of the integrator. G_{int1} and G_{int2} are the integrator gains of the upper and lower bridges, respectively. H_1 and H_2 are the feedback factors of the upper and lower bridges, respectively. G_{M1} and

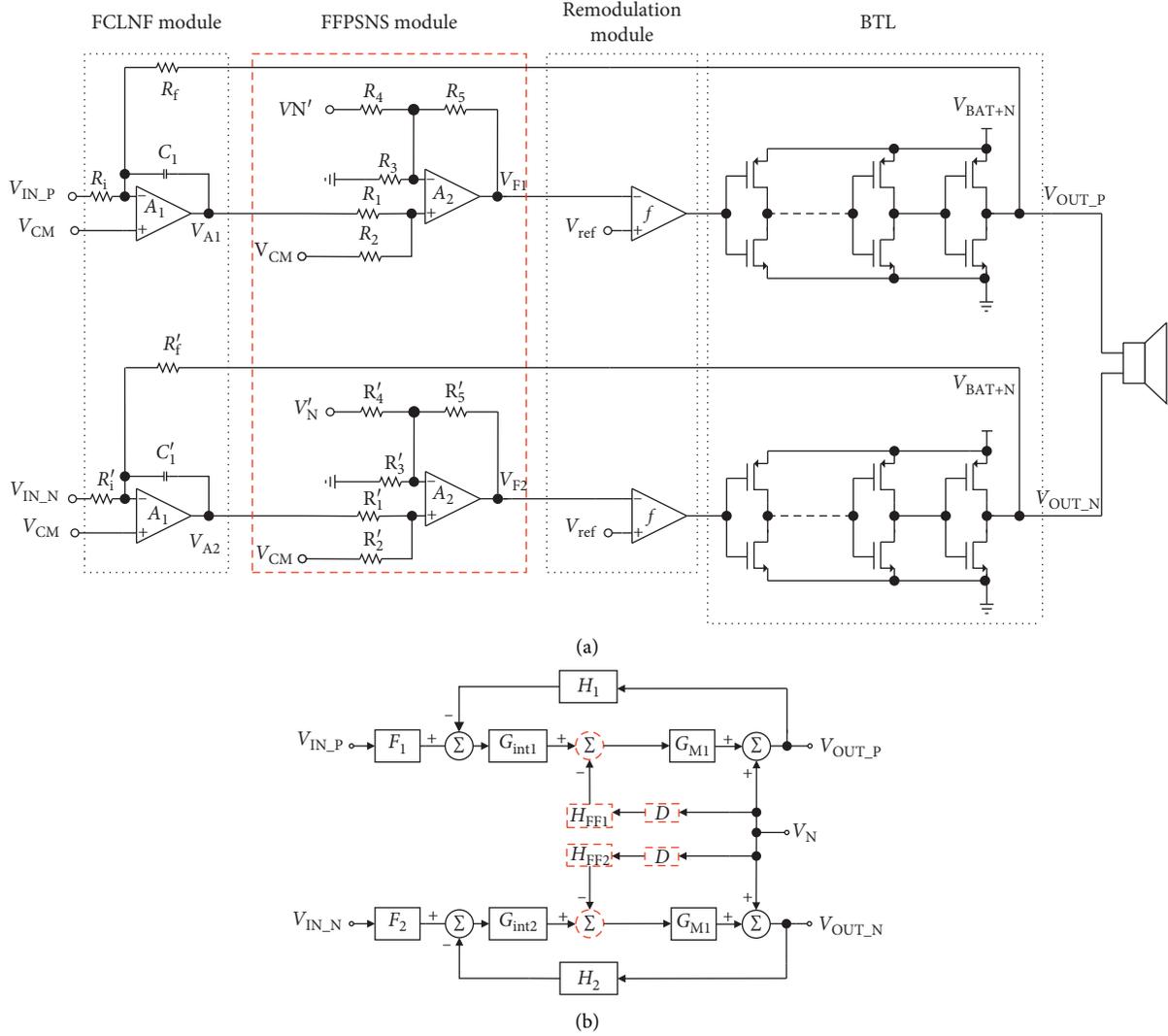


FIGURE 3: Diagram of FCLNF + FFPSNS correction circuit. (a) Block diagram of FCLNF + FFPSNS correction. (b) Mathematical model diagram of FCLNF + FFPSNS correction.

G_{M2} are the combined linear gain of the power level and the remodulation module. D is the power supply noise scaling factor. H_{FF1} and H_{FF2} are the transfer function of feed-forward path.

Under ideal conditions, $H_{FF1} = H_{FF2}$, $G_{M1} = G_{M2}$, and $V_{IN_P} = V_{IN_N} = 0$ if the deviation between the two feedback paths is ϵ .

The deviation between H_{FF} theory and actual situation is β . The mismatch factor between resistances is r ($0 < r < 1$), mismatch factor between capacitors is c ($0 < c < 1$), and ϵ is equivalent to $r + c$.

The PSRR of power amplifier using the FCLNF + FFPSNS method is

$$\begin{aligned} \text{PSRR}_{\text{FCLNF+FFPSNS}} \\ = 20 \lg [LG_2(s)] - 20 \lg(r + c) - 20 \lg(|\beta|). \end{aligned} \quad (3)$$

2.3. Circuit Design of Improved Error Correction Method.

The double-input single-output folding cascode two-stage Miller compensation operational amplifier used in this paper is shown in Figure 4.

Based on the proposed power stage error correction method, the circuit implementation of the filter-free digital class D power amplifier BTL power stage with error correction is implemented. It can be seen from Figure 1 that the operational amplifier and voltage comparator are the key modules for this method. The operational amplifier A_1 uses a double-input single-output folding cascode two-stage Miller compensation architecture, as shown in Figure 4. In the figure, V_{DD} is the power supply voltage; V_{b1} , V_{b2} , V_{b3} , and V_{b4} are the bias voltages of the operational amplifier; V_O is the output signal of the operational amplifier; V_{in1} and V_{in2} are the input signals of the operational amplifier; C_m is the Miller compensation capacitor; and resistance is R_m . By

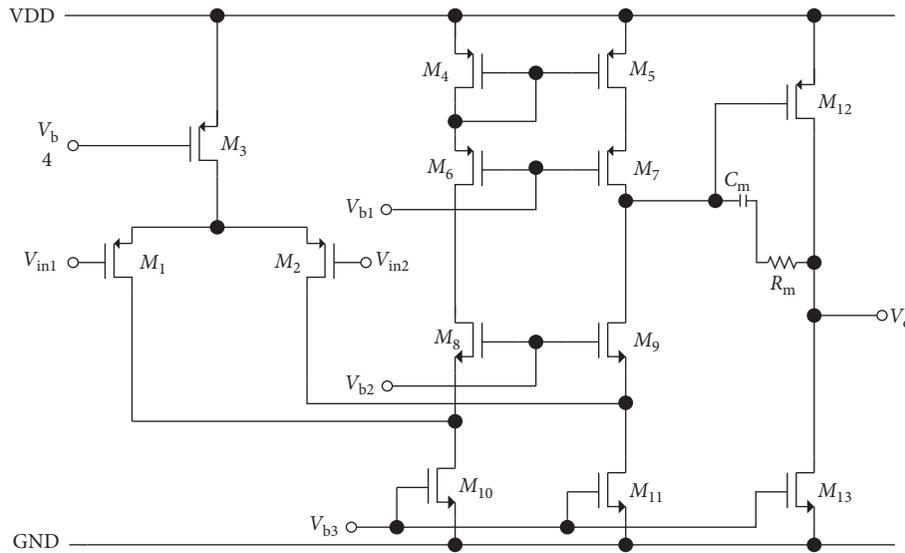


FIGURE 4: Structure of the operational amplifier.

connecting with C_m in parallel to improve the stability of the operational amplifier, the unity gain bandwidth and phase margin of the operational amplifier A_1 are 13 MHz and 70.3° , respectively, and the open loop gain is 109.9 dB, and the PSRR at 100 Hz is 95 dB. The feedforward operational amplifier A_2 also uses the architecture of Figure 4, with unity gain bandwidth and phase margin of 10 MHz and 68° , respectively.

The voltage comparator circuit structure is relatively simple, and its circuit is shown in Figure 5. In the figure, V_{in1} and V_{in2} are the input signals of the voltage comparator and V_O is the output signal of the voltage comparator. The comparator uses a two-stage amplification architecture. The first stage of amplification uses a differential amplifier circuit structure and a differential circuit to suppress common mode interference. The second-stage amplification adopts a cascode circuit to control the offset voltage well. The output stage adopts the push-pull output to increase the driving capability of the output, while adding an inverter to the output stage can enhance the response time of the comparator. After simulation, the output waveform of the comparator has a rise time of 560 ps and a fall time of 720 ps.

2.4. Simulation and Result Analysis. In order to verify the error correction effect of the above scheme, the simulation experiment route adopted in this paper is shown in Figure 6. The experimental simulation in this paper is based on Matlab and Cadence. Specifically, Matlab is used to generate the two PWM signal sources required by Cadence simulation, and the signal data exported by Matlab is saved as .dat file. In Cadence, V_{source} module is used to store the waveform data in pwl type in Cadence and use it as the signal for Cadence simulation Source. FCLNF control circuit containing BTL power level was built on Cadence platform, and then Cadence Spectre simulator was used for transient simulation of the system. Finally after sampling in Cadence, import the.csv

file into Matlab for spectrum analysis and performance calculation.

In this scheme, ASMC $0.35 \mu\text{m}$ CMOS process is adopted to design and build the circuit on Cadence platform. The simulation conditions are mos_tt process angle and the temperature is 27°C . FCLNF control circuit works under 5 V DC power supply voltage, that is, V_{DD} is 5 V, while the BTL power stage works under 10 V DC power supply voltage. VCM is half of the working voltage of the negative feedback control circuit, and an 8Ω resistor is used as the load RL of the BTL power stage. The input signal of power amplifier is 24-bit sinusoidal single frequency digital signal (frequency is 1 kHz and amplitude is -5 dB). The UPWM waveform data generated by Matlab is input into the simulation circuit through the V_{source} component in Cadence. The transient simulation time is 42.7 ms. The simulation output waveform is sampled and exported at an interval of 40.69 ns (the sampling frequency is 24.6 MHz). The simulation result is shown in Figure 7.

In Figure 7, after FCLNF correction, the power amplifier's PSRR at 200 Hz power source noise frequency was equal to 82.8 dB, and the PSRR increased by 36.02 dB. The PS-IMD of the power amplifier is approximately equal to -80.63 dB, reducing by 34.73 dB. The SNR was increased to 85.7 dB and the SNR performance was much higher than that of the output signal of the uncorrected scheme (58.59 dB), which improved by 27.11 dB. The output THD + N performance of the power amplifier was reduced to 0.0356%, far less than the output THD + N (0.464%) of the power amplifier without correction scheme. Figure shows that the PSRR of FCLNF + FFPSNS corrected power amplifier at 200 Hz power noise frequency is 84.3 dB, which is close to the performance of PSRR in FCLNF.

The influence of power level source noise amplitude on the performance of power amplifier PSRR and PS-IMD is shown in Figures 8 and 9.

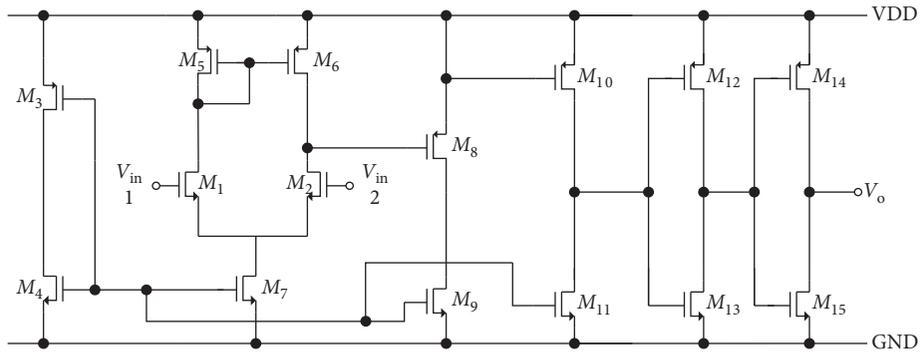


FIGURE 5: Structure of the voltage comparator.

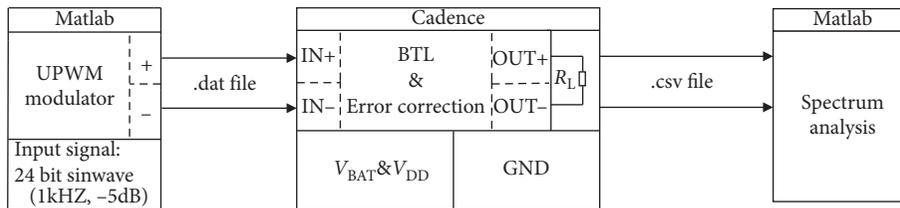


FIGURE 6: Block diagram of experimental.

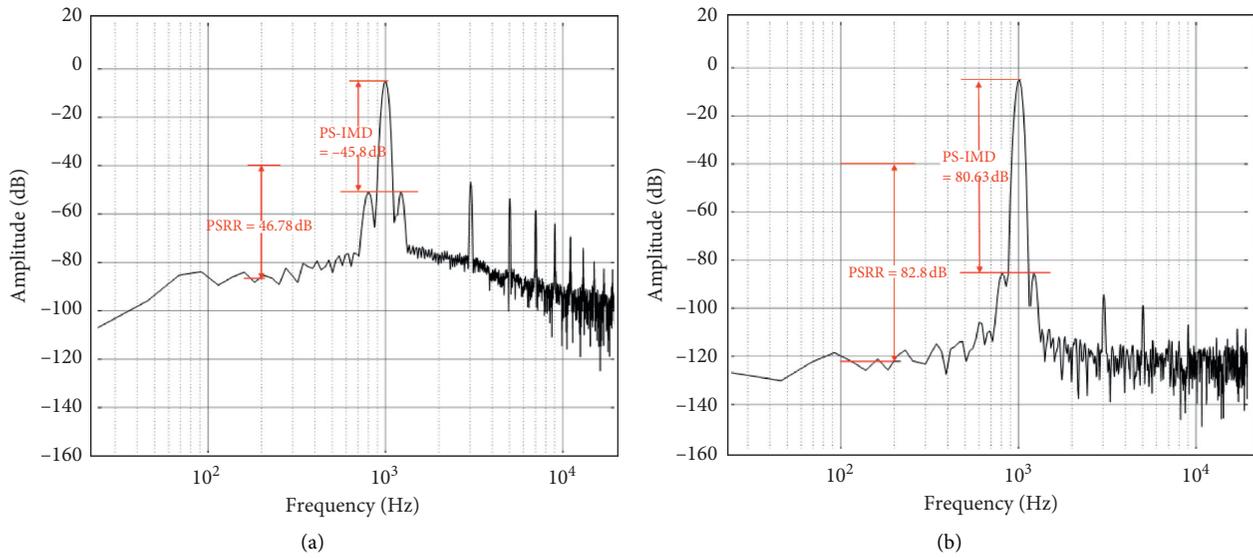


FIGURE 7: Continued.

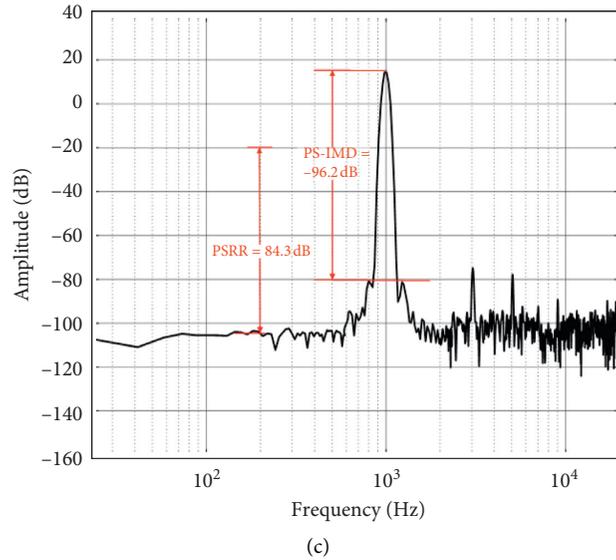


FIGURE 7: Spectrum diagram of power output signal. (a) Uncorrected. (b) FCLNF corrected. (c) FCLNF + FFPSNS corrected.

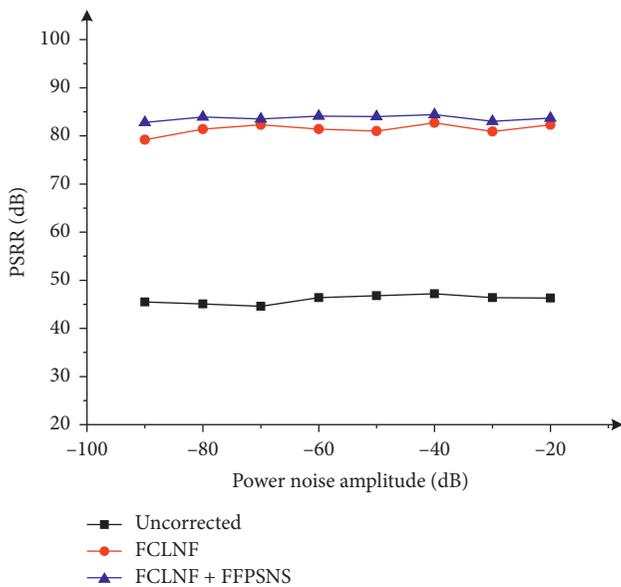


FIGURE 8: Contrast diagram of PSRR vs. power noise amplitude.

The power supply noise amplitude increased from -90 dB to -20 dB. Regardless of whether it is calibrated or not, the power amplifier’s PSRR remained basically unchanged with the increase of power supply noise amplitude, and the PSRR corrected by FCLNF and FCLNF + FFPSNS is significantly higher than that by uncorrected. The PSRR characteristics of the two correction schemes are basically the same.

The PS-IMD of the power amplifier does not change with the noise amplitude of the power supply. After FCLNF correction and FCLNF + FFPSNS correction, when the power supply noise amplitude is low (< -70 dB), PS-IMD is basically unchanged. This is because of the background noise in the output signal spectrum. The amplitude of the

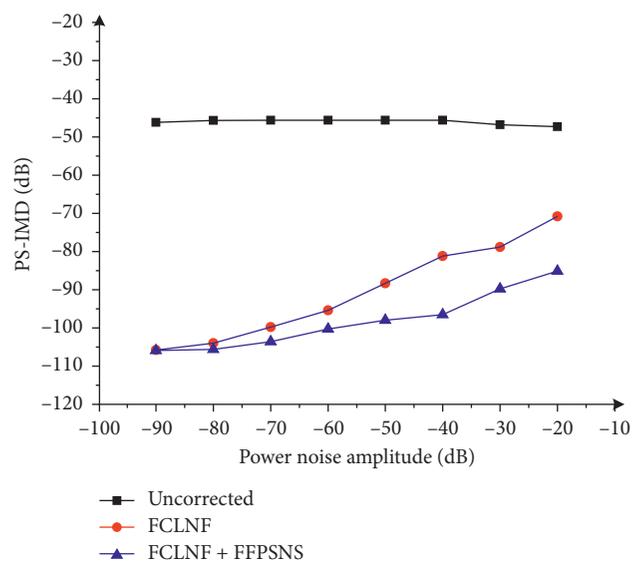


FIGURE 9: Contrast diagram of PS-IMD vs. power noise amplitude.

intermodulation components generated by the power supply noise and the input signal is basically the same as the background noise amplitude. However, as the noise amplitude of power supply continues to increase, PS-IMD of power amplifier starts to increase, and PS-IMD performance declines. This is due to the intermodulation component generated by the power supply noise and the input signal is higher than the background noise when the power supply noise amplitude increases to a certain extent and the PS-IMD characteristics of the two correction schemes are basically equivalent.

Figure 10 compares the changes in the PSRR of the power amplifier with the power supply noise frequency when the three solutions are used. It can be seen from Figure 6 that, whether corrected or not, the PSRR of the

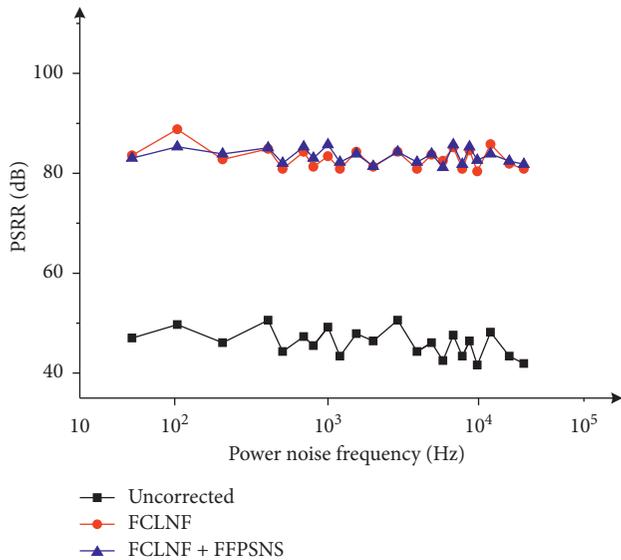


FIGURE 10: Contrast diagram of PSRR vs. power noise frequency.

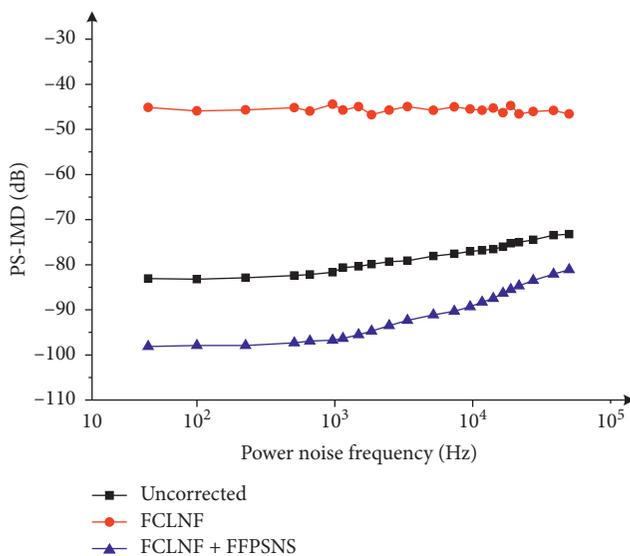


FIGURE 11: Contrast diagram of PS-IMD vs. power noise frequency.

power amplifier will not change drastically as the noise frequency of the power stage power supply increases, and the PSRR of the power amplifier after correction by LCLNF + FFPSNS and LCLNF is significantly higher than the PSRR of the uncorrected power amplifier.

Figure 11 compares the changes of the PS-IMD of the power amplifier with the power supply noise frequency when the three schemes are used. As the power supply noise frequency increases, the PS-IMD of the uncorrected power amplifier is relatively large and basically remains unchanged, while the PS-IMD of the power amplifier after correction using LCLNF and LCLNF + FFPSNS changes slowly at low frequencies (<1000 Hz). At high frequencies (>1000 Hz), the PS-IMD increases significantly, which is caused by the limited gain bandwidth product of the operational amplifier in the correction circuit, but the PS-IMD is smaller than the

uncorrected one. At the same time, the PS-IMD of the power amplifier after LCLNF + FFPSNS correction is significantly smaller than the LCLNF correction scheme.

In summary, the PSRR of the power amplifier after correction by LCLNF and LCLNF + FFPSNS is basically not affected by the amplitude and frequency of the power stage power supply noise. With the change of the noise amplitude and frequency of the power stage power supply, the PS-IMD of the power amplifier after correction by LCLNF + FFPSNS is significantly lower than that after correction by LCLNF. At the same time, the power-stage power supply noise amplitude has a more significant impact on the PS-IMD of the power amplifier than the power supply noise frequency.

3. Concluding Remarks

Under the same experimental conditions, the two correction schemes were compared and analyzed. The results show that compared with the uncorrected power level, the performance of PSRR at 200 Hz source noise frequency is improved by 36.02 dB after FCLNF correction. The PS-IMD component was approximately reduced by 34.73 dB. SNR performance improved by 27.11 dB, and THD + N decreased significantly. Compared with only using FCLNF error correction scheme, the performance of the power amplifier using FCLNF + FFPSNS error correction scheme is comparable at 200 Hz power supply noise frequency. However, the PS-IMD of the power amplifier decreased by 15.57 dB. SNR was further improved by 17 dB, and THD + N dropped further down to 0.02%.

Data Availability

The whole result data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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