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Research Article

Analytical Modelling and Verification of Bus-Clamping Modulation Technique for Switched-Capacitor Converter

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Space vector modulation techniques have advantages of high output voltages and reduced harmonic content as they utilize the dc bus effectively. Bus-clamped pulse width modulation classified in space vector techniques has the ability to reduce the switching losses of the converter and has reduced harmonic distortion. This paper provides mathematical analysis for 60-degree bus-clamping strategy to obtain the complete closed-form solution for finding the harmonic coefficients using double Fourier integral expression. The effectiveness of the bus-clamped approach on switched capacitor based multilevel inverter has been shown with comparison to Sinusoidal PWM. The DSP controller TMS320F240 has been chosen for the real-time implementation of 60-degree bus-clamping modulation technique. Simulation and experimental results of the prototype are presented for RL load at different modulation indices showing the superiority of the configuration to cascaded multilevel inverter.

1. Introduction

Research and development are focused on renewable energies, as they are the major future solution to the increasing energy demand. Power electronic converters with improved efficiency play a vital role in energy harvesting and supply to the power system through dedicated controls [1]. This led to the innovation of a wide range of power converter topologies. The research is still in progress to develop the most efficient and reliable converters. Multilevel inverters are the most commercial converter topologies enabling the medium voltage grid-connection. Multilevel inverters have replaced the earlier used three-level inverters because of their high-quality output waveform, low voltage stress, and reduced switching losses [2, 3]. The first prototype of multilevel inverter was made in USSR and was presented in [4]. Development of this prototype has given the idea for the latest schemes of the multilevel inverter.

There are three conventional multilevel inverter categories: (1) Diode-Clamped (Neutral Point Clamped) Multilevel Inverter (DCMLI) [5], (2) Capacitor Clamped (Flying Capacitor) Multilevel Inverter (CCMLI) [6], and (3) Cascaded Multilevel Inverter (CMLI) [7]. DCMLI has some drawbacks like an unequal rating of the devices, the high-voltage rating of blocking diode, and voltage unbalance. CCMLI uses a large number of capacitors and requires a special technique to balance the capacitor voltages. In CMLI, the problem of voltage unbalancing does not arise, but it requires number of isolated DC supplies for higher levels. Due to the limitations, many efforts were being made to develop more multilevel topologies suitable for different applications. Many multilevel inverter topologies with reduced power devices and higher voltage levels have been presented with improvement in efficiency [8–11]. The two main challenges for the converter are the quality of the output waveform and boosting of the input voltage. At first, transformers are being served for boosting of the input voltage. But the use of transformer increases the size and cost of the system and decreases efficiency. This encouraged the research towards the transformerless topologies. The first transformerless topology with boosting capability was introduced in [12]. This type of converter uses switched-capacitor concept

to boost the input voltage. But this includes a number of switches and has certain limitations on a number of output levels. Later many switched capacitor based topologies have been introduced to overcome those limitations [13, 14]. In [13], a topology has been introduced with the advantage of extending a number of levels with reduced number of power switches. This topology has inherent voltage balancing capability and a simplified gating circuit. A new hybrid topology has been introduced in [14] which have an advantage of cascading the units. This topology produces output levels based on the input voltage applied to the cascaded unit.

Space vector modulation is an advanced technique used in three-phase inverters. SVPWM method has the following advantages: good utilization of dc-link voltage, low current ripple, and relatively easy hardware implementation by a digital signal processor (DSP) [15]. These features make it suitable for high-voltage high-power applications. The major drawback of this technique is when the number of levels increases, this method becomes more complex. Conventional SVPWM has better spectral performance but higher switching losses. Bus-clamping techniques are the discontinuous space vector strategies to reduce the switching losses [16]. In these techniques, each phase is clamped to either positive or negative DC bus for a particular duration. The phase to be clamped and the duration of clamping depend on the orientation of desired reference voltage vector. In 30-degree clamping, each phase gets clamped for duration of 30 degrees in every quarter cycle. In 60-degree clamping, the duration is of 60 degrees for a half cycle of the phase. 60-degree strategies perform better when compared to 30-degree clamping at higher modulation indices [17].

In this paper, the analytical solution for the BC-PWM has been proposed and verified using the platform of DSP controller TMS320F240. The superiority of the technique is shown by comparison with the preexisting control strategies. The reduction in losses has been compared over cascaded multilevel converter and observed the improvement in the efficiency.

2. Topology Description

The proposed converter operation is based on switched-capacitor scheme. Switched-capacitor unit has a capacitor whose role is similar to the transformer. It has an advantage of boosting the input voltage by using a simple technique. The boosting of voltage level obtains by a series-parallel combination of the capacitor with the input voltage. When the capacitor is in parallel to the input voltage it gets charged and when in series it gets discharged supporting the input voltage as illustrated in Figure 1. Thus the boosting of the voltage is achieved without the use of a transformer.

Operation of Basic SC Unit. Basic unit consists of two power switches, a diode, and a capacitor as shown in Figure 2. When the switch *Sa* is turned OFF and *Sb* is turned ON, the capacitor comes in parallel with the supply voltage. During this stage, the capacitor gets charged to the supply voltage.

$$V_{\text{out}} = V_C = V_{\text{in}}. \tag{1}$$

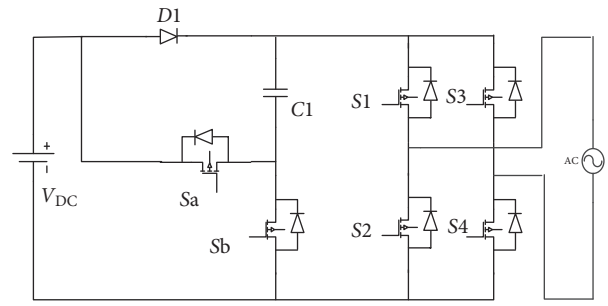

Figure 1: Detailed switched-capacitor multilevel inverter.

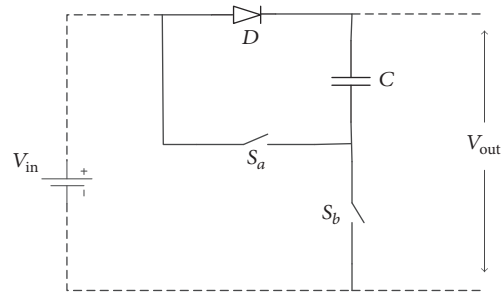

Figure 2: Single unit of switched-capacitor cell.

When the switch *Sa* is turned ON and *Sb* is turned OFF, the capacitor is in series with the supply voltage and increases the output voltage.

$$\begin{aligned} V_{\text{out}} &= V_C + V_{\text{in}} \\ V_{\text{out}} &= 2V_{\text{in}} \quad (\because V_C = V_{\text{in}}). \end{aligned} \tag{2}$$

Both the switches *Sa* and *Sb* work complementary to each other and prevent the supply voltage from being short. The diode in the circuit prevents the capacitor discharging to the source. Thus the output voltage is greater than input voltage without any transformer, thus reducing the size and cost of the circuit. The level of output voltage depends on the number of SC units used in the circuit.

Level-Zero. In Figure 1, when switch *S*1 is turned ON and the remaining switches of the H-bridge are turned OFF, a zero-level voltage is produced at the output. Freewheeling current can pass through switch *S*1 and the bypassing diode of switch *S*3 in case if the load is inductive in nature. Zero-level voltage can also be obtained when the switch *S*2 is turned ON and the remaining switches of the H-bridge are turned OFF. In this case, the path for freewheeling current is through switch *S*2 and the bypassing diode of switch *S*4.

Level-1V. Switch *Sa* is turned OFF and *Sb* is turned ON. Now, the capacitor comes in parallel to the input voltage source. At this stage, the capacitor gets charged eventually and the voltage across the capacitor becomes equal to the input voltage *V* dc. This provides +1*V* dc input to the H-bridge and, by turning ON *S*1 and *S*4 of the H-bridge +1*V* dc, voltage level can be produced at the output as displayed in Figure 3.

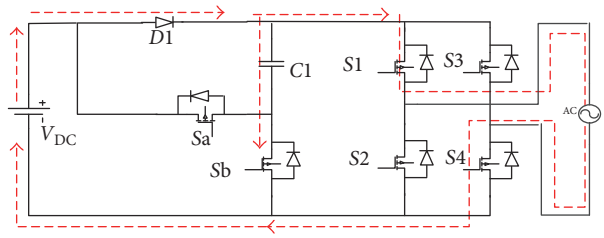

Figure 3: Switching operation for $1V$-level output.

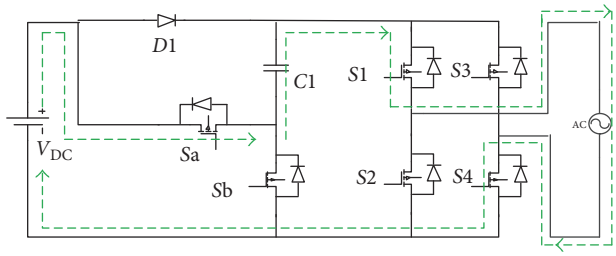

Figure 4: Switching operation for $2V$-level output.

Similarly, by turning ON $S2$ and $S3$ $-1V$dc, voltage can be produced.

Level-2V. Switch *Sa* is turned ON and *Sb* is turned OFF. Now, the capacitor comes in series to the input voltage source. At this stage, the capacitor starts discharging and supports the input voltage. Since the capacitor is previously charged to Vdc, this provides $+2V$dc input to the H-bridge and, by turning ON $S1$ and $S4$ of the H-bridge $+2V$dc, voltage level can be produced at the output as illustrated in Figure 4. Similarly, by turning ON $S2$ and $S3$ $-1V$dc, voltage can be produced. Switching states have been illustrated in Table 1.

3. Control Algorithm

The space vector modulation (SVPWM) can be easily implemented to all types of multilevel inverters. These vector diagrams are universal regardless of the type of multilevel inverter used. The adjacent three vectors can produce the desired voltage vector by computing the duty cycle ratio (T_j, T_{j+1} and T_{j+2}) for each vector based on the principle of volt-second equivalence [16]:

$$TV^* = \left(T_jV_j + T_{j+1}V_{j+1} + T_{j+2}V_{j+2}\right). \tag{3}$$

Space vector PWM methods generally have the following features: good utilization of dc-link voltage, low current ripple, and relatively easy hardware implementation by a digital signal processor (DSP). These features make it suitable for high-voltage high-power applications. At different switching frequency, SVPWM has better output results, increased efficiency, and reduced THD when compared to the inverters with SPWM technique. The main drawback of this technique is, as the number of levels increases, redundant switching states and the complexity of selecting switching states increase.

Table 1: Switching states for five-level output.

Level	*Sa*	*Sb*	*S1*	*S2*	*S3*	*S4*
$2V$	1	0	1	0	0	1
$1V$	0	1	1	0	0	1
0	1	0	0	1	0	1
$-1V$	0	1	0	1	1	0
$-2V$	1	0	0	1	1	0

Conventional SVPWM has better spectral performance but higher switching losses. Bus-clamping techniques are the discontinuous space vector strategies to reduce the switching losses [6]. This paper presents the implementation and comparison of bus-clamping strategy over SPWM techniques. In these techniques, each phase is clamped to either positive or negative DC bus for a particular duration by adding a common mode signal.

$$\begin{aligned} m_R &= (M * v_R) + m_{\text{cm}} \\ m_Y &= (M * v_Y) + m_{\text{cm}} \\ m_B &= (M * v_B) + m_{\text{cm}}, \end{aligned} \tag{4}$$

where v_R, v_Y, and v_B are the three phases, M is the modulation index, and m_{cm} is the common mode signal. m_R, m_Y, and m_B are the resulting modulating signal. The phase to be clamped and the duration of clamping depend on the orientation of desired reference voltage vector. In 30-degree clamping, each phase gets clamped for the duration of 30 degrees in every quarter cycle. In 60-degree clamping, the duration is of 60 degrees for a half cycle of the phase. 60-degree strategies perform better when compared to 30-degree clamping at higher modulation indices [7]. In this paper, 60° bus-clamping technique has been discussed.

The common mode signal is generated based on the following:

$$m_{\text{cm}} = \begin{bmatrix} 2A_C - (M * v_Y) & -\pi < \omega_O t < \dfrac{-2\pi}{3} \\ -2A_C - (M * v_R) & \dfrac{-2\pi}{3} < \omega_O t < \dfrac{-\pi}{3} \\ 2A_C - (M * v_B) & \dfrac{-\pi}{3} < \omega_O t < 0 \\ -2A_C - (M * v_Y) & 0 < \omega_O t < \dfrac{\pi}{3} \\ 2A_C - (M * v_R) & \dfrac{\pi}{3} < \omega_O t < \dfrac{2\pi}{3} \\ -2A_C - (M * v_B) & \dfrac{2\pi}{3} < \omega_O t < \pi \end{bmatrix}, \tag{5}$$

where A_C is the amplitude of the sinusoidal modulating signal. The common mode signal using (5) is obtained and this generated signal is added to each of the phases to get the required modulating signal as in Figure 5. The inverter output for the 60-degree bus-clamping technique has been shown in Figure 6. From the output waveform, it can be observed that there is no switching during the clamping period of the phase. This reduces the switching losses of the converter. In

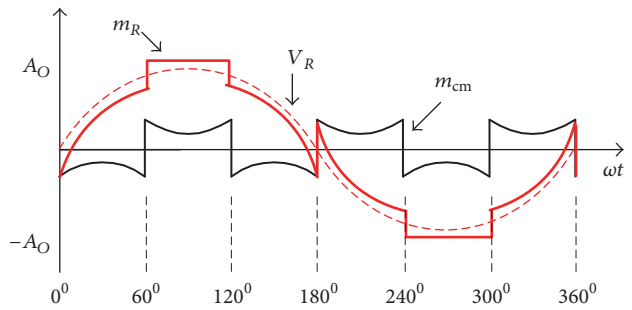

Figure 5: 60° bus-clamping modulating signal.

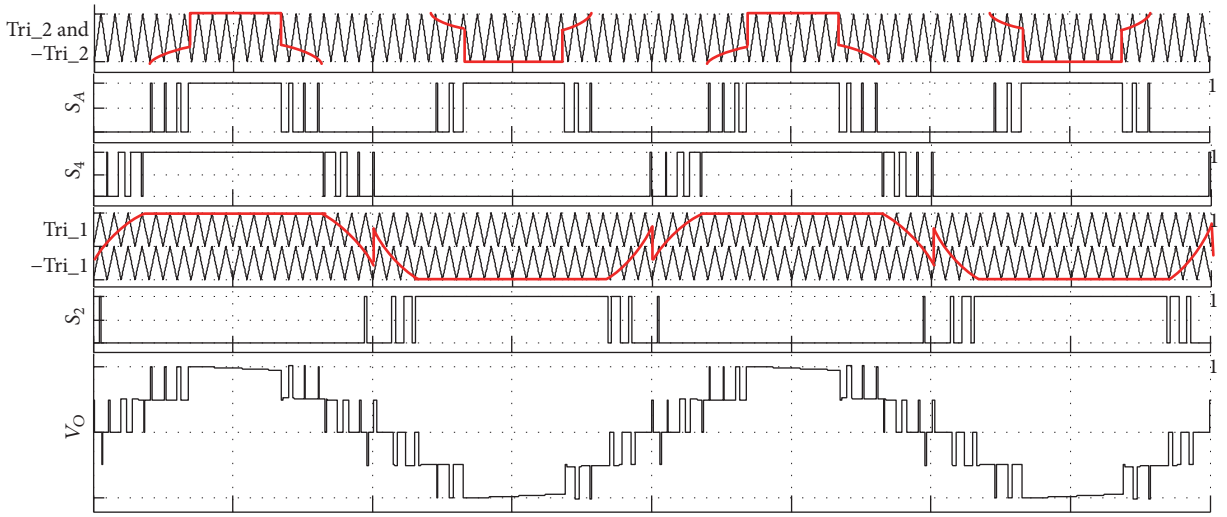

Figure 6: Reference and carrier signals required for modulation of a five-level switched-capacitor inverter.

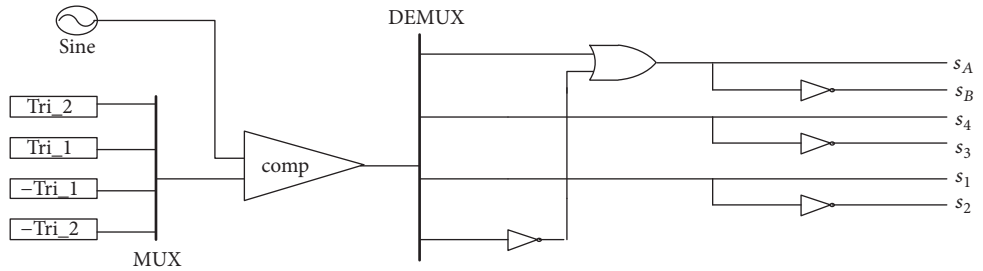

Figure 7: Control Logic circuit for driving the active switches.

60-degree clamping mode, the clamping duration is 60° for every half cycle. Therefore, nearly one-third of the switching losses of the converter are reduced in this technique. For the simulated five-level inverter, 4 triangular carriers are required. All the carriers are having the same frequency, f_C, and peak-to-peak amplitude, A_C. Modulating or reference signal, here considered, is a sine wave with the frequency, f_O, and the amplitude, A_O. As shown in Figure 6, Tri_1, Tri_2 represents the positive carriers and −Tri_1, −Tri_2 represents the negative carriers. At every instant, each carrier is compared with the reference signal. The outputs of the comparator are used to drive the corresponding switches. The control logic of the multicarrier comparison for the switching devices is shown in Figure 7.

4. Analysis of Modulation Strategy

The general form of a time-varying switched waveform of a single phase leg controlled by any PWM strategy can be written as

$$\begin{aligned} F(t) = \frac{A_{OO}}{2} &+ \sum_{n=1}^{\infty} \{A_{On}\cos(ny) + B_{On}\sin(ny)\} \\ &+ \sum_{m=1}^{\infty} \{A_{mO}\cos(mx) + B_{mO}\sin(mx)\} \\ &+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \{A_{mn}\cos(mx+ny) \\ &+ B_{mn}\sin(mx+ny)\}. \end{aligned} \tag{6}$$

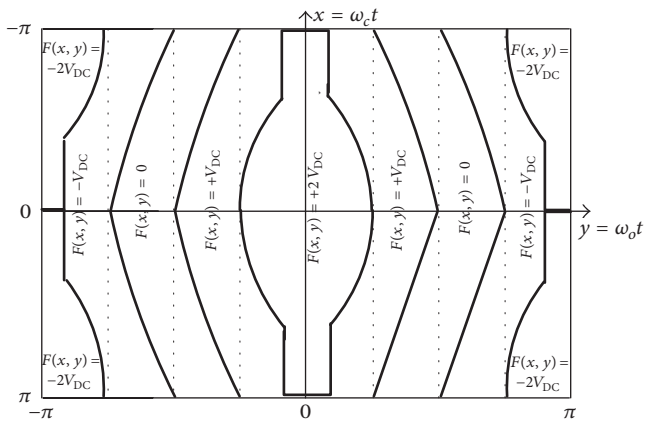

Figure 8: Contour plot of $F(x, y)$ for five-level multilevel inverter.

The first term in (6) represents the dc offset value, the second represents the fundamental and baseband harmonics, the third terms in the expression give the carrier harmonics, and the last term includes the carrier sideband harmonics, respectively [18].

The coefficients of (6) are obtained for any particular PWM strategy by evaluating the double Fourier integral form as developed by black and adapted by Bowes for power electronic converter systems:

$$A_{mn} + jB_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} F(x, y)\, e^{j(mx+ny)} dx\, dy \tag{7}$$

$$\begin{aligned} x &= \omega_C t + \theta_C; \\ y &= \omega_O t + \theta_O. \end{aligned} \tag{8}$$

The difficulty is to specify $F(x, y)$ in a time-varying form which makes (7) tractable to solve. This formulation separates the integration of the switched waveform across each carrier period from the integration of each carrier period across the whole fundamental period so that the two parts can be separately evaluated to determine the coefficients. Equation (8) has been adapted from [19] to include an arbitrary phase offset of θ_O for the reference waveform and θ_C for the carrier waveforms. To evaluate (7), the function $F(x, y)$ is compared against the reference waveform in the "y" dimension and against the carrier waveform(s) in the "x" dimension, according to the rules of the modulation strategy to be solved, to create regions in the (x, y) space within which $F(x, y)$ is constant. This is illustrated in Figure 8 for the five-level discontinuous space vector strategy.

The inner integral limits for simple naturally sampled sine-triangle modulation have been previously identified by Bowes and others as the instantaneous values of the modulating reference waveform during each carrier period [20]. Discontinuous and space vector modulation strategies present a more complex problem since they do not use a continuous modulation reference waveform. It is also straightforward to apply the sectionalized concept to modulation strategies which introduce arbitrary offsets to achieve some perceived harmonic benefit [21]. A similar approach can be used for other discontinuous PWM strategies using one of the various phase offsets that have been investigated. All that is required is to define the reference waveform in terms of sequences of sinusoidal reference waveform sections linked together to span a complete fundamental cycle.

The time-varying expressions for reference and carrier waves can be mathematically represented as follows,

Reference wave equation with frequency, ω_O, peak amplitude, A_O, and modulation index, M, can be evaluated using equations (4) and (5):

$$\begin{aligned} &\text{(i) for} \longrightarrow y \subset \left(0, \frac{\pi}{3}\right) \\ &m_{R1} = M * v_R + \left(-2A_C - M * v_Y\right) \\ &\quad = \left(M * A_O \sin(y)\right) \\ &\qquad + \left(-2A_C - \left(M * A_O \sin\left(y - \frac{2\pi}{3}\right)\right)\right) \\ &\quad = -2A_C + \sqrt{3} * M * A_O \cos\left(y - \frac{\pi}{3}\right). \end{aligned} \tag{9}$$

Similarly, we can obtain the equation of the resultant modulating signal through the following equations:

$$\begin{aligned} &\text{(ii) for} \longrightarrow y \subset \left(-\pi, \frac{-2\pi}{3}\right); \\ &m_{R2} = +2A_C + \sqrt{3} * M * A_O \cos\left(y - \frac{\pi}{3}\right) \\ &\text{(iii) for} \longrightarrow y \subset \left[\frac{-2\pi}{3}, \frac{-\pi}{3}\right]; \\ &m_{R3} = -2A_C \\ &\text{(iv) for} \longrightarrow y \subset \left(\frac{-\pi}{3}, 0\right); \\ &m_{R4} = +2A_C + \sqrt{3} * M * A_O \cos\left(y - \frac{2\pi}{3}\right) \\ &\text{(v) for} \longrightarrow y \subset \left[\frac{\pi}{3}, \frac{2\pi}{3}\right]; \\ &m_{R5} = 2A_C \\ &\text{(vi) for} \longrightarrow y \subset \left(\frac{2\pi}{3}, \pi\right); \\ &m_{R6} = -2A_C + \sqrt{3} * M * A_O \cos\left(y - \frac{2\pi}{3}\right). \end{aligned} \tag{10}$$

Equations (9) and (10) give the mathematical forms of the reference signal in the period $(-\pi, \pi)$.

Table 2: Lists the outer and inner integral limits of the six reference waveform sections.

Outer integral limits		Inner integral limits	
Lower limit	Upper limit	Lower limit	Upper limit
$-\pi$	$-\frac{2\pi}{3}$	$-\frac{\pi}{2}\left(1+\sqrt{3}*M*\cos\left(y-\frac{\pi}{3}\right)\right)$	$\frac{\pi}{2}\left(1+\sqrt{3}*M*\cos\left(y-\frac{\pi}{3}\right)\right)$
$-\frac{2\pi}{3}$	$-\frac{\pi}{3}$	0	0
$-\frac{\pi}{3}$	0	$-\frac{\pi}{2}\left(1+\sqrt{3}*M*\cos\left(y-\frac{2\pi}{3}\right)\right)$	$\frac{\pi}{2}\left(1+\sqrt{3}*M*\cos\left(y-\frac{2\pi}{3}\right)\right)$
0	$\frac{\pi}{3}$	$-\frac{\pi}{2}\left(-1+\sqrt{3}*M*\cos\left(y-\frac{\pi}{3}\right)\right)$	$\frac{\pi}{2}\left(-1+\sqrt{3}*M*\cos\left(y-\frac{\pi}{3}\right)\right)$
$\frac{\pi}{3}$	$\frac{2\pi}{3}$	0	0
$\frac{2\pi}{3}$	π	$-\frac{\pi}{2}\left(-1+\sqrt{3}*M*\cos\left(y-\frac{2\pi}{3}\right)\right)$	$\frac{\pi}{2}\left(-1+\sqrt{3}*M*\cos\left(y-\frac{2\pi}{3}\right)\right)$

Carrier wave equation with frequency, ω_C, and peak amplitude, A_C, is given by

$$\text{(i) for } \longrightarrow x \subset \left(((i-1)*2\pi), \left(\frac{(2i-1)*2\pi}{2}\right)\right] \quad (\text{Tri\_1})^{+} = 2A_C\left(\frac{x}{2\pi}-(i-1)\right) \tag{11}$$

$$\text{(ii) for } \longrightarrow x \subset \left(\left(-\frac{(2i-1)*2\pi}{2}\right), ((i-1)*2\pi)\right] \quad (\text{Tri\_1})^{-} = -2A_C\left(\frac{x}{2\pi}-(i-1)\right), \tag{12}$$

where i is a natural number.

Other carrier wave equations are given by

$$\begin{aligned}(\text{Tri\_2}) &= A_C + (\text{Tri\_1})\\ (-\text{Tri\_1}) &= -A_C + (\text{Tri\_1})\\ (-\text{Tri\_2}) &= -2*A_C + (\text{Tri}_1).\end{aligned} \tag{13}$$

Therefore, amplitude modulation index and frequency modulation index of the converter are given by the following:

$$\text{Amplitude modulation index, } M_a = A_O/2A_C$$

$$\text{Frequency modulation index, } M_f = \omega_C/\omega_O$$

The Fourier analysis for these modulation strategies is achieved by breaking the outer integral of the Fourier double integral formulation (7) into separate integrations for each section of the reference waveform, with appropriate inner integral limits for each section. In Table 2, the terms contain sinusoidal expressions, which create $e^{\pm\lambda\cos y}$ terms in the outer integrals. The evaluation of these terms is so difficult to obtain an analytical solution of PWM. These terms can be solved by using Jacobi-Anger expansion to create deterministic outer integral formulations.

$$e^{\pm\lambda\cos y} = J_0(\lambda) + 2\sum_{k=1}^{\infty} j^{\pm k} J_k(\lambda)\cos(ky). \tag{14}$$

The algebra required for the more complex PWM strategies of the state vector is fairly large and space precludes their inclusion in this paper. The mathematical conditions to obtain the solution are quite precise and must be done with utmost care to get correct harmonic components. The process of evaluation and complete closed-form solutions and verification for various naturally sampled PWM modulation waveforms have been presented in [21].

Table 3: Circuit parameters considered in simulation study.

Input voltage	100 V
Output phase voltage frequency	50 Hz
Carrier frequency	5 kHz
Circuit capacitance	4700 μF
Load (R-L)	$R = 10\,\Omega$; $L = 12$ mH

5. Results and Discussion

Switched-capacitor multilevel inverter has been simulated with the parameters mentioned in Table 3 and the following graphs and observations are noted in the analysis. The hardware in loop switched-capacitor multilevel inverter has been simulated and verified using DSP microcontroller TMS320F240. The MOSFETs utilized in the prototype are IRFP250N with inbuilt bypass diodes. The experimental prototype is given an input supply of 15 V and switching frequency of 1 kHz operating at an output phase frequency of 50 Hz with the load parameters $R = 10$ ohm and $L = 12$ mH. Figures 9–12 show the experimental results of the switched-capacitor inverter for both PD and bus-clamping techniques.

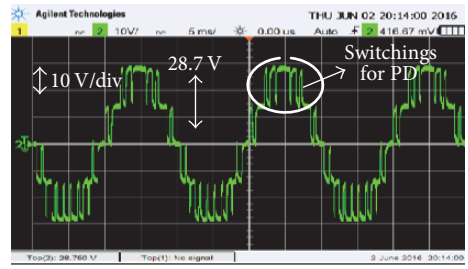

Figure 9: Output phase voltage waveform for PD modulation.

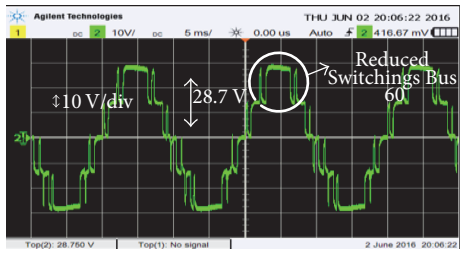

Figure 10: Output phase voltage for 60-degree bus-clamping modulation.

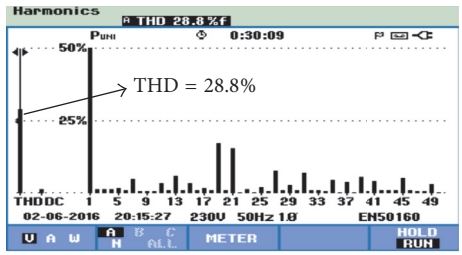

Figure 11: Output voltage THD for PD technique.

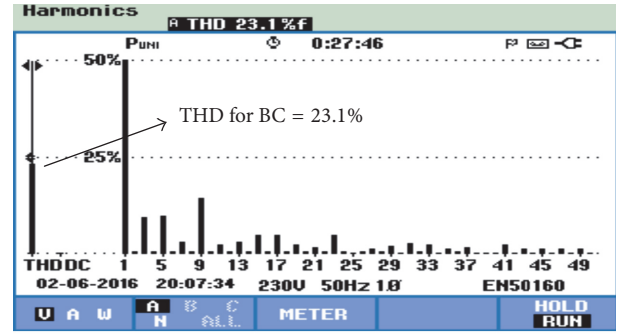

Figure 12: Output voltage THD for 60-degree bus-clamping technique.

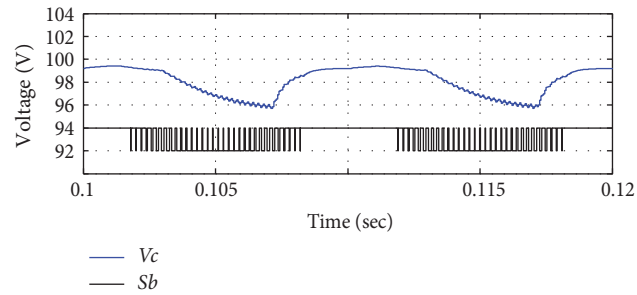

Figure 13: Voltage across the capacitor during the turning ON/OFF of switch S_b.

From the output voltage waveforms shown in Figure 9 for PD and Figure 10 for bus-clamping techniques at M.I = 0.95. It is observed that, in bus-clamping modulation, switching was disabled due to clamping of phase for a particular duration resulting in lower THD. From Figures 11 and 12, output phase voltage THD observed in 60-degree bus-clamping modulation is 23.1%, whereas it is 28.8% in PD modulation.

Figure 13 shows the capacitor voltage variation during charging and discharging process. Figure 14 shows the frequency response of the capacitor unit and suitable value of capacitance is chosen in order to limit the charging current and shows the system is stable under operation. Set of simulations were performed to observe the variation of phase voltage and line current parameters at different modulation indices. It is observed that as the modulation index increases, there is an improvement in significant percentage of THD of phase voltage and also observed that there is a gradual increment in the output fundamental voltage. From Figure 15, it is noted that all the SPWM techniques considered show almost similar performance. It can be observed that 60-degree clamp PWM with *R-L* load

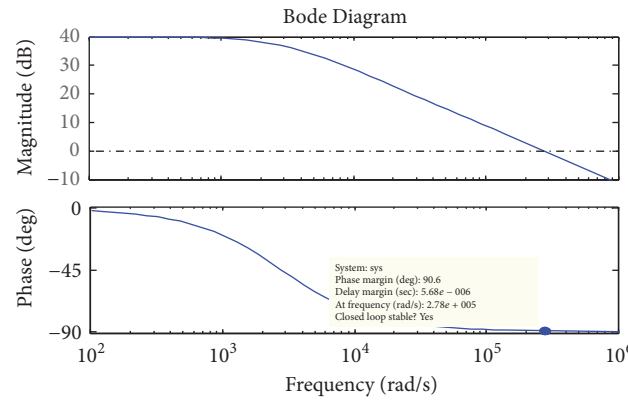

Figure 14: Frequency response of the capacitor circuit.

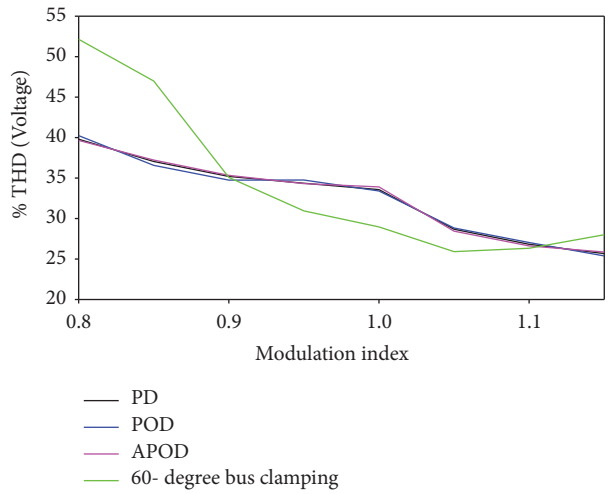

Figure 15: Harmonic distortion in output phase voltage at different modulation indices.

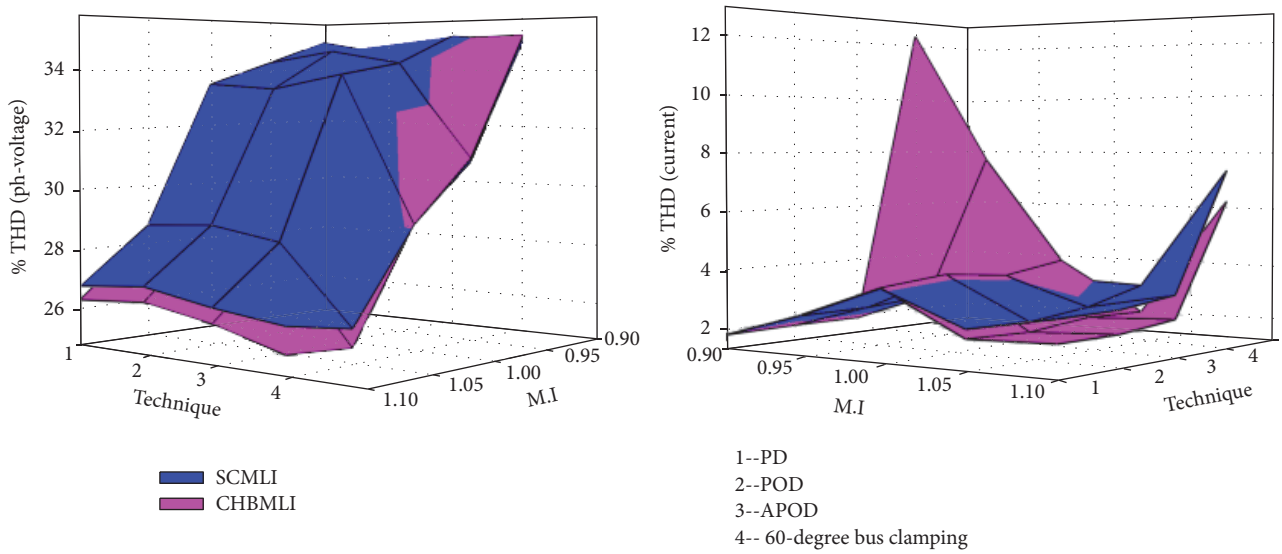

Figure 16: Comparison of harmonic distortion in SCMLI and CHBMLI at various modulation indices.

gives a best harmonic performance at modulation indices close to unity. The harmonic distortion of the output voltage and load current of switched-capacitor inverter have been compared with cascaded H-bridge multilevel inverter with the input parameters being the same and the analysis has been shown in Figure 16. From the graph, it is observed that both inverters show almost similar performance for the technique used for a given modulation index. From Figure 16, it is seen that bus clamping shows better voltage performance than the SPWM techniques at higher modulation indices. In voltage THD versus modulation index plot, bus-clamping technique results in reduced distortion in the output phase voltage waveform. In current THD versus modulation index plot, bus-clamping technique has more distortion at the modulation indices far from unity, as the modulation index approaches unity distortion gradually decreases. At unity modulation index, it is less than that of the SPWM techniques and again increases as the modulation index moves away from unity.

Switching losses in both SCMLI and CHBMLI are compared for SPWM and bus-clamping modulation methods at different modulation indexes. From Figure 17, it is inferred that, in comparison to SPWM techniques, bus-clamping modulation has reduced switching losses due to clamping of the phase to the peak value as stated in Section 3. It is nearly 30% reduction in switching losses noted for bus-clamping 60-degree modulation when compared to SPWM strategies. Whereas SCMLI topology has comparatively lower switching losses than CHBMLI, this is due to the reduced number of switching components in the topology design. In Figure 18, total conduction losses of both inverters for different techniques are presented. It is observed that, for

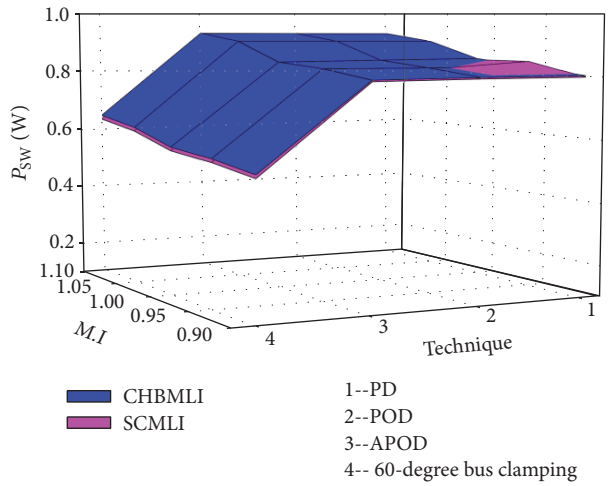

Figure 17: Switching losses comparison at various modulation indices.

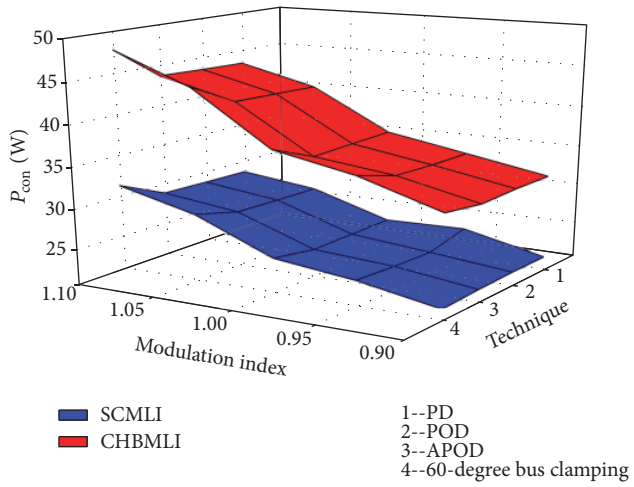

Figure 18: Conduction losses comparisons of the inverters for different techniques.

a given topology, bus-clamping strategy has slightly increased conduction losses when compared to other techniques at higher modulation indexes. This is due to high value of fundamental current at the output drawn from the source. In terms of topologies, CHBMLI has more conduction losses when compared to the SCMLI, due to the reduced number of conducting devices in SCMLI.

6. Conclusion

The analytical solution for 60-degree bus-clamping strategy has been presented for the switched-capacitor multilevel inverter. It is observed that there is around 30 percent reduction in switching losses in SCMLI with 60-degree bus clamping in comparison to SPWM techniques. This minimization results from the absence of switching in the vicinity of peaks in a given phase. An excellent trade-off between the harmonic distortion and a number of switching losses have been achieved experimentally, making the BC-PWM strategy superior to the existing regular SPWM techniques. A study on the switched-capacitor unit has been done and its performance is compared with its equivalent level conventional cascaded H-bridge inverter using DSP microcontroller TMS320F240.

Competing Interests

The authors declare that there are no competing interests regarding the publication of this paper.

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