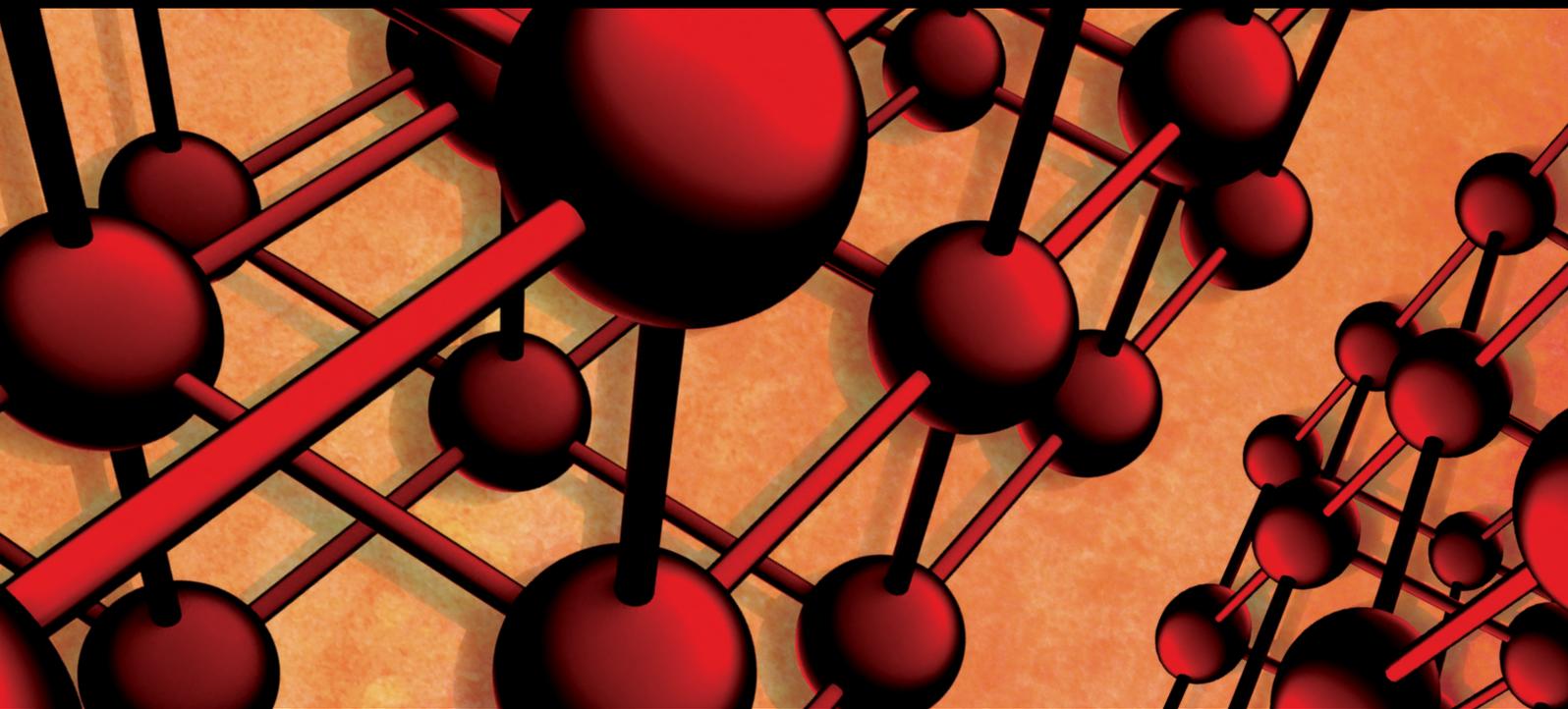


Thin Film Applications in Advanced Electron Devices

Guest Editors: Fu-Chien Chiu, Tung-Ming Pan, Tapas Kumar Kundu,
and Chun-Hsing Shih





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Advances in Materials Science and Engineering

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Editorial

Thin Film Applications in Advanced Electron Devices

Fu-Chien Chiu,¹ Tung-Ming Pan,² Tapas Kumar Kundu,³ and Chun-Hsing Shih⁴

¹ Department of Electronic Engineering, Ming Chuan University, Taoyuan 333, Taiwan

² Department of Electronic Engineering, Chang Gung University, Taoyuan 333, Taiwan

³ Department of Physics, Visva-Bharati University, West Bengal, Santiniketan 731235, India

⁴ Department of Electrical Engineering, National Chi Nan University, Nantou 545, Taiwan

Correspondence should be addressed to Fu-Chien Chiu; fcchiu@mail.mcu.edu.tw

Received 26 March 2014; Accepted 26 March 2014; Published 10 April 2014

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The application of thin films has always been a very important subject for the semiconductor industry and the scientific community. This is especially true for metal-oxide-semiconductor field effect transistor (MOSFET) technology in integrated circuits (ICs). The concept of MOSFET is based on the modulation of channel carriers by an applied gate voltage across a dielectric thin film. The electric charges in dielectrics will respond to an applied electric field through the change of dielectric polarization. The conduction current in dielectric films at normal applied electric field will be very small because their conductivities are inherently very low. However, the conduction current through the dielectric films is considerable when a relatively large electric field is applied. This considerable conduction current is owing to many different conduction mechanisms, which is crucial to the successful applications of dielectric thin films.

In general, there are two types of conduction mechanisms in dielectric films, that is, electrode-limited conduction mechanism and bulk-limited conduction mechanism [1]. The electrode-limited conduction mechanism relies on the electrical properties at the electrode-dielectric interface. Based on this type of conduction mechanism, the key physical properties are the barrier height at the electrode-dielectric interface and the effective mass of the conduction carriers in dielectric films [1]. Meanwhile, the bulk-limited conduction mechanism relies on the electrical properties of the dielectric itself. Based on the bulk-limited conduction mechanisms, some important physical parameters in the dielectric films can be obtained, such as the trap level, the trap spacing, the trap density, the carrier drift mobility, the dielectric relaxation

time, and the density of states in the conduction band [1]. One can find a review article in which the analytical methods of conduction mechanisms in dielectric films are discussed in detail [1]. Aside from the conduction mechanisms, the interface properties between silicon channel and gate dielectric are critical to the performance and reliability of MOSFETs. The methods for the characterization of electrical properties at the dielectric/Si interface can be performed by several techniques, for example, capacitance-voltage method, charge pumping method, gate-diode method, and subthreshold swing measurement [2, 3]. Based on these techniques, the surface state capture cross section at the interface between silicon and gate dielectric can be obtained. The quality of interface between silicon and dielectric film is associated with the successful applications of dielectric thin films in semiconductor industry.

Recently, the developments of next generation non-volatile memory (NVM) devices are required because the physical limitations of traditional flash memory devices are approaching [4]. A variety of thin films have been studied for the application of NVM devices. For example, BiFeO₃ film is antiferromagnetic at room temperature, and it is promising for the applications of magnetic random access memory (MRAM) and spintronic devices [5]. Moreover, lead-zirconium-titanate (PZT) film is suitable for building the ferroelectric random access memory (FRAM) because of its ferroelectricity [6]. Recently, the resistance random access memory (RRAM) device has attracted a great deal of attention for the next generation NVM applications [7]. Since the RRAM technology is well compatible with

the CMOS process, the scaling of RRAM devices may keep on in terms of the low power operation. This benefit will bring a strong cost-competitiveness to RRAM. Additionally, the advantages of RRAM include small cell size, simple cell structure, high switching speed, high operation durability, multistate switching, and three-dimensional architecture. The resistance switching behavior has been reported for a variety of materials such as binary metal oxides, solid-state electrolytes, organic compounds, amorphous Si, and perovskite-type oxides [4, 7]. All these materials mentioned above were made by thin films for the applications of advanced electron devices, for example, MRAM, FRAM, and RRAM. Recently, the applications of organic electronics were attractive due to the advantages of low cost, light weight, large-area manufacturing, and mechanical flexibility. Thus, the organic thin films were proposed and implemented for the applications of organic thin film transistors, solar cells, organic light-emitting diodes, and sensors.

In addition to the dielectric thin films used by the fabrication of advanced electron devices, the metallic thin films used by the interconnection between devices are also required to be considered. In deep-submicron CMOS technology, Cu thin film has been used as an interconnect metallization material to reduce the effect of the resistance capacitance (RC) delay because of its lower resistivity and higher electromigration (EM) resistance [8]. Aside from the interconnection application, the metallic thin films can be used in the fabrication of electron devices, such as the ferromagnetic films used in MRAM devices.

We hope that readers will realize in this special issue not only the thin film applications in advanced electron devices, but also the characterization methods for the electrical properties in thin films and their related interface, such as the interface barrier height, the carrier effective mass, the trap energy level, the trap spacing, the trap density, the dielectric relaxation time, and the density of states in the conduction band, among others.

Fu-Chien Chiu
Tung-Ming Pan
Tapas Kumar Kundu
Chun-Hsing Shih

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Research Article

Percolation of Carbon Nanoparticles in Poly(3-Hexylthiophene) Enhancing Carrier Mobility in Organic Thin Film Transistors

Chang-Hung Lee,¹ Chun-Hao Hsu,¹ Iu-Ren Chen,² Wen-Jong Wu,² and Chih-Ting Lin^{1,3}

¹ Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 10617, Taiwan

² Department of Engineering Science and Ocean Engineering, National Taiwan University, Taipei 10617, Taiwan

³ Department of Electrical Engineering, National Taiwan University, Taipei 10617, Taiwan

Correspondence should be addressed to Wen-Jong Wu; wjwu@ntu.edu.tw and Chih-Ting Lin; timlin@ntu.edu.tw

Received 3 November 2013; Revised 15 January 2014; Accepted 16 January 2014; Published 25 February 2014

Academic Editor: Chun-Hsing Shih

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To improve the field-effect mobility of all-inkjet-printed organic thin film transistors (OTFTs), a composite material consisted of carbon nanoparticles (CNPs) and poly(3-hexylthiophene) (P3HT) was reported by using homemade inkjet-printing system. These all-inkjet-printed composite OTFTs represented superior characteristics compared to the all-inkjet-printed pristine P3HT OTFTs. To investigate the enhancement mechanism of the blended materials, the percolation model was established and experimentally verified to illustrate the enhancement of the electrical properties with different blending concentrations. In addition, experimental results of OTFT contact resistances showed that both contact resistance and channel resistance were halved. At the same time, X-ray diffraction measurements, Fourier transform infrared spectra, ultraviolet-visible light, and photoluminescence spectra were also accomplished to clarify the material blending effects. Therefore, this study demonstrates the potential and guideline of carbon-based nanocomposite materials in all-inkjet-printed organic electronics.

1. Introduction

The extensive researches of organic semiconductors have attracted considerable attention due to their potential in printed and flexible electronics. Because of the advantages of organic electronics, such as low cost, light weight, large-area manufacturing, and mechanical flexibility, these researches promote applications of organic electronics. For instance, organic thin film transistors (OTFTs) [1], solar cells [2], organic light-emitting diodes [3], and sensors [4] were proposed and implemented. In spite of these promising developments, some crucial problems have blocked the path to commercialization, such as the mobility of organic semiconductor and the feasibility of manufacturing. To address manufacturing technologies, solution processes are one of the candidates. These processes include spin coating, screen printing, gravure printing, roll-to-roll printing, and inkjet printing. Among these processes, inkjet printing has advantages of mask-less deposition, etch-free fabrication, and low material consumption [1, 5].

Although the inkjet printing technique can offer many advantages in applications, the electrical properties of OTFTs still need to be improved from the aspect of materials. To enhance the effective mobility of the OTFT, commonly, the self-assembled monolayers (SAM) have been used to modify the interfacial properties between the organic semiconductor, dielectric layer, and the contact electrodes [6–8]. However, the SAM technique is not adapted for the all-inkjet-printing process, because the solvent used in SAM may easily dissolve the inkjet-printed layer. On the other hand, the O₂ plasma treatment can also improve the surface characteristics of the dielectric layer [9]. But the plasma would break the bonds at the dielectric surface which would drive the drain current unsaturated [10]. To address these issues, some researchers have directly printed blending composite materials to improve the electrical properties of OTFTs [11]. Blending carbon nanotubes (CNTs) and organic semiconductive polymer as an active layer can enhance the carrier mobility of OTFTs [12–15]. However, forming a homogenous suspension of the CNT-blended material needs additional

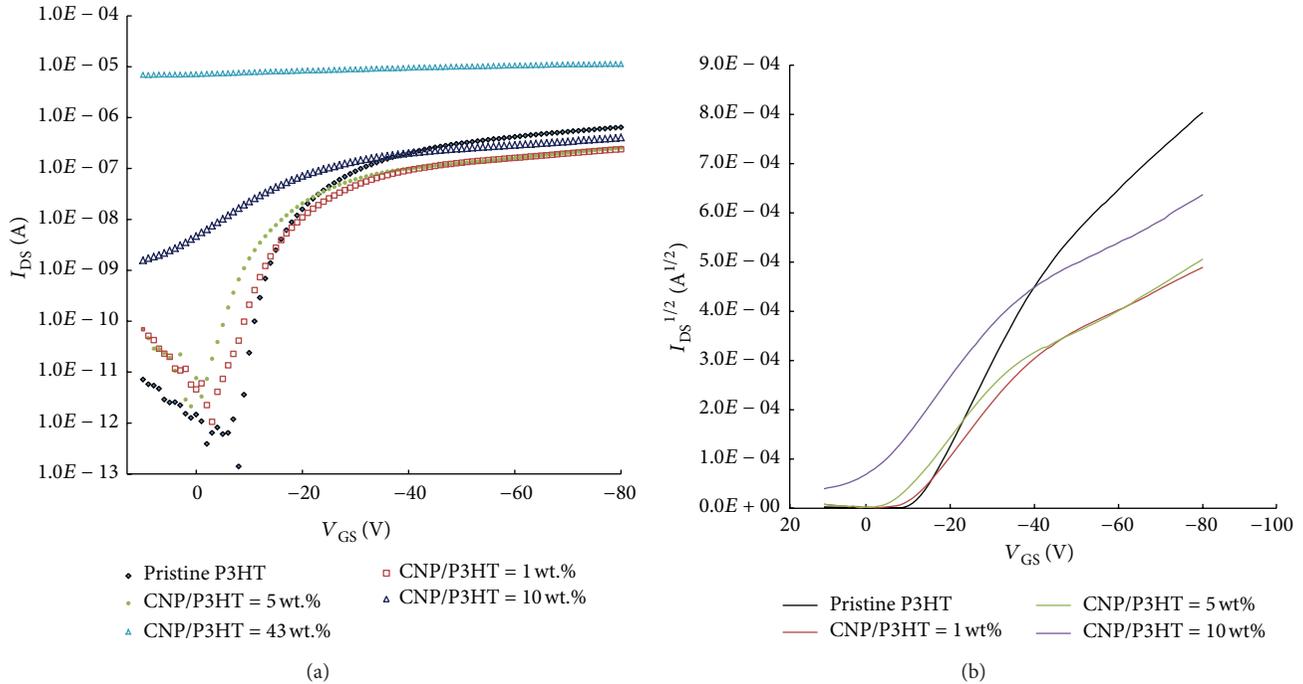


FIGURE 1: (a) V_{GS} - I_{DS} characteristics and (b) V_{GS} - $I_{DS}^{1/2}$ characteristics of all-inkjet-printed OTFTs.

treatments such as ultrasonication or functionalized CNT. Compared with the CNTs/organic semiconductor in the previous reports, carbon nanoparticles (CNPs) could be a proper choice for inkjet printing because the CNP-blended ink has higher uniformity than CNT-blended ink does.

In this study, the OTFTs based on composite organic materials, that is, poly(3-hexylthiophene) (P3HT) blended with CNP, were fabricated to study the mobility enhancement phenomenon. In addition, a series of material analyses were accomplished to verify its characteristics. For instance, X-ray diffraction (XRD) measurements were used to study the crystalline ordering in the composite film; Fourier transform infrared (FTIR) spectra were used to confirm the bonding formation between the CNP and P3HT; ultraviolet-visible light (UV-Vis) and photoluminescence (PL) spectra were conducted to explore the formation of the charge-transfer complexes (CTC). The contact resistance measurements are achieved to explore the interfaces between the electrodes and the active layer, further to study the carrier injection barrier. Based on the above analysis and the local electric field enhancement model [13, 16, 17], the percolation theory interpreted the electrical properties of the OTFTs at the different blended CNP concentrations.

2. Materials and Methods

The all-inkjet-printed OTFTs were fabricated by using a homemade inkjet printing system. The fabricated OTFTs was bottom-gate, bottom-contact structure. We used 0.3 wt.% P3HT (Uni-Onward Corp., Taiwan), dissolved in p-xylene, as an organic semiconductor. The P3HT solution was blended with various concentrations of CNPs (Qf-Nano Tech. Co.

Ltd., Taiwan, model: QF-PHG-1P) including 1 wt.%, 5 wt.%, 10 wt.%, and 43 wt.% with respect to P3HT. The manufacturing process of the OTFTs is shown in detail in previous report [18]. In this study, the channel length and width are typically $20 \mu\text{m}$ and $400 \mu\text{m}$, respectively. However, to verify the contact resistance of OTFTs, a series of transistors was made in different channel lengths (20 , 60 , and $100 \mu\text{m}$), and the channel width was expanded to $800 \mu\text{m}$. The electrical properties of the fabricated OTFTs were measured by using Agilent 4156C in a dark environment with humidity controlled (relative humidity $<25\%$) in atmosphere.

To identify the material properties of the blended semiconductors, the fabricated OTFTs were analyzed by a series of methods. The solid-state UV-Vis absorption spectra were determined by using Jasco V-570 UV/V-s/NIR spectrophotometer. The PL spectra were obtained by using Jasco FP-6300 with an excitation wavelength of 453 nm . The FTIR transmittance spectra were derived by using Thermo Nicolet NEXUS470. The XRD were recorded by using PANalytical, X'Pert PRO. The field emission scanning electron microscope (SEM) images were performed by using JOEL JSM-6700F.

3. Results and Discussion

Figure 1 shows the transfer characteristics of the all-inkjet-printed OTFTs with various CNP concentrations. The threshold voltages (V_T) of the OTFTs were obtained from the plot of the V_{GS} - $I_{DS}^{1/2}$ at saturation region by extrapolating the fitting line and locating the x -intercept, as shown in Figure 1(b). However, the switching behavior of the transistor degenerated, while 43 wt.% CNP blended, as shown in Figure 1(a).

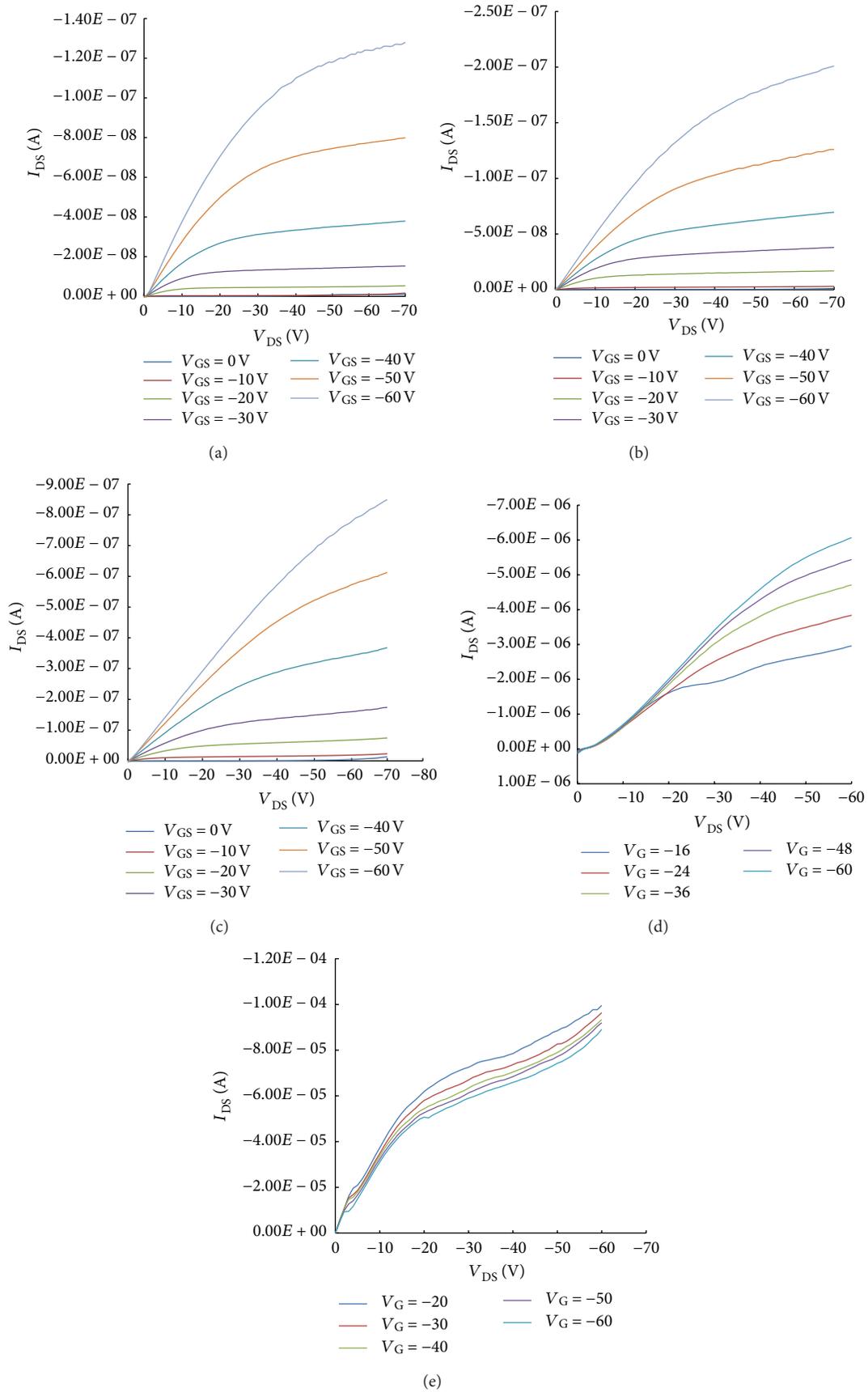


FIGURE 2: Output characteristics for (a) pristine P3HT, (b) CNP/P3HT = 1 wt.%, (c) CNP/P3HT = 5 wt.%, (d) CNP/P3HT = 10 wt.%, and (e) CNP/P3HT = 43 wt.% OTFTs.

Because the CNP dominated the channel conductance, the V_T of OTFT with 43 wt.% CNP could not be defined.

To obtain the field-effect mobility, the output characteristics of the OTFTs are shown in Figure 2. Three kinds of methods were approached to calculate the average field-effect mobility accurately for different OTFTs. Because the OTFTs blended with 0 wt.%, 1 wt.%, and 5 wt.% CNP exhibited saturation behavior (as shown in Figures 2(a)–2(c)), the field-effect mobility of such OTFTs was calculated in saturation region ($V_{DS} = -70$ V) by plotting the $V_{GS}-I_{DS}^{1/2}$ and fitting the data to the equation [12, 14]

$$\mu = \frac{2L}{WC_i} \left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}} \right)^2, \quad (1)$$

where the capacitance $C_i = 11.0 \times 10^{-9}$ F cm⁻². The OTFT with 10 wt.% CNP did not present saturation behavior (as shown in Figure 2(d)) but was still modulated by the gate bias. Consequently, the average field-effect mobility was estimated in linear region ($V_{DS} = -60$ V) by using the equation [19]

$$\mu = \frac{L}{WC_i V_{DS}} \frac{\partial I_{DS}}{\partial V_{GS}}. \quad (2)$$

As shown in Figure 2(e), at the same time, the OTFT with 43 wt.% CNP had neither saturation behavior nor gate-modulation effect. First, the conductivity was derived from the channel length and cross-sectional area ($A = W \times t$) by

$$\sigma = \frac{I_{DS}}{V_{DS}} \frac{L}{A}, \quad (3)$$

where the thickness $t = 100$ nm. Then the mobility could be estimated by [20]

$$\mu = \frac{\sigma}{ep}. \quad (4)$$

The electrical properties of the OTFTs including mobility, on/off ratio, and V_T are summarized in Table 1. The effective mobility (μ_{eff}) of OTFT ranges from around 10^{-4} to 10^{-2} cm²/V-s, which is comparable to those of inkjet-printed P3HT OTFTs reported previously [11, 21]. The μ_{eff} can be modeled by using percolation theory as described by the following equation [22, 23]:

$$\mu_{\text{eff}} = \mu_{\text{pristine-P3HT}} + \frac{\mu_{\text{blend-max}}}{1 + \exp((p_C - p)/C)}, \quad (5)$$

where the $\mu_{\text{pristine-P3HT}}$ was the intrinsic mobility of pristine P3HT; the maximum mobility ($\mu_{\text{blend-max}}$) was obtained from the OTFT with highest CNP blending concentration (i.e., 43 wt.%); p is the blending concentration of CNP; the p_C is percolation threshold; and C is a fitting parameter. After fitting the effective mobility to (5), the following parameters were extracted: $p_C = 7.5$ wt.% and $C = 1$ wt.%. The fitting result is plotted in Figure 3. When the concentration $p < p_C$, CNPs would induce a local electric field, which would let the P3HT near CNPs experience electric field larger than the applied gate bias. As a consequence, the carrier density

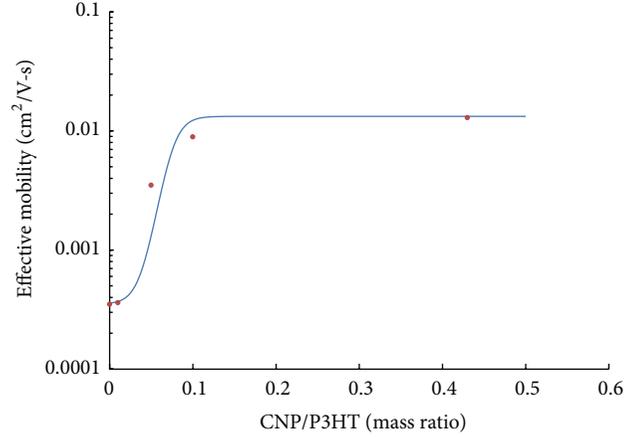


FIGURE 3: Percolation model for simulation and experimental data.

of P3HT can be increased [13] and the effective mobility of the OTFTs was also increased. When the CNP concentration is near or equal to the p_C , the percolation path is gradually formed, which is caused by the aggregation of CNPs. While the CNP concentration is above the p_C , the charge carrier would travel directly through the percolation path, and the CNPs will dominate the conductivity. It should be noted that the local electric field, which was induced by CNP, would also affect the threshold voltage of OTFTs. The threshold voltage was shifted from -12.5 V (pristine P3HT) to 3 V (CNP/P3HT = 10 wt.%), which increased with the CNP concentration. The similar phenomena and the field enhancement factor have also been reported [16, 17].

To investigate the mechanism of the improved performance, the contact resistance between the P3HT and the electrodes, poly(3,4-ethylenedioxythiophene)/poly(styrenesulfonate) (PEDOT:PSS), was studied. In order to exam the electronic properties at the interface, the OTFTs were operated in linear region ($V_{DS} \ll V_{GT}$; $V_{DS} = -0.1$ V; $V_{GT} = V_{GS} - V_T = -5, -15, -25, -35, -45, \text{ and } -55$ V) with different channel lengths ($L = 20, 60, \text{ and } 100$ μm) and constant channel width ($W = 800$ μm). Figure 4 shows the on-resistance (R_{on}) as a function of channel length at fixed V_{GT} for pristine P3HT and CNP-blended OTFT. The R_{on} can be represented by $R_{\text{on}} = R_{\text{ch}} + R_{\text{C}}$, where R_{ch} represents the channel resistance and R_{C} symbolizes the contact resistance. The contact resistance and channel resistance of OTFT with $L = 20$ μm are summarized in Table 2. Figure 4 also shows that incorporating CNPs with P3HT reduced the contact resistance and channel resistance by an average factor of two. These results suggested that incorporating CNPs could modulate the hole-injection barrier between the PEDOT and P3HT, which could reduce the contact resistance and result in a higher effective carrier injection [14, 24].

The morphology of the CNP/P3HT nanocomposites was observed by an optical microscope and SEM. Figure 5(a) shows the optical images in the channel region of OTFTs with 0 wt.% CNP, 1 wt.% CNP, 5 wt.% CNP, and 10 wt.% CNP. These images indicated that the CNPs aggregated when the concentration of CNP increased. For the detailed dispersion

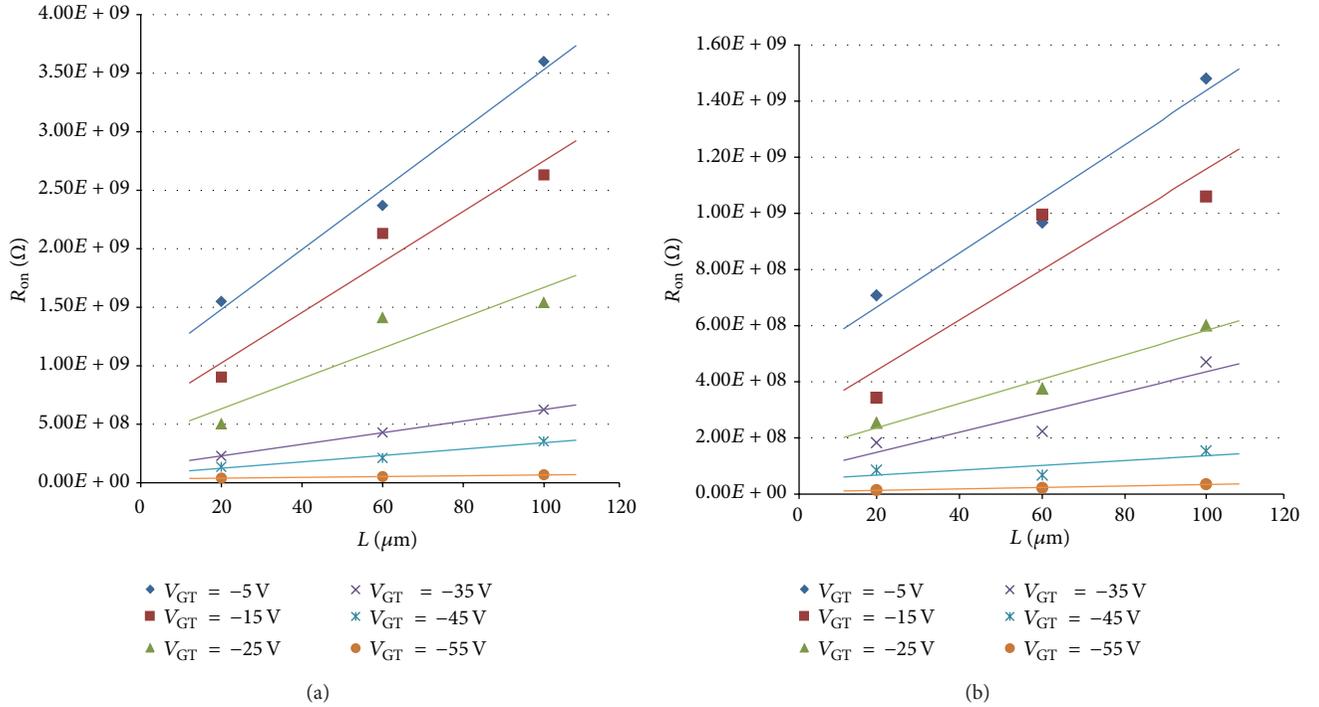


FIGURE 4: On resistance (R_{on}) measurement as a function of channel length with various V_{GT} for (a) pristine P3HT and (b) CNP/P3HT = 5 wt.% OTFTs.

TABLE 1: Electrical properties of fabricated OTFTs.

Blending concentration	Pristine P3HT	CNP/P3HT = 1 wt. %	CNP/P3HT = 5 wt. %	CNP/P3HT = 10 wt. %	CNP/P3HT = 43 wt. %
On/off ratio	3.67×10^5	2.26×10^5	1.20×10^5	4.13×10^2	2.1
V_T (V)	-12.5	-10	-7.5	3	n/a
μ ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	0.00035	0.00036	0.0035	0.0089	0.0123

of the CNP/P3HT nanocomposite, the SEM images with various concentrations were performed in Figures 5(b)–5(f). As aforementioned, CNP improved the injection barrier and enhance the field-effect mobility at low blending ratio. When the blending concentration reaches a critical value, however, the CNPs form a percolation path, and the excess localized aggregations increase the off-current. As a consequence, the fabricated OTFT is turned into a resistor-like device and it might be further dominated by the electrical properties of CNPs. Based on the observations from Table 2 and Figure 5, small groups of CNP would aggregate, but the percolation path would not be connected when CNP/P3HT < 10 wt.%. When the CNPs concentration was up to 10 wt.%, some localized aggregations started to connect to each other. While CNP/P3HT = 43 wt.%, most of CNPs were aggregated and the electrical properties of OTFT were dominated by CNPs. In other words, the drain current of fabricated OTFT devices was not modulated by the gate bias.

Previous investigations in XRD spectra show the intensity of the (100) reflection, which is caused by the lamellar layer structure, reduced with the increasing amount of CNP [18]. This result indicated that adding CNP into P3HT will disturb the crystal ordering of the organic semiconductor. In general,

the decreasing of crystal ordering suppresses the carrier transportation. However, adding CNP into P3HT improved the field-effect mobility of OTFT. To further explore the reason of this mobility enhancement, other analyses were executed.

The functional groups were identified by the absorption band of the FTIR spectra for P3HT and CNP/P3HT nanocomposite, as shown in Figure 6. The band at 721 cm^{-1} is associated with the methyl rock of P3HT. The peak at 819 cm^{-1} is contributed by the aromatic C–H, out-of-plane. The band at 1377 cm^{-1} is assigned to methyl deformation. The band at 1457 cm^{-1} is assigned to the symmetric C–C stretching mode, and the 1509 cm^{-1} is assigned the antisymmetric C=C stretching mode. We could mark the variation of the average conjugation length of P3HT from the ratio between the intensity at 1509 cm^{-1} and 1457 cm^{-1} [25, 26]. If the relative intensity increases at 1509 cm^{-1} , the average conjugation length will increase. From Figure 6, the intensity ratio is kept the same, so the average conjugation length of P3HT backbones did not change after adding CNPs, which means that the molecule structure of P3HT is maintained. Consequently, no new bonding was observed between CNPs and P3HT.

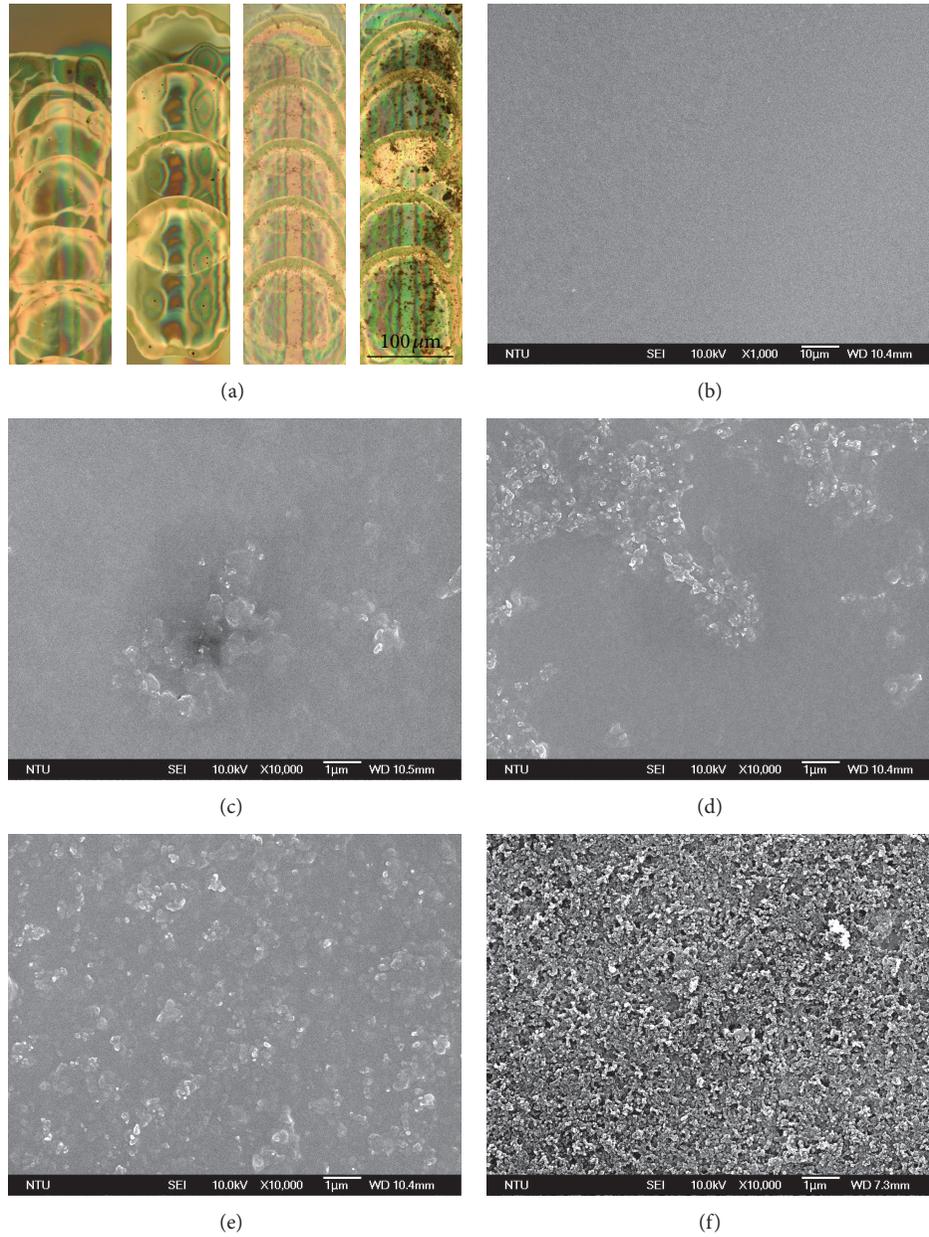


FIGURE 5: (a) Microscope images of channel region, from left to right, the CNP/P3HT, are 0 wt.%, 1 wt.%, 5 wt.%, and 10 wt.%, respectively. SEM images for (b) pristine P3HT, (c) CNP/P3HT = 1 wt.%, (d) CNP/P3HT = 5 wt.%, (e) CNP/P3HT = 10 wt.%, and (f) CNP/P3HT = 43 wt.%.

TABLE 2: Contact resistance and channel resistance analysis.

R_C (Ω)	$V_{GT} = -5$ V	$V_{GT} = -15$ V	$V_{GT} = -25$ V	$V_{GT} = -35$ V	$V_{GT} = -45$ V	$V_{GT} = -55$ V
P3HT	1.00×10^9	5.00×10^8	2.50×10^8	1.25×10^8	7.50×10^7	2.50×10^7
CNP/P3HT (5 wt.%)	5.00×10^8	2.50×10^8	1.50×10^8	7.50×10^7	5.00×10^7	7.50×10^6
R_{ch} (Ω), ($L = 20$ μ m)	$V_{GT} = -5$ V	$V_{GT} = -15$ V	$V_{GT} = -25$ V	$V_{GT} = -35$ V	$V_{GT} = -45$ V	$V_{GT} = -55$ V
P3HT	5.53×10^8	4.03×10^8	2.53×10^8	1.04×10^8	6.03×10^7	1.50×10^7
CNP/P3HT (5 wt.%)	2.08×10^8	2.00×10^8	1.03×10^8	5.00×10^7	3.50×10^7	6.43×10^6

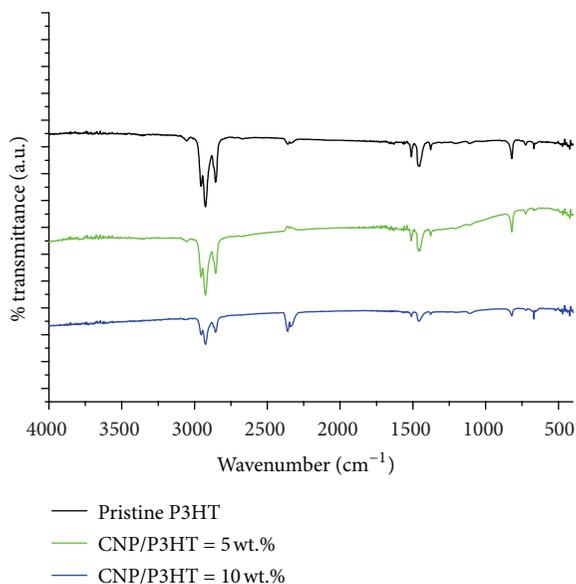


FIGURE 6: FTIR spectra of pristine P3HT, CNP/P3HT = 5 wt.%, and CNP/P3HT = 10 wt.% thin films.

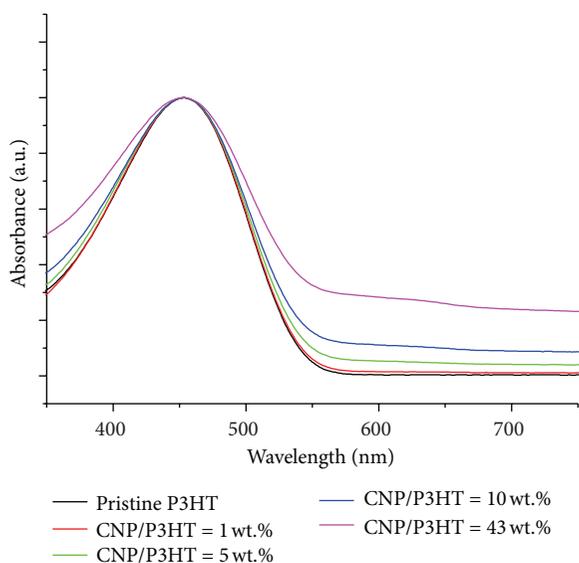


FIGURE 7: UV-Vis spectra of pristine P3HT, CNP/P3HT = 1 wt.%, 5 wt.%, 10 wt.%, and 43 wt.%.

To study interactions among the P3HT chains in the CNP/P3HT, furthermore, the UV-Vis spectra of P3HT and CNP/P3HT nanocomposites are shown in Figure 7. The absorption peak which located at 453 nm represented to the electron transition from the highest occupied molecular orbital (HOMO) to the lowest unoccupied molecular orbital (LUMO) of the P3HT [27, 28]. Geng et al. reported that the π electrons of the blended CNTs would interact with the conjugated polymers, which represent as the UV-Vis absorption peaks broadening [29]. The similar phenomenon could be observed in the spectra of CNP/P3HT. Figure 7 shows that the main absorption peak was broadened with the increasing

amount of CNPs because of the π - π interaction between the conjugated chain of the P3HT and the π orbital of CNPs.

The LUMO-HOMO relaxation could be observed from the maximum emission peak (λ_{\max}) of the PL spectra [29], as shown in Figure 8. The spectra mark the λ_{\max} at 589, 586, 572, and 566 nm for 0 wt.%, 1 wt.%, 5 wt.%, and 10 wt.% CNP/P3HT, respectively. The main emission peak appeared small blueshift with the increasing concentration of the blended CNP. This is because the ground state energy of the composite material was lower than that of P3HT. This difference results in the increase of the energy gap of relaxation [30, 31]. Another phenomenon that could be observed from the PL spectra is quenching effect. The PL quenching revealed that the CNPs may offer another decaying path which competing with the radiative relaxation and the quenching effect became more obvious with the CNPs concentration increased [30]. Both the blue shift and quenching effects illustrated that the charge transfers appeared from the LUMO of P3HT to CNPs [29–32]. Consequently, the CTC state formed in the CNP/P3HT composites and the energy level of the CTC state was between the work function of CNP and the HOMO of P3HT [33, 34].

According to the experiments shown in this paper, the blending CNP/P3HT would not modify the molecular structures of P3HT or CNPs, either adjust the intrinsic mobility of P3HT or CNPs. Therefore, three reasons for effective mobility enhancement by incorporating CNP/P3HT nanocomposites could be concluded: (1) local electric field enhancement resulted from the CNPs that will induce higher carrier density of P3HT, (2) adding CNPs in P3HT matrix would reduce the carrier injection barrier and improve the injection efficiency, and (3) the formation of the CTC would enhance the carrier transportation between CNPs and P3HT.

The band diagrams of CNP/P3HT illustrate the effect of the local electric field, as shown in Figure 9. When the negative gate bias is applied, p-type organic semiconductor will be operated in accumulation mode, as shown in Figure 9(b). The addition of CNPs will induce local electric field to drive the P3HT near CNPs experience larger gate bias than that of external applied. Therefore, the P3HT will induce more carriers and further increase the effective mobility. Second, the work functions are 5.2–5.3, 5.13, and 4.9 eV, respectively, for PEDOT, CNP, and P3HT [35–38]. Adding CNPs into P3HT matrix can reduce the injection barrier which was verified by contact resistance measurement. Third, according to the material analyses in this study, we proposed that the formation of CTC at the interface between P3HT and CNPs could assist the carrier transportation in the channel region to enhance the effective mobility.

4. Conclusion

Adding CNPs in P3HT matrix enhanced the effective mobility by a factor of 10. The improvement of the contact resistance resulted from the injection barrier decreased at the interface between PEDOT and P3HT by cooperating CNPs into P3HT matrix. On the other hand, the improvement of the channel resistance is caused by the formation of CTC. According to the percolation model, local electric field is enhanced, while

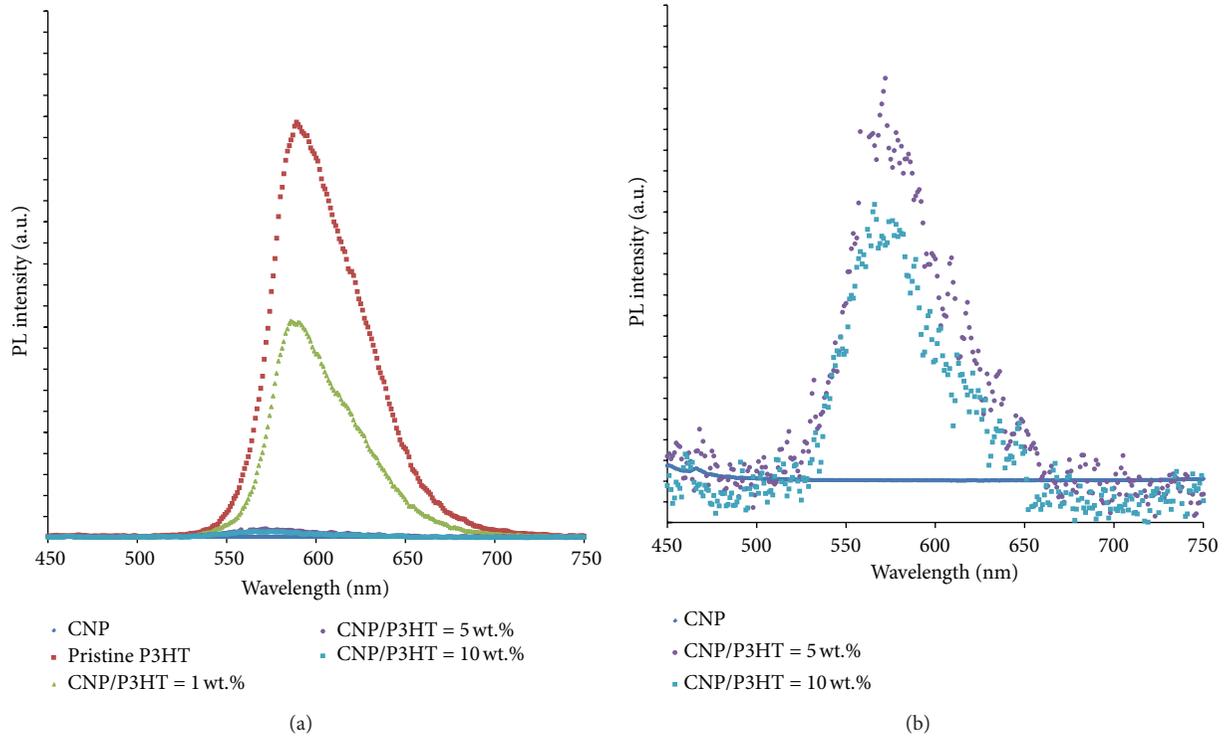


FIGURE 8: Photoluminescence spectra of CNPs, pristine P3HT, CNP/P3HT = 1 wt.%, 5 wt.%, and 10 wt.%.

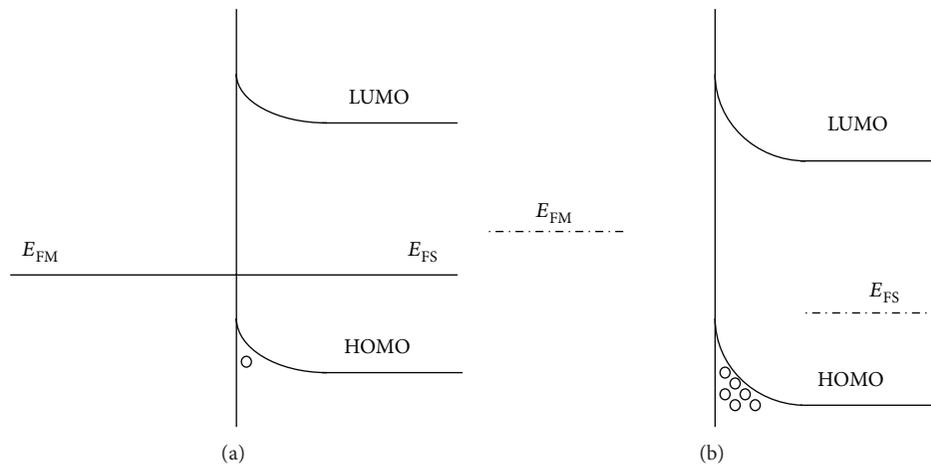


FIGURE 9: Energy band diagrams for (a) equilibrium condition with $V_{GS} = 0$ V and (b) accumulation mode with $V_{GS} < 0$ V.

the blending concentration is less than the threshold concentration. This enhancement can induce more carriers of P3HT near CNPs to increase the effective mobility. If CNP concentration is near p_C , the percolation path is gradually formed. The local field enhancement will gradually diminish due to the CNPs aggregation. After the percolation path formed, charge will transport directly through the path. The percolation paths formed from the considerable aggregations of CNPs will dominate the electrical properties and degrade transistor characteristics of the OTFT. In this work, the basis of CNP/P3HT blended system has been analyzed for further applications in OTFT.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

This work is supported by National Science Council (NSC 101-2628-E-002-022-MY3 and NSC 101-2911-I-002-001) and Intel-NTU Connected Context Computing Center (NTU102R7501).

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Review Article

A Review on Conduction Mechanisms in Dielectric Films

Fu-Chien Chiu

Department of Electronic Engineering, Ming Chuan University, Taoyuan 333, Taiwan

Correspondence should be addressed to Fu-Chien Chiu; fcchiu@mail.mcu.edu.tw

Received 29 August 2013; Revised 5 December 2013; Accepted 11 December 2013; Published 18 February 2014

Academic Editor: Chun-Hsing Shih

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The conduction mechanisms in dielectric films are crucial to the successful applications of dielectric materials. There are two types of conduction mechanisms in dielectric films, that is, electrode-limited conduction mechanism and bulk-limited conduction mechanism. The electrode-limited conduction mechanism depends on the electrical properties at the electrode-dielectric interface. Based on this type of conduction mechanism, the physical properties of the barrier height at the electrode-dielectric interface and the effective mass of the conduction carriers in dielectric films can be extracted. The bulk-limited conduction mechanism depends on the electrical properties of the dielectric itself. According to the analyses of bulk-limited conduction mechanisms, several important physical parameters in the dielectric films can be obtained, including the trap level, the trap spacing, the trap density, the carrier drift mobility, the dielectric relaxation time, and the density of states in the conduction band. In this paper, the analytical methods of conduction mechanisms in dielectric films are discussed in detail.

1. Introduction

The application of dielectric films has always been a very important subject for the semiconductor industry and the scientific community. This is especially true for metal-oxide-semiconductor field effect transistor (MOSFET) technology in integrated circuits (ICs). The concept of MOSFET is based on the modulation of channel carriers by an applied gate voltage across a thin dielectric. Dielectric is a material in which the electrons are very tightly bonded. The electric charges in dielectrics will respond to an applied electric field through the change of dielectric polarization. Dielectric materials are nearly insulators in which the electrical conductivity is very low and the energy band gap is large. In general, the value of energy band gap of insulators is set to be larger than 3 eV or 5 eV. Although not all dielectrics are insulators, all insulators are typical dielectrics. At 0 K, the valence band is completely filled and the conduction band is completely empty. Thus, there is no carrier for electrical conduction. When the temperature is larger than 0 K, there will be some electrons thermally excited from the valence band and also from the donor impurity level to the conduction band. These electrons will contribute to the current transport of the dielectric material. Similarly, holes will be generated by acceptor impurities

and vacancies will be left by excited electrons in the valence band. The conduction current of insulators at normal applied electric field will be very small because their conductivities are inherently low, on the order of $10^{-20} \sim 10^{-8} \Omega^{-1} \text{cm}^{-1}$. However, the conduction current through the dielectric film is noticeable when a relatively large electric field is applied. These noticeable conduction currents are owing to many different conduction mechanisms, which is critical to the applications of the dielectric films. For example, the gate dielectric of MOSFETs, the capacitor dielectric of dynamic random access memories, and the tunneling dielectric of Flash memories are of top importance to the IC applications. In these cases, the conduction current must be lower than a certain level to meet the specific reliability criteria under normal operation of the devices. Consequently, the study of the various conduction mechanisms through dielectric films is of great importance to the success of the integrated circuits.

To measure the conduction current through the dielectric film, one must prepare some kind of sample devices for testing. In general, there are two types of device structures used in sample testing. One is metal-insulator-metal structure which is called the MIM capacitor or the MIM diode. The considered issue in MIM capacitors is the possible asymmetry of the electrical properties when the top and bottom electrodes

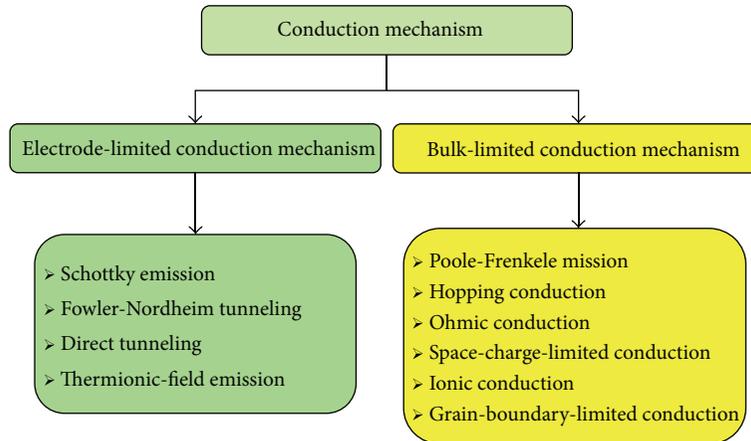


FIGURE 1: Classification of conduction mechanisms in dielectric films.

are made of different metals. Different metals generally lead to different work functions, and therefore result in different metal-dielectric interface barriers. The main parameters in this type of measurement are the barrier height of the metal-dielectric interface and the effective mass of the conduction carriers. The second type used to characterize a dielectric film is the metal-insulator-semiconductor (MIS) capacitor. Since MIS capacitor is the most useful device in the study of semiconductor surfaces, it is of interest to characterize the electrical properties of the device. However, the structure of the MIS capacitor is inherently asymmetric and one should be careful about the voltage drop across each layer. If the MIS capacitor can be biased in such a way that the semiconductor surface is in accumulation, the voltage drop across the semiconductor is minimal and most of the voltage will be applied across the dielectric film. If the semiconductor surface is in depletion or inversion, some voltage drop across the semiconductor will take place and then the voltage drop needs to be considered in calculation of the electric field across the dielectric film.

Among the conduction mechanisms being investigated, some depend on the electrical properties at the electrode-dielectric contact. These conduction mechanisms are called electrode-limited conduction mechanisms or injection-limited conduction mechanisms. There are other conduction mechanisms which depend only on the properties of the dielectric itself. These conduction mechanisms are called bulk-limited conduction mechanisms or transport-limited conduction mechanisms [1–10]. The methods to distinguish these conduction mechanisms are essential because there are a number of conduction mechanisms that may all contribute to the conduction current through the dielectric film at the same time. Since several conduction mechanisms depend on the temperature in different ways, measuring the temperature dependent conduction currents may afford us a helpful way to know the constitution of the conduction currents. The electrode-limited conduction mechanisms include (1) Schottky or thermionic emission (2) Fowler-Nordheim

tunneling, (3) direct tunneling, and (4) thermionic-field emission. The bulk-limited conduction mechanisms include (1) Poole-Frenkel emission, (2) hopping conduction, (3) ohmic conduction, (4) space-charge-limited conduction, (5) ionic conduction, and (6) grain-boundary-limited conduction. Figure 1 shows the classification of conduction mechanisms in dielectric films.

2. Electrode-Limited Conduction Mechanisms

The electrode-limited conduction mechanisms depend on the electrical properties at the electrode-dielectric contact. The most important parameter in this type of conduction mechanism is the barrier height at the electrode-dielectric interface. The electrode-limited conduction mechanisms include (1) Schottky or thermionic emission, (2) Fowler-Nordheim tunneling, (3) direct tunneling, and (4) thermionic-field emission. The current due to thermionic emission is highly dependent on the temperature, whereas the tunneling current is nearly temperature independent. Aside from the barrier height at the electrode-dielectric interface, the effective mass of the conduction carriers in dielectric films is also a key factor in the electrode-limited conduction mechanisms.

2.1. Schottky or Thermionic Emission. Schottky emission is a conduction mechanism that if the electrons can obtain enough energy provided by thermal activation, the electrons in the metal will overcome the energy barrier at the metal-dielectric interface to go to the dielectric. Figure 2 shows the MIS energy band diagram when the metal electrode is under negative bias with respect to the dielectric and the semiconductor substrate. The energy barrier height at the metal-dielectric interface may be lowered by the image force. The barrier-lowering effect due to the image force is called Schottky effect. Such a conduction mechanism due to electron emission from the metal to the dielectric is called thermionic emission or Schottky emission. Thermionic emission is one of

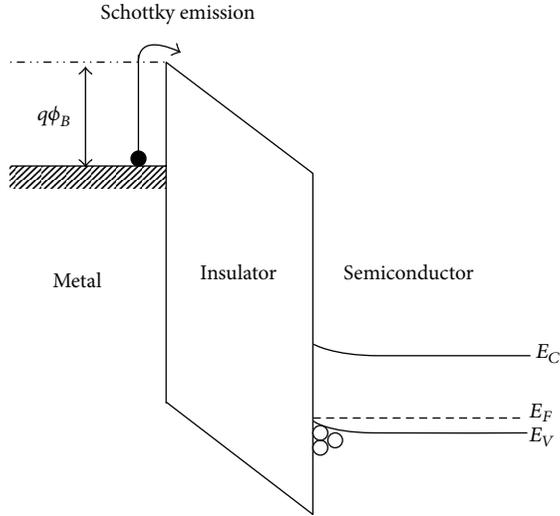


FIGURE 2: Schematic energy band diagram of Schottky emission in metal-insulator-semiconductor structure.

the most often observed conduction mechanism in dielectric films, especially at relatively high temperature. The expression of Schottky emission is

$$J = A^* T^2 \exp \left[\frac{-q(\phi_B - \sqrt{qE/4\pi\epsilon_r\epsilon_0})}{kT} \right], \quad (1)$$

$$A^* = \frac{4\pi q k^2 m^*}{h^3} = \frac{120 m^*}{m_0},$$

where J is the current density, A^* is the effective Richardson constant, m_0 is the free electron mass, m^* is the effective electron mass in dielectric, T is the absolute temperature, q is the electronic charge, $q\phi_B$ is the Schottky barrier height (i.e., conduction band offset), E is the electric field across the dielectric, k is the Boltzmann's constant, h is the Planck's constant, ϵ_0 is the permittivity in vacuum, and ϵ_r is the optical dielectric constant (i.e., the dynamic dielectric constant). In view of the classical relation between dielectric and optical coefficients, the dynamic dielectric constant should be close to the square of the optical refractive index (i.e., $\epsilon_r = n^2$) [11]. It is worthy of note that the dielectric constant is generally a function of frequency, why the optical dielectric constant is used in this case. During the emission process, if the electron transit time from the metal-dielectric interface to the barrier maximum position is shorter than the dielectric relaxation time, the dielectric does not have enough time to be polarized; consequently, the dielectric constant at high frequency or optical dielectric constant should be chosen. This optical dielectric constant is smaller than the static dielectric constant or the value at low frequency where more polarization mechanisms can contribute to the total polarization [10].

Figure 3 shows the current density-electric field (J - E) characteristics of Al/CeO₂/ p -Si MIS capacitors biased in

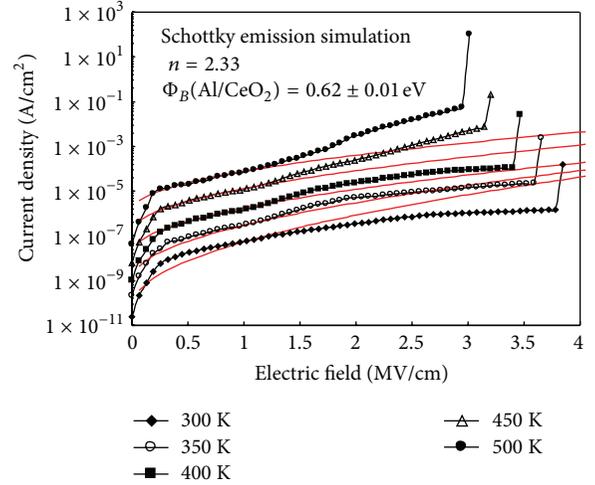


FIGURE 3: Experimental J - E curves (symbols) and simulation of Schottky emission (lines) for the Al/CeO₂/ p -Si MIS capacitor.

accumulation mode at temperatures ranging from 300 K to 500 K. According to the optical characterization of CeO₂ films, the refractive index (n) at 632.8 nm is about 2.33. Therefore, the optical dielectric constant of CeO₂ films is about 5.43. The measured J - E curves in [11] and the simulations of Schottky emission are shown in Figure 3. The experimental data match the Schottky emission theory very well at high temperature (≥ 400 K) in a medium electric field (0.5~1.6 MV/cm). The corresponding conduction band offset between Al and CeO₂ is then determined to be 0.62 ± 0.01 eV.

Besides the simulation method, Schottky plot is the most popular way to identify the barrier height at the interface. For a standard Schottky emission, the plot of $\log(J/T^2)$ versus $E^{1/2}$ should be linear. The barrier height can be obtained from the intercept of Schottky plot. For example, the J - E data measured at high temperatures (>425 K) and in high fields (>1 MV/cm) correlate well with the Schottky emission theory under the gate injection in an Al/ZrO₂ (17.4 nm)/ p -Si MIS capacitor [13], as shown in Figure 4. Moreover, the fitted optical dielectric constant in the plot of standard Schottky emission is extremely close to the square of optical refractive index (i.e., $6.25 = 2.5^2$), and the extracted Schottky barrier height between Al and ZrO₂ is about 0.92 eV.

Simmons indicated that if the electronic mean free path in the insulator is less than the thickness of dielectric film, the equation of standard Schottky emission must be modified [14]. When excited electrons pass through dielectric films, the thermal electrons are affected by traps and interface states, which are generated from oxygen vacancies and thermal instability between dielectric and Si, respectively. The thickness of dielectric films also affects the behavior of Schottky emission. A trap-limited mechanism governs the carrier transportation in dielectric films [13]. Therefore,

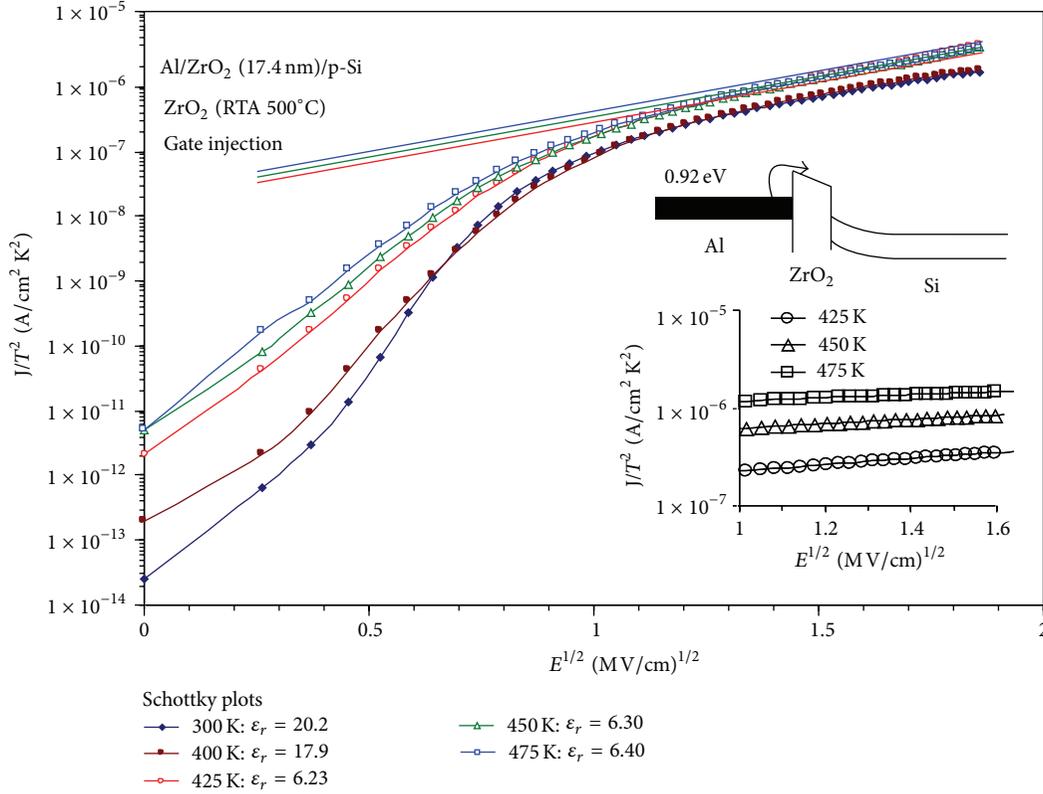


FIGURE 4: Characteristics of standard Schottky emission at various temperatures. Inset graphs present standard Schottky emission constrained by $n = \epsilon_r^{1/2}$ at high temperatures; the band diagram is also shown.

(1) should be modified into (2) when the electronic mean free path (l) is less than the dielectric thickness (t_d):

$$J = \alpha T^{3/2} E \mu \left(\frac{m^*}{m_0} \right)^{3/2} \exp \left[\frac{-q(\phi_b - \sqrt{qE/4\pi\epsilon_r\epsilon_0})}{KT} \right] \quad (2)$$

$(l < t_d),$

where $\alpha = 3 \times 10^{-4} \text{ A s/cm}^3 \text{ K}^{3/2}$ and μ is the electronic mobility in the insulator; the other notations are the same as defined before. Notably, no clear distinction can be made between the bulk- and electrode-limited conduction mechanisms, as indicated by (2), because each is involved in the conduction process [15]. By generating modified Schottky emission plots for ZrO₂ films of various thicknesses, the electronic mean free path in ZrO₂ films can be determined to be between 16.2 and 17.4 nm at high temperature (>425 K) [13]. In addition, the electronic mobility (μ) in ZrO₂ films can be determined from the intercept of the plot of modified Schottky emission. The obtained electronic mobility in ZrO₂ is 12-13 cm²/V-s in a medium field at high temperatures [13].

2.2. Fowler-Nordheim Tunneling. According to the classical physics, when the energy of the incident electrons is less than the potential barrier, the electrons will be reflected. However, quantum mechanism predicts that the electron wave function

will penetrate through the potential barrier when the barrier is thin enough (<100 Å). Hence, the probability of electrons existing at the other side of the potential barrier is not zero because of the tunneling effect. Figure 5 shows the schematic energy band diagram of Fowler-Nordheim (F-N) tunneling. F-N tunneling occurs when the applied electric field is large enough so that the electron wave function may penetrate through the triangular potential barrier into the conduction band of the dielectric. The expression of the F-N tunneling current is

$$J = \frac{q^3 E^2}{8\pi h q \phi_B} \exp \left[\frac{-8\pi(2qm_T^*)^{1/2}}{3hE} \phi_B^{3/2} \right], \quad (3)$$

where m_T^* is the tunneling effective mass in dielectric; the other notations are the same as defined before. To extract the tunneling current, one can measure the current-voltage (I - V) characteristics of the devices at very low temperature. At such a low temperature, the thermionic emission is suppressed and the tunneling current is dominant.

For F-N tunneling, a plot of $\ln(J/E^2)$ versus $1/E$ should be linear. Figure 6 shows the I - V data measured at 77 K for an HfO₂ MIS capacitor biased in the accumulation mode [16]. The inset graph indicates that the fitting of F-N tunneling

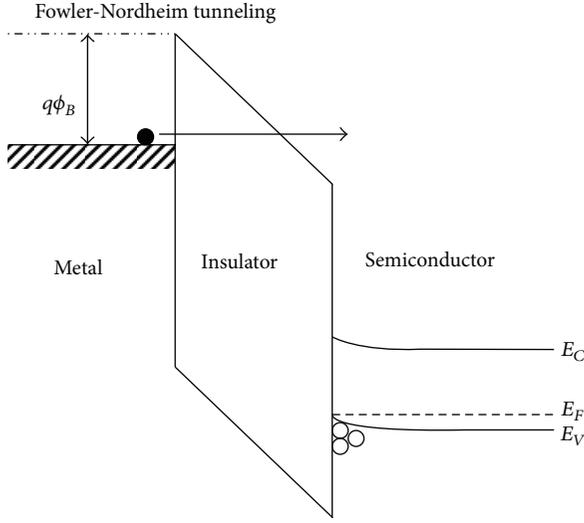


FIGURE 5: Schematic energy band diagram of Fowler-Nordheim tunneling in metal-insulator-semiconductor structure.

theory in high electric fields is very good. The slope of F-N plot can be expressed in (4) [17] and is also a function of electron effective mass and barrier height:

$$\text{slope} = -6.83 \times 10^7 \sqrt{\left(\frac{m_T^*}{m_0}\right)} \phi_B^3. \quad (4)$$

To identify electron effective mass and barrier height, it is useful to measure the thermionic emission current at high temperature and the tunneling current at low temperature. Chiu [16] reported that the electron effective mass in HfO₂ and barrier height at the Al/HfO₂ interface can be determined using the intercept of Schottky plot at high temperatures and the slope of F-N plot at 77 K, as shown in Figure 7. In general, $m_T^* = m^*$ is assumed. Using a mathematical iteration method for a 23.2 nm HfO₂ MIS capacitor, the electron effective mass and barrier height at the Al/HfO₂ interface were extracted to be about $0.4m_0$ and 0.94 eV, respectively [16]. These two parameters are self-consistent with the intercept of Schottky plot and the slope of F-N plot. For the case of a 12.2 nm HfO₂ MIS capacitor, the electron effective mass and Al/HfO₂ barrier height were determined to be $0.09m_0$ and 0.94 eV, respectively.

For HfO₂ films, the correlation between electron effective mass, barrier height, equivalent oxide thickness, and current conduction mechanism was summarized in [16]. In addition, reports showed that the electron effective mass in SiO₂ tends to increase with decreasing oxide thickness in ultrathin silicon dioxide layers [18, 19]. Both parabolic and nonparabolic energy-momentum dispersion were used for measuring the tunneling effective mass in SiO₂. The latter has been found to work better in many cases [18–21]. As the SiO₂ thickness is increased beyond 4 nm, the nonparabolic tunneling effective mass ultimately converges to electron effective mass in SiO₂ [19]. Also, the electron effective mass in SiO₂ is approximately constant over the voltage bias range studied [19, 20]. Based on

these results, the tunneling effective mass can be assumed to be equal to the electron effective mass for dielectric films with wide enough thickness.

2.3. *Direct Tunneling.* There are two main gate current conduction mechanisms in SiO₂ films. If the voltage across the SiO₂ is large enough, the electrons see a triangular barrier and the gate current is due to F-N tunneling. On the other hand, if the voltage across the SiO₂ is small, the electrons see the full oxide thickness and the gate current is due to direct tunneling. The driving oxide voltage between the two mechanisms is approximately 3.1 V for the SiO₂-Si interface. For SiO₂ thicknesses of 4–5 nm and above, F-N tunneling dominates and for SiO₂ thickness less than about 3.5 nm, direct tunneling becomes dominant. The schematic energy band diagram of direct tunneling is shown in Figure 8. Based on the result of Lee and Hu on a polysilicon-SiO₂-silicon structure, the expression of the direct tunneling current density is [12]

$$J = \frac{q^2}{8\pi h \epsilon \phi_B} C(V_G, V, t, \phi_B) \times \exp \left\{ -\frac{8\pi \sqrt{2m^*} (q\phi_B)^{3/2}}{3hq|E|} \cdot \left[1 - \left(1 - \frac{|V|}{\phi_B} \right)^{3/2} \right] \right\}, \quad (5)$$

where t is the thickness of the dielectric, V is the voltage across the dielectric, and the other notations are the same as defined before. The tunneling current components include electron tunneling from the conduction band (ECB), electron tunneling from the valence band (EVB), and hole tunneling from the valence band (HVB). The correction function C can be expressed as [12]

$$C(V_G, V, t, \phi_B) = \exp \left[\frac{20}{\phi_B} \left(\frac{|V| - \phi_B}{\phi_0} + 1 \right)^\alpha \cdot \left(1 - \frac{|V|}{\phi_B} \right) \right] \cdot \frac{V_G}{t} \cdot N, \quad (6)$$

where α is a fitting parameter depending on the tunneling process, $q\phi_0$ is the Si/SiO₂ barrier height (e.g., 3.1 eV for electron and 4.5 eV for hole), and $q\phi_B$ is the actual barrier height (e.g., 3.1 eV for ECB, 4.2 eV for EVB, and 4.5 eV for HVB). N is an auxiliary function which is used as an indicator of carrier population for ECB and HVB cases or transmission probability for EVB case. For ECB and HVB tunneling processes in both the inversion or accumulation regimes, N is given by

$$N = \frac{\epsilon}{t} \left\{ n_{\text{inv}} \nu_T \cdot \ln \left[1 + \exp \left(\frac{V_{G,\text{eff}} - V_{\text{TH}}}{n_{\text{inv}} \nu_T} \right) \right] + \nu_T \cdot \ln \left[1 + \exp \left(-\frac{V_G - V_{\text{FB}}}{\nu_T} \right) \right] \right\}, \quad (7)$$

where $\nu_T (= kT/q)$ is the thermal voltage, V_{TH} is threshold voltage, V_{FB} is flatband voltage, and $V_{G,\text{eff}} = V_G - V_{\text{poly}}$ is the effective gate voltage after accounting for the voltage drop across the polysilicon depletion region. The rate of increase

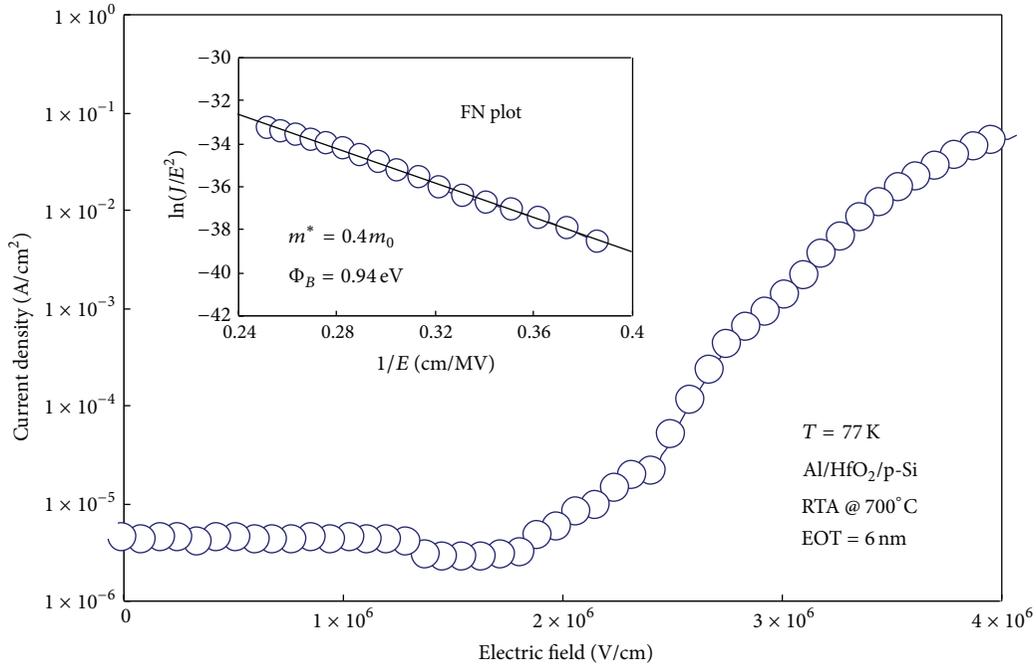


FIGURE 6: Characteristics of J - E plots for HfO_2 MIS capacitor at 77 K. The inset graph presents the Fowler-Nordheim tunneling.

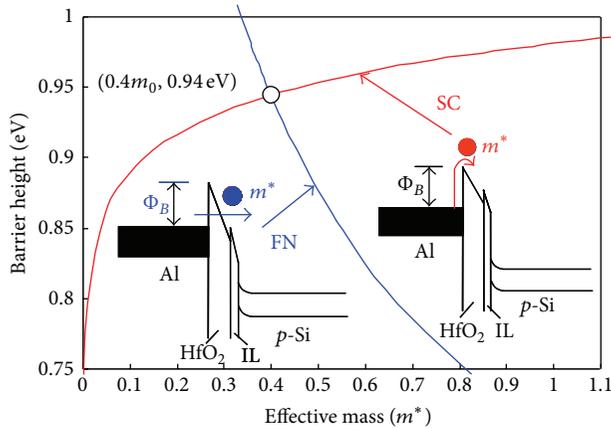


FIGURE 7: The extracted relationships between electron effective mass and Al/ HfO_2 barrier height from the intercept of the Schottky plot at a high temperature (465 K) and the slope of the F-N plot at a low temperature (77 K). The band diagrams for the Schottky emission and F-N tunneling are also shown.

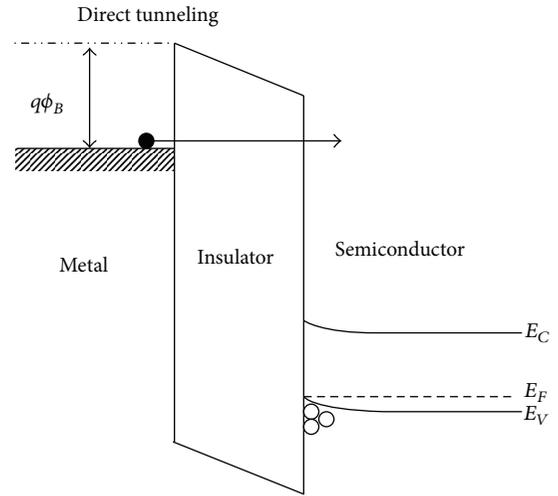


FIGURE 8: Schematic energy band diagram of direct tunneling in metal-insulator-semiconductor structure.

of the subthreshold carrier density with V_G is indicated by the swing parameter n_{inv} , where $n_{\text{inv}} = S/v_T$ and S are the subthreshold swing which is positive for NMOS and negative for PMOS. For EVB tunneling process, N can be written as

$$N = \frac{\varepsilon}{t} \cdot \left\{ 3v_T \cdot \ln \left[1 + \exp \left(\frac{q|V| - E_g}{3kT} \right) \right] \right\}. \quad (8)$$

Equation (5) can be simplified using a binomial expansion and neglecting higher order terms, which leads to

$$J \sim \exp \left\{ -\frac{8\pi(q\phi_B)^{3/2} \sqrt{2m_{\text{eff}}}}{3hq|E|} \left[\frac{3|V|}{2\phi_B} \right] \right\} \quad (9)$$

$$\sim \exp \left\{ -\frac{8\pi\sqrt{2q}}{3h} (m_{\text{eff}}\phi_B)^{1/2} \kappa \cdot t_{\text{ox,eq}} \right\}.$$

Yeo et al. indicated the scaling limits of alternative gate dielectrics based on their direct tunneling characteristics and

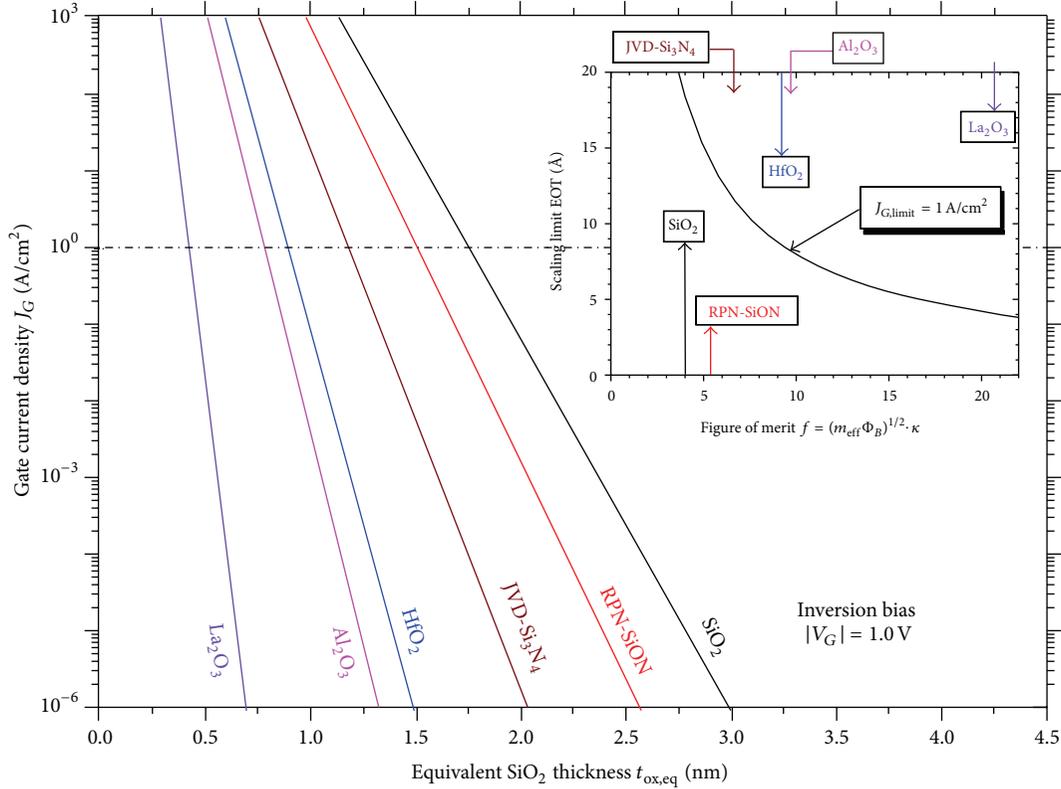


FIGURE 9: Scaling limit for several gate dielectrics when $V_{dd} = 1.0$ V and $J_{G,limit} = 1$ A/cm² [12].

gate leakage requirements for future CMOS technology [22]. The tunneling leakage current for a given EOT (equivalent oxide thickness, $t_{ox,eq}$) is not only dependent on the κ value of a gate dielectric but also tunneling barrier height ($q\phi_B = \Phi_B$) and tunneling effective mass (m_{eff}). They introduced a figure of merit to compare the relative advantages of gate dielectric candidates. The figure of merit is given by $f = (m_{eff}\Phi_B)^{1/2} \cdot \kappa$. Figure 9 shows the scaling limit for several gate dielectrics when V_G or V_{dd} is specified to be 1.0 V and the maximum tolerable gate current density $J_{G,limit}$ is 1 A/cm². A dielectric with a larger figure of merit possesses a lower scaling limit EOT, as shown in the inset of Figure 9. The EOT scaling limits of La_2O_3 and HfO_2 are about 4 Å and 9 Å, respectively.

2.4. Thermionic-Field Emission. Thermionic-field emission takes place intermediately between field emission and Schottky emission. In this condition, the tunneling electrons should have the energy between the Fermi level of metal and the conduction band edge of dielectric. The schematic energy band diagram of thermionic-field emission is shown in Figure 10(a). The difference between thermionic emission, thermionic-field emission, and field emission is shown in Figure 10(b). The current density due to thermionic-field emission can be roughly expressed as [8]

$$J = \frac{q^2 \sqrt{m}(kT)^{1/2} E}{8\hbar^2 \pi^{5/2}} \exp\left(-\frac{q\phi_B}{kT}\right) \exp\left[\frac{\hbar^2 q^2 E^2}{24m(kT)^3}\right]. \quad (10)$$

3. Bulk-Limited Conduction Mechanisms

The bulk-limited conduction mechanisms depend on the electrical properties of the dielectric itself. The most important parameter in this type of conduction mechanism is the trap energy level in the dielectric films. The bulk-limited conduction mechanisms include (1) Poole-Frenkel emission, (2) hopping conduction, (3) ohmic conduction, (4) space-charge-limited conduction, (5) ionic conduction, and (6) grain-boundary-limited conduction. Based on the bulk-limited conduction mechanisms, some important electrical properties in the dielectric films can be extracted, including the trap energy level, the trap spacing, the trap density, the electronic drift mobility, and the dielectric relaxation time, the density of states in the conduction band.

3.1. Poole-Frenkel Emission. Poole-Frenkel (P-F) emission involves a mechanism which is very similar to Schottky emission; namely, the thermal excitation of electrons may emit from traps into the conduction band of the dielectric. Therefore, P-F emission is sometimes called the internal Schottky emission. Considering an electron in a trapping center, the Coulomb potential energy of the electron can be reduced by an applied electric field across the dielectric film. The reduction in potential energy may increase the probability of an electron being thermally excited out of the trap into the conduction band of the dielectric. The schematic energy band diagram of P-F emission is shown in Figure 11. For

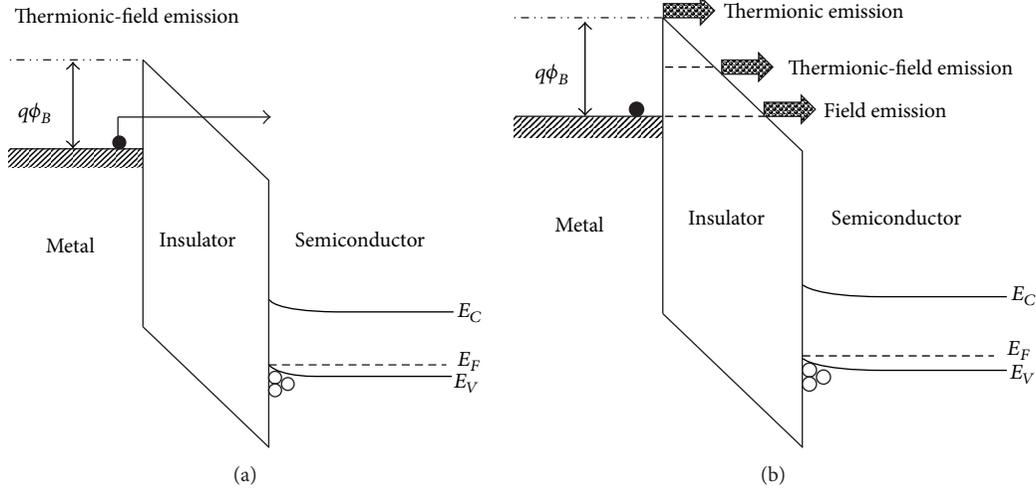


FIGURE 10: (a) Schematic energy band diagram of thermionic-field emission in metal-insulator-semiconductor structure. (b) Comparison of thermionic-field emission, thermionic emission, and field emission.

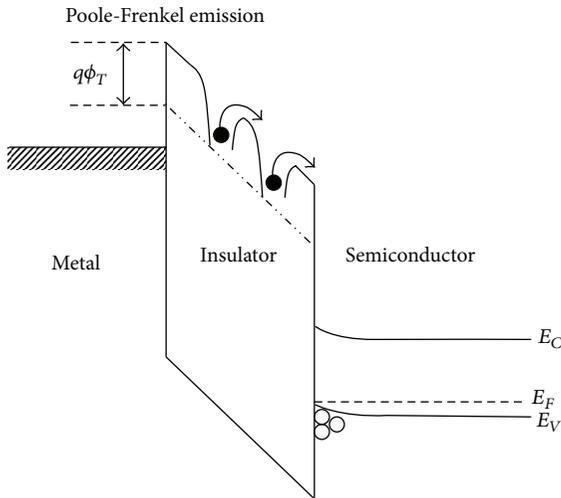


FIGURE 11: Schematic energy band diagram of Poole-Frenkel emission in metal-insulator-semiconductor structure.

a Coulombic attraction potential between electrons and traps, the current density due to the P-F emission is

$$J = q\mu N_C E \exp \left[\frac{-q(\phi_T - \sqrt{qE/\pi\epsilon_i\epsilon_0})}{kT} \right], \quad (11)$$

where μ is the electronic drift mobility, N_C is the density of states in the conduction band, $q\phi_T$ ($=\Phi_T$) is the trap energy level, and the other notations are the same as defined before. Since P-F emission is owing to the thermal activation under an electric field, this conduction mechanism is often observed at high temperature and high electric field. Chiu et al. reported that the dominant conduction mechanism through Pr_2O_3 is the P-F emission at high temperature and high electric field [23]. Figure 12 shows the measured J - E data and

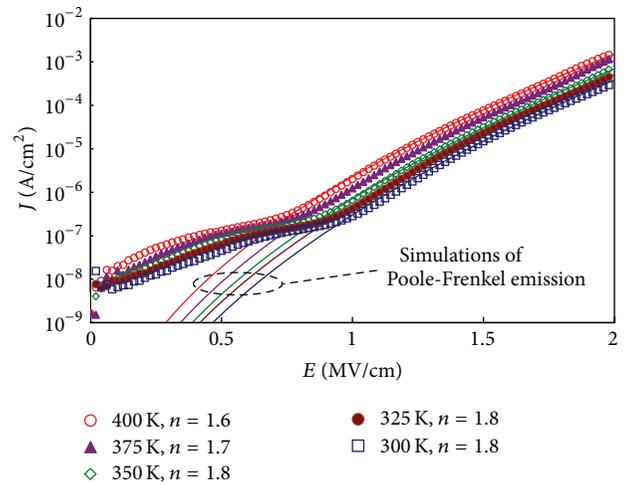


FIGURE 12: Characteristics of J - E plot and simulation of P-F emission for the laminated $\text{Pr}_2\text{O}_3/\text{SiON}$ MIS capacitors at high fields.

the modeled P-F emission curves for the laminated $\text{Pr}_2\text{O}_3/\text{SiON}$ MIS capacitors. The experimental data match the modeled curves very well in high electric fields (>1 MV/cm) from 300 K to 400 K. Therefore, the dominant conduction mechanism is the P-F emission in high electric fields at temperatures ranging from 300 K to 400 K. In addition, the trap energy level in Pr_2O_3 can be extracted by using the Arrhenius plot, as shown in Figure 13. The determined trap energy level in Pr_2O_3 is about 0.56 ± 0.01 eV. Besides the simulation method, P-F plot is also a popular way to identify the trap energy level in dielectric films. For the P-F emission, a plot of $\ln(J/E)$ versus $E^{1/2}$ is linear. The trap barrier height can be extracted from the intercept of P-F plot. Figure 14 shows the P-F plot for a 17.4 nm ZrO_2 MIS capacitor in

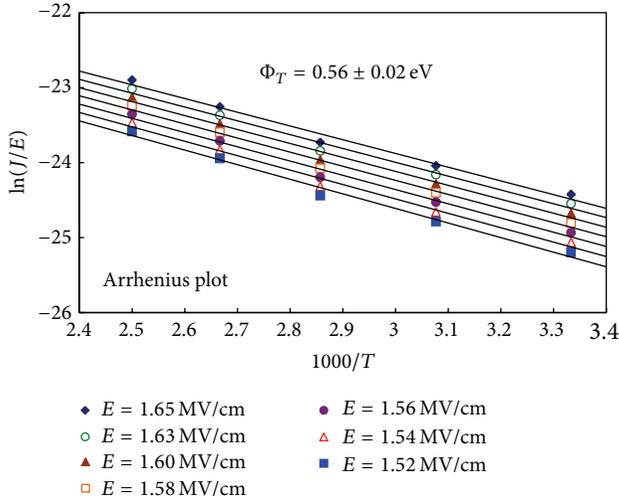


FIGURE 13: Arrhenius plot of the P-F emission for the laminated $\text{Pr}_2\text{O}_3/\text{SiON}$ MIS capacitors at high fields.

the accumulation mode at high temperatures (>425 K) and in low electric fields (<0.6 MV/cm) [13]. Under the constraint of $n = \epsilon_r^{1/2}$, the trap barrier height in ZrO_2 films was extracted to be about 1.1 eV according to the intercepts of the fitted lines in the P-F plot.

Aside from the intercept of P-F plot for the trap barrier, the slope of P-F plot is an important factor for determining the optical dielectric constant (ϵ_r) in dielectric films. For the case of Pr_2O_3 MIS capacitors [23], the fitted ϵ_r is 3 ± 0.3 and the fitted refractive index is 1.7 ± 0.1 . The refractive index obtained by the electrical method is fairly close to the one obtained by the optical method ($n = 1.7$ -1.8). This implies that during the emission process, the electron transit time from the trap site to the barrier maximum position is shorter than the dielectric relaxation time. Consequently, the dielectric film does not have enough time to be polarized during the emission process and the optical dielectric constant should be used in this case. Besides the trap energy level and the optical dielectric constant, the electronic drift mobility in dielectric films can also be extracted by the analyses of P-F emission. One can find the result of electron mobility in Pr_2O_3 films in [23]. Note that Angle and Talley proposed that the free electrons in P-F emission are emitted from the donor centers [24]. If there are other defect states such as trap states or acceptor centers in dielectric films, the number of emitted free electrons from the donor center will decrease. The existence of the trapping centers may influence the relation of current density and electric field. Accordingly, the P-F emission is dependent on the concentration of trap centers (N_t) and donor centers (N_d). When $N_t < N_d$, the conduction mechanism is called the normal P-F emission [24]. When $N_t \cong N_d$, the conduction mechanism is called the modified P-F emission or anomalous Poole-Frenkel effect [24]. In such a case, the slope of P-F plot is reduced by half and equals the slope of Schottky plot. To distinguish the Schottky emission and modified P-F emission, the effect of different

electrode materials on the conduction characteristics is a valuable means.

3.2. Hopping Conduction. Hopping conduction is due to the tunneling effect of trapped electrons “hopping” from one trap site to another in dielectric films. Figure 15 shows the schematic energy band diagram of hopping conduction. The expression of hopping conduction is [5, 10, 23]

$$J = qanv \exp \left[\frac{qaE}{kT} - \frac{E_a}{kT} \right], \quad (12)$$

where a is the mean hopping distance (i.e., the mean spacing between trap sites), n is the electron concentration in the conduction band of the dielectric, v is the frequency of thermal vibration of electrons at trap sites, and E_a is the activation energy, namely, the energy level from the trap states to the bottom of conduction band (E_C); the other terms are as defined above. The P-F emission corresponds to the thermionic effect and the hopping conduction corresponds to the tunnel effect. In P-F emission, the carriers can overcome the trap barrier through the thermionic mechanism. However, in hopping conduction, the carrier energy is lower than the maximum energy of the potential barrier between two trapping sites. In such case, the carriers can still transit using the tunnel mechanism.

Chiu et al. [23] reported that the experimental J - E data match the simulated hopping conduction curves very well from 300 K to 400 K in low electric fields (<0.6 MV/cm) in a Pr_2O_3 MIS structure, as shown in Figure 16. From the simulations of hopping conduction, the mean hopping distance in the Pr_2O_3 films was determined to be about 1.5 ± 0.1 nm. Using the slopes of Arrhenius plot in low fields, the activation energy was determined to be about 50 ± 1 meV, as shown in Figure 17. Furthermore, according to (12), the trap spacing can be extracted by the slope of linear part of $\log(J)$ versus E . Figure 18 shows the J - E characteristics at temperatures ranging from 300 K to 425 K for a Pt/MgO/Pt memory device in high resistance state [25]. Simulation results show that the measured data match the theory of hopping conduction very well when the electric field is larger than about 0.25 MV/cm. Based on the slope in Figure 18, the trap spacing in MgO can be determined to be about 1.0 nm [25]. In Figure 18, we can observe an interesting characteristic, that is, a lower current density is observed at a higher temperature. This finding is far different from the normal J - E characteristics in dielectric films in which the higher current density can be achieved in a higher temperature. In the case of Pt/MgO/Pt, a simulation work can be adopted by varying the trapping level [25]. Therefore, the temperature dependence of the trap energy levels in MgO can be obtained, as shown in Figure 19. The trap energy level increases with increasing temperature. This result indicates that the defects with deeper level are activated by the elevated temperature. Hence, the deeper trap level activated at higher temperature leads to the exponential decrease in current density.

3.3. Ohmic Conduction. Ohmic conduction is caused by the movement of mobile electrons in the conduction band and

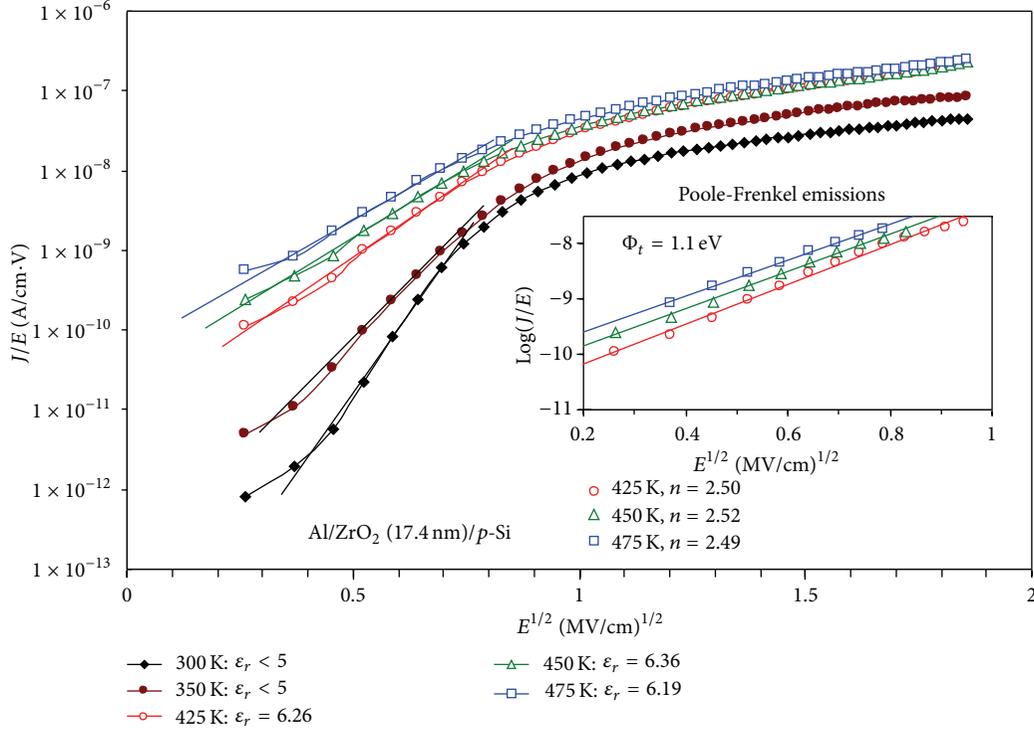


FIGURE 14: Characteristics of P-F emission at various temperatures. Inset graph presents Poole-Frenkel emission constrained by $n = \epsilon_r^{1/2}$ at high temperatures.

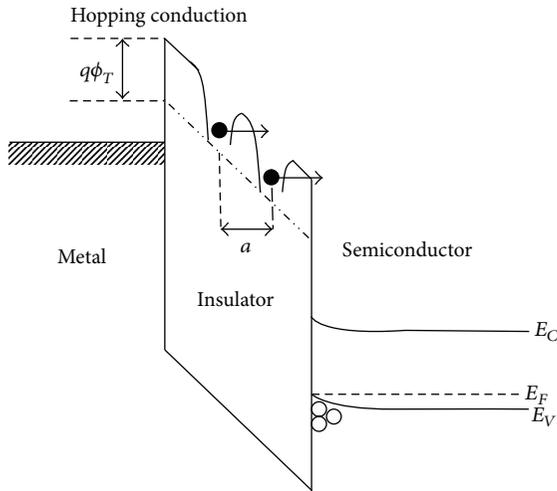


FIGURE 15: Energy band diagram of hopping conduction in metal-insulator-semiconductor structure.

holes in the valence band. In this conduction mechanism, a linear relationship exists between the current density and the electric field. Figure 20 shows a schematic energy band diagram of the Ohmic conduction due to electrons. Although the energy band gap of dielectrics is by definition large, there will still be a small number of carriers that may be generated due to the thermal excitation. For example, the electrons may be excited to the conduction band, either from the valence

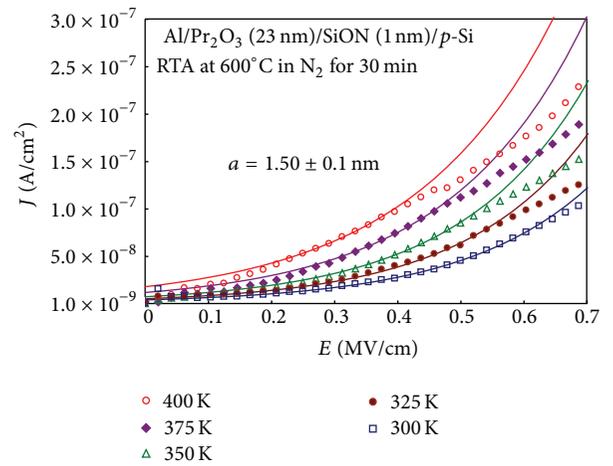


FIGURE 16: J - E characteristics and simulation of hopping conduction for a laminated $\text{Pr}_2\text{O}_3/\text{SiON}$ MIS capacitors at low electric fields.

band or from the impurity level. The carrier numbers will be very small but they are not zero. The current density of ohmic conduction can be expressed as

$$J = \sigma E = nq\mu E, \quad n = N_C \exp \left[\frac{-(E_C - E_F)}{kT} \right], \quad (13)$$

where σ is electrical conductivity, n is the number of electrons in the conduction band, μ is electron mobility, and N_C is

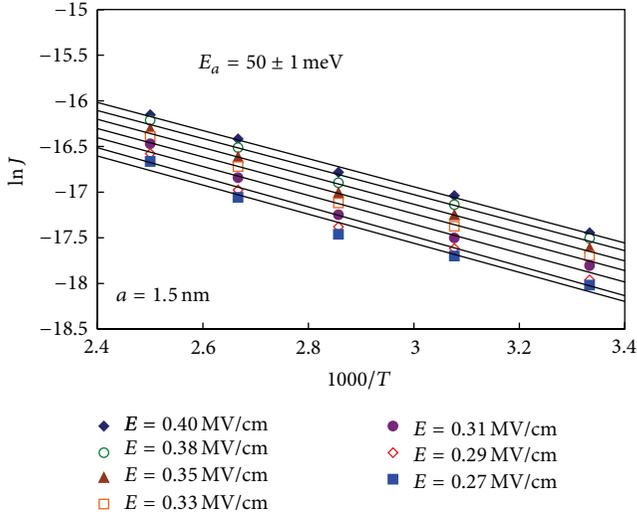


FIGURE 17: Arrhenius plot of the hopping conduction at low fields for the laminated $\text{Pr}_2\text{O}_3/\text{SiON}$ MIS capacitors.

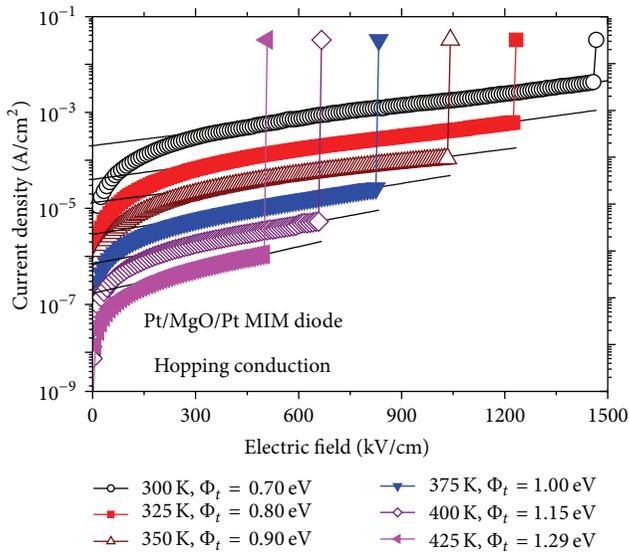


FIGURE 18: Experimental data and simulation curves of hopping conduction in high resistance state in Pt/MgO/Pt memory device.

the effective density of states of the conduction band; the other terms are as defined above.

Because the energy band gap of a dielectric is very large, we can assume that the Fermi level E_F is close to the middle of the energy band gap; that is, $E_C - E_F \sim E_g/2$. In this case, the ohmic conduction current is $J = q\mu EN_C \exp(-E_g/2kT)$. The magnitude of this current is very small. This current mechanism may be observed if there is no significant contribution from other conduction mechanisms of current transport in dielectrics [10]. The ohmic conduction current due to mobile electrons in the conduction band or similarly holes in the valence band is linearly dependent on the electric field. This current usually may be observed at very low voltage in the current-voltage (I - V) characteristics of the dielectric films.

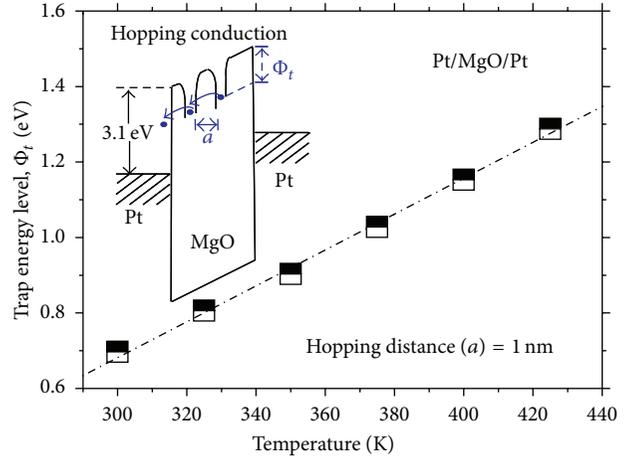


FIGURE 19: Temperature dependence of the trap energy levels in high resistance state. Inset graph shows the band diagram of hopping conduction in Pt/MgO/Pt memory cells.

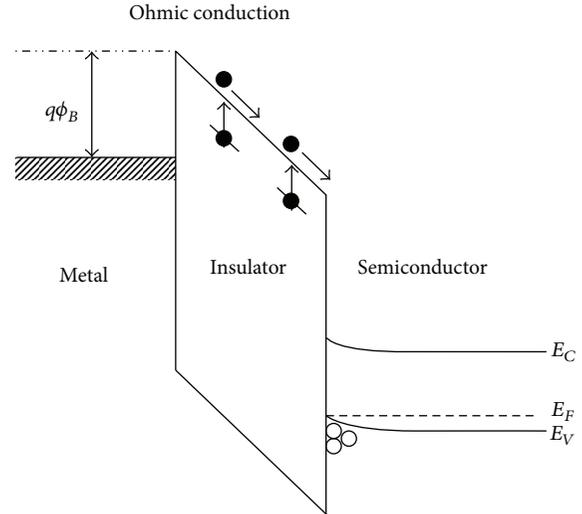


FIGURE 20: Energy band diagram of ohmic conduction in metal-insulator-semiconductor structure.

Recently, the resistance switching behaviors in dielectric films have been extensively studied [26–29]. The ohmic conduction can be often observed in low resistance state in the resistance switching memory devices. Figure 21 shows the J - E curves in a double-logarithmic plot in low resistance state in Pt/ZnO/Pt memory devices [29]. The linear relation between current density and electric field is observed, which matches the ohmic conduction very well because the slopes are very close to 1. In Figure 21, the current density increases with increasing temperature. Hence, the linear relation between electrical conductivity (σ) and inverse temperature can be derived from Figure 21, as shown in Figure 22. Using the Arrhenius plot, the Fermi level (E_F) of ZnO is determined to be about 0.4 eV below the conduction band edge in ZnO (E_C), as shown in the inset of Figure 22. Consequently, the product of μ and N_C at each temperature can be extracted by

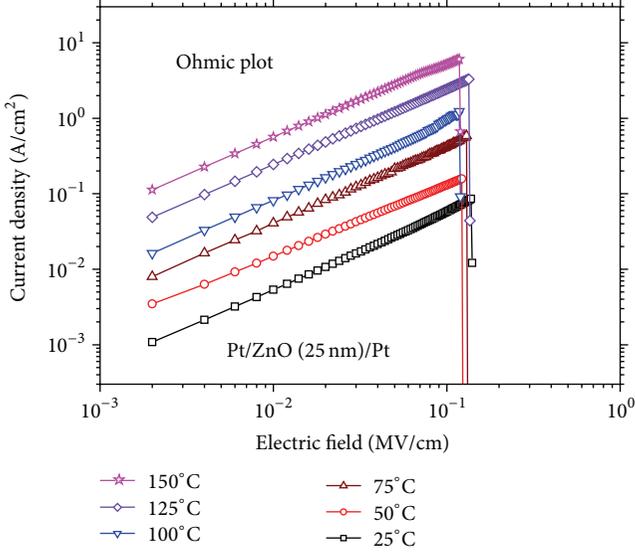


FIGURE 21: Linear relation between current density and electric field at temperature ranging from 25 to 150°C in low resistance state in Pt/ZnO/Pt memory devices.

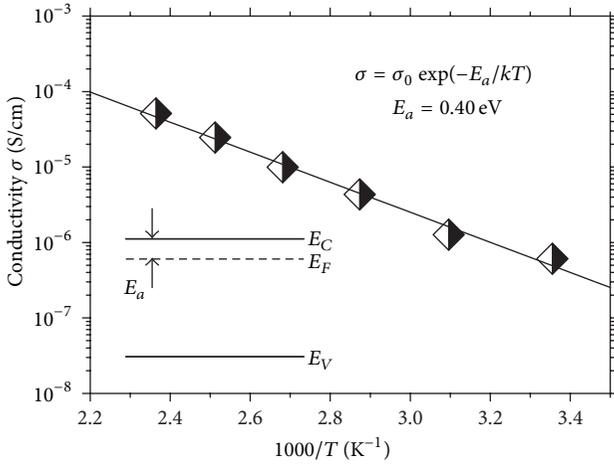


FIGURE 22: Temperature dependence of the electrical conductivity in low resistance state in Pt/ZnO/Pt memory devices. The inset graph shows the location of Fermi level in ohmic conduction.

the combination of E_F and σ . In addition, N_C is a function of temperature, which is proportional to $\beta T^{3/2}$, where β is a constant [30]. The effective density of states of the conduction band (N_C) in ZnO at room temperature is $4.8 \times 10^{18} \text{ cm}^{-3}$ [31]. Therefore, the temperature-dependent electron mobility (μ) and effective density of states of the conduction band (N_C) in ZnO can be obtained, as shown in Figure 23. At room temperature the electron mobility in ZnO films is about $4.6 \text{ cm}^2/\text{V}\cdot\text{s}$.

3.4. Space-Charge-Limited Conduction. The mechanism of space-charge-limited conduction (SCLC) is similar to the transport conduction of electrons in a vacuum diode.

The thermionic cathode of a vacuum diode can emit electrons with a Maxwellian distribution of initial velocities (v). The corresponding charge distribution can be written by the Poisson's equation:

$$\frac{\partial^2 V}{\partial x^2} = -\frac{\rho(x)}{\epsilon_0}. \quad (14)$$

Moreover, in the steady state, with the condition $v(x) = [2qV(x)/m]^{1/2}$, the continuity equation is

$$j_x = qn(x)v(x). \quad (15)$$

The current density-voltage (J - V) characteristic of a vacuum diode is governed by the Child's law:

$$J = \frac{4\epsilon_0}{9} \left(\frac{2e}{m} \right)^{1/2} \frac{V^{3/2}}{d^2}. \quad (16)$$

In a solid material, the space-charge-limited current is caused by the injection of electrons at an ohmic contact. The continuity equation should include the diffusion component and can be written as

$$j_x = en(x)v(x) + eD \frac{dn}{dx}. \quad (17)$$

A typical J - V characteristic plotted in a log-log curve for space-charge-limited current is shown in Figure 24. The J - V characteristic in the log J -log V plane is bounded by the three limited curves, namely, ohm's law ($J_{\text{Ohm}} \propto V$), traps-filled limit (TFL) current ($J_{\text{TFL}} \propto V^2$), and Child's law ($J_{\text{Child}} \propto V^2$). V_{tr} and V_{TFL} are the transition voltage at the departure from ohm's law and TFL curve, respectively:

$$J_{\text{Ohm}} = qn_0 \mu \frac{V}{d}, \quad (18)$$

$$J_{\text{TFL}} = \frac{9}{8} \mu \epsilon \theta \frac{V^2}{d^3}, \quad (19)$$

$$J_{\text{Child}} = \frac{9}{8} \mu \epsilon \frac{V^2}{d^3}, \quad (20)$$

$$V_{\text{tr}} = \frac{8}{9} \times \frac{qn_0 d^2}{\epsilon \theta}, \quad (21)$$

$$\theta = \frac{N_C}{g_n N_t} \exp\left(\frac{E_t - E_C}{kT}\right), \quad (22)$$

$$V_{\text{TFL}} = \frac{qN_t d^2}{2\epsilon}, \quad (23)$$

$$\tau_c = \frac{d^2}{\mu \theta V_{\text{tr}}}, \quad (24)$$

$$\tau_d = \frac{\epsilon}{qn\mu\theta}, \quad (25)$$

where n_0 is the concentration of the free charge carriers in thermal equilibrium, V is the applied voltage, d is the thickness of thin films, ϵ is the static dielectric constant, θ is the

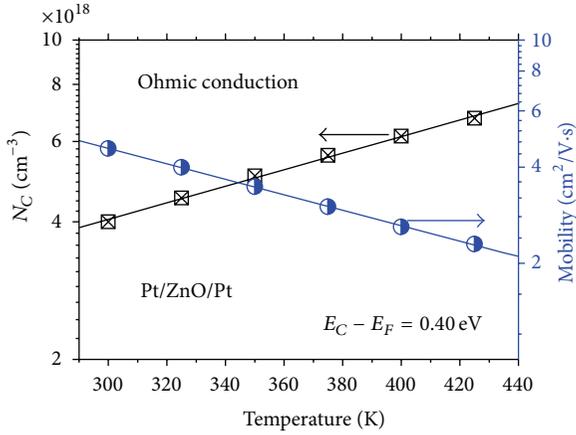


FIGURE 23: Temperature dependence of the electron mobility and the effective density of states of the conduction band in low resistance state in Pt/ZnO/Pt memory devices.

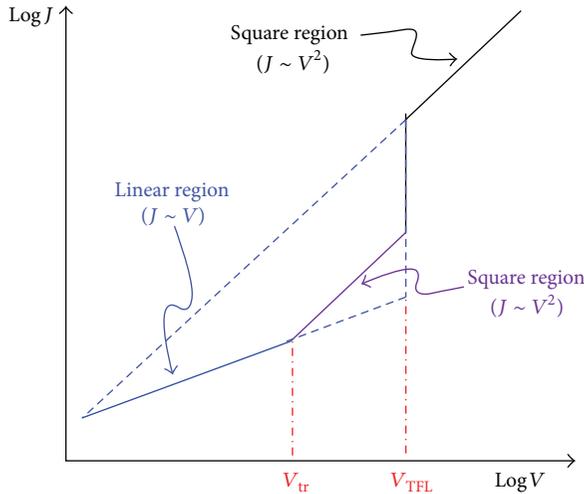


FIGURE 24: A typical current density-voltage (I - V) characteristic of space-charge-limited conduction current. V_{tr} is transition voltage. V_{TFL} is trap-filled limit voltage.

ratio of the free carrier density to total carrier (free and trapped) density, g_n is the degeneracy of the energy state in the conduction band, E_t is the trap energy level, N_t is the trap density, n is the concentration of the free carrier in the insulator, and the other terms are as defined above. It is noticed that (20) is the Mott-Gurney relation which indicates the space-charge-limited current under the condition of single type of carriers and no traps. If there are traps in the dielectric, the SCL conduction can be described by (19) based on the assumption of monoenergetical trapping levels in the dielectric [5–7, 10].

At low applied voltages ($V < V_{tr}$), J - V characteristics followed the ohm's law, which implies that the density of thermally generated free carriers (n_0) inside the films is larger than the injected carriers [32]. This ohmic mode takes place

in the electrically quasineutral state corresponding to the situation when partial trap centers are filled at weak injection. When the transition from the ohmic to the space-charge-limited region, the carrier transit time (τ_c) at V_{tr} (the minimum voltage required for the transition) becomes equal to the dielectric relaxation time (τ_d) [2]. The onset of the departure from ohm's law or the onset of the SCL conduction takes place when the applied voltage reaches the value of V_{tr} . Accordingly, $\tau_c \cong \tau_d$ can be extracted at the transition point V_{tr} . If the applied voltage V is smaller than V_{tr} , then the carrier transit time τ_c is larger than the dielectric relaxation time τ_d . This implies that the injected carrier density n is small in comparison with n_0 and that the injected carriers will redistribute themselves with a tendency to maintain electric charge neutrality internally in a time comparable to τ_d . Consequently, the injected carriers have no chance to travel across the insulator. The redistribution of the charge is known as dielectric relaxation. The ohmic behavior can be observed only after these space charge carriers become trapped. Figure 25 shows the schematic diagrams of carrier distributions in dielectric film in SCLC mechanism under the conditions of (a) very weak injection ($V < V_{tr}$, $n < n_0$, $\tau_c > \tau_d$), (b) dielectric relaxation and carriers redistribution, and (c) weak injection at V_{tr} ($V = V_{tr}$, $n = n_0$, $\tau_c = \tau_d$).

In the case of strong injection, the traps are filled up and a space charge appears. When $V > V_{tr}$ and $\tau_c \sim \tau_d$ or $\tau_c < \tau_d$, the injected excess carriers dominate the thermally generated carrier since the injected carrier transit time is too short for their charge to be relaxed by the thermally generated carriers. It is noted that for $V < V_{tr}$, τ_c increases with decreasing V but τ_d remains almost constant, while for $V > V_{tr}$, τ_c decreases with increasing V and τ_d also decreases with increasing V since the increase in V causes an increase in free carrier density in the dielectric. The increase of applied voltage may increase the density of free carriers resulting from injection to such a value that the Fermi level (E_{Fn}) moves up above the electron trapping level (E_t). The trap-filled limit (TFL) is the condition for the transition from the trapped J - V characteristics to the trap-free J - V characteristics. It can be imagined that after all traps are filled up, the subsequently injected carriers will be free to move in the dielectric films, so that at the subthreshold voltage (V_{TFL}) to set on this transition, the current will rapidly jump from its low trap-limited value to a high trap-free SCL current. V_{TFL} is defined as the voltage required to fill the traps or, in other words, as the voltage at which Fermi level (E_{Fn}) passes through E_t .

In the case of very strong injection, all traps are filled and the conduction becomes the space-charge-limited (Child's law). Thus a space charge layer in the dielectric builds up and the electric field cannot be regarded as constant any longer. While the bias voltage reaches V_{TFL} in the strong injection mode, the traps get gradually saturated, which means that the Fermi-level gets closer to the bottom of the conduction band. This results in a strong increase of the number of free electrons, thus explaining the increase of the current for $V = V_{TFL}$. For the voltage $> V_{TFL}$, the current is fully controlled by the space charge, which limits the further injection of free carriers in the dielectric. Square law dependence of

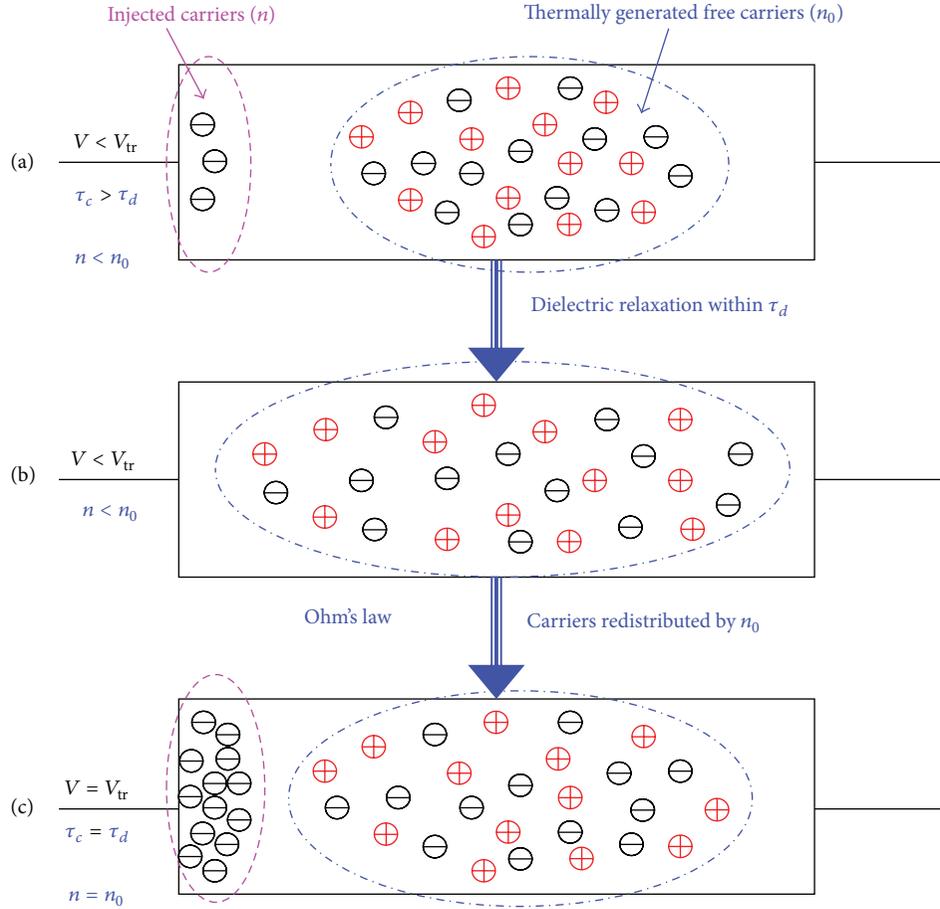


FIGURE 25: Carriers distribution in dielectric film under carrier weak injection ($V \leq V_{tr}$) in space-charge-limited conduction. (a) Very weak injection ($V < V_{tr}$, $n < n_0$, $\tau_c > \tau_d$), (b) dielectric relaxation and carriers redistribution, and (c) weak injection at V_{tr} ($V = V_{tr}$, $n = n_0$, $\tau_c = \tau_d$). V_{tr} is the transition voltage at the onset of departure from ohm's law; n is the concentration of injected carriers; n_0 is the concentration of thermally generated free carriers in dielectric film; τ_c is the carrier transit time; τ_d is the dielectric relaxation time.

the current ($J \sim V^2$, Child's law) is the consequence of the space charge controlled current. Figure 26 shows the schematic diagrams of carrier and trap distributions in dielectric film in SCLC mechanism under the conditions of (a) strong injection ($V > V_{tr}$, $n < n_0 < N_t$, $\tau_c < \tau_d$), (b) trap-filled-limited conduction ($V_{tr} < V < V_{TFL}$, $n < n_0 < N_t$, $E_{Fn} < E_t$): trapped behavior, parts of traps are filled up, and (c) space-charge-limited conduction ($V > V_{TFL}$, $n_0 > N_t$, $E_{Fn} > E_t$): trap-free behavior, all traps are filled up.

A report [32] showed that the dominant conduction mechanism through the polycrystalline La_2O_3 films is space-charge-limited current, as shown in Figure 27. Three different regions, ohm's law region, trap-filled-limited region, and Child's law region are observed in the current density-voltage (J - V) characteristics at room temperature. Based on the SCLC study in [32], some valuable electrical properties in polycrystalline La_2O_3 were obtained. For example, at room temperature, the trap density (N_t) is about $9.2 \times 10^{17} \text{ cm}^{-3}$, the trap energy level (E_t) is about 0.21 eV, the trap capture cross-section (σ_t) is about $1.2 \times 10^{-21} \text{ cm}^2$, the effective density of states in the conduction band (N_C) is about

$5.5 \times 10^{18} \text{ cm}^{-3}$, the maximum of dielectric relaxation time ($\tau_{d,max}$) is about $8.8 \times 10^{-5} \text{ s}$, and the electron mobility (μ) is about $8.2 \times 10^{-7} \text{ cm}^2/\text{V}\cdot\text{s}$. In addition, some important electrical properties in polycrystalline Dy_2O_3 were also obtained according to the SCLC mechanism [33]. At 350 K, the trap density (N_t) is about $1.5 \times 10^{19} \text{ cm}^{-3}$, the trap energy level (E_t) is about 0.20 eV, the trap capture cross-section (σ_t) is about $3.2 \times 10^{-21} \text{ cm}^2$, the effective density of states in the conduction band (N_C) is about $4.5 \times 10^{21} \text{ cm}^{-3}$, the maximum of dielectric relaxation time ($\tau_{d,max}$) is about $8.2 \times 10^{-6} \text{ s}$, and the electron mobility (μ) is about $1.2 \times 10^{-6} \text{ cm}^2/\text{V}\cdot\text{s}$.

3.5. Ionic Conduction. Ionic conduction results from the movement of ions under an applied electric field. The movement of the ions may come from the existence of lattice defects in the dielectric films. Due to the influence of external electric field on defect energy level, the ions may jump over a potential barrier from one defect site to another. Figure 28(a) shows a schematic energy band diagram of ionic

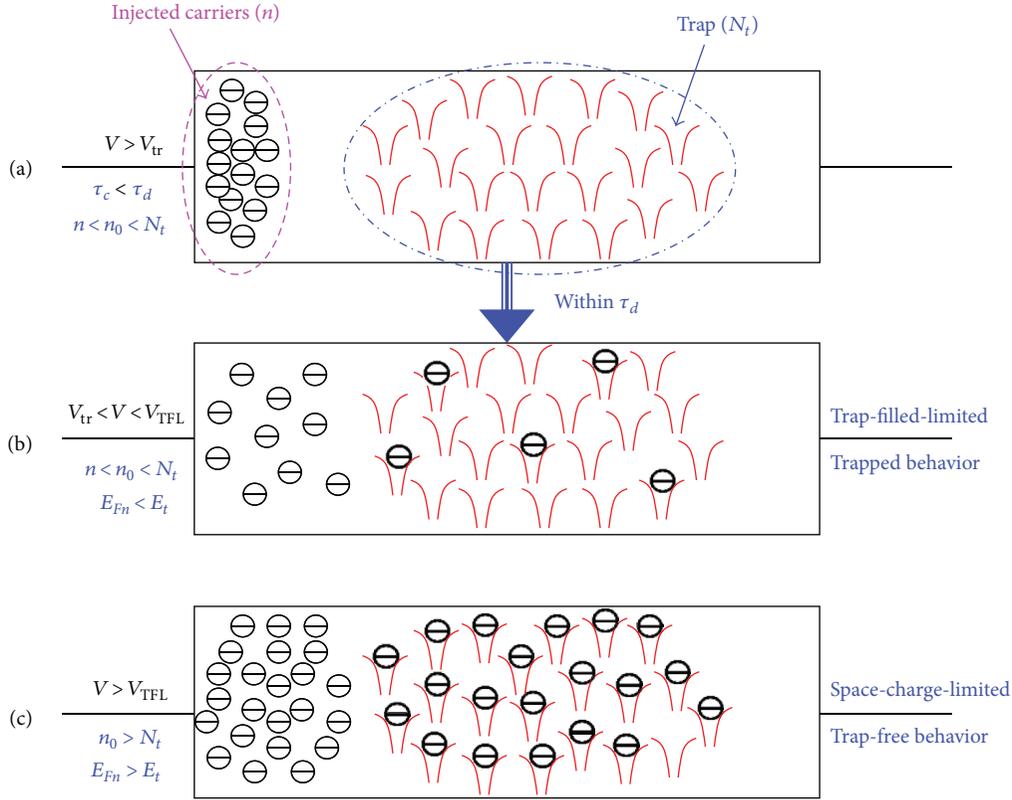


FIGURE 26: Carriers distribution in dielectric film under carrier strong injection ($V > V_{tr}$) in space-charge-limited conduction. (a) Strong injection ($V > V_{tr}$, $n < n_0 < N_t$, $\tau_c < \tau_d$), (b) trap-filled-limited ($V_{tr} < V < V_{TFL}$, $n < n_0 < N_t$, $E_{Fn} < E_t$): parts of traps are filled up (trapped behavior), and (c) space-charge-limited ($V > V_{TFL}$, $n_0 > N_t$, $E_{Fn} > E_t$): all traps are filled up (trap-free behavior). V_{tr} and V_{TFL} are the transition voltage at the departure from ohm's law and TFL curve, respectively; n is the concentration of injected carriers; n_0 is the concentration of thermally generated free carriers; N_t is the trap density; τ_c is the carrier transit time; τ_d is the dielectric relaxation time; E_{Fn} is the Fermi level; E_t is the trapping level.

conduction without the applied electric field. Figure 28(b) shows the condition with the applied electric field [10]. The ionic conduction current can be expressed as

$$J = J_0 \exp \left[- \left(\frac{q\phi_B}{kT} - \frac{Eqd}{2kT} \right) \right], \quad (26)$$

where J_0 is the proportional constant, $q\phi_B$ is the potential barrier height, E is the applied electric field, d is the spacing of two nearby jumping sites, and the other terms are as defined above. Because the ion mass is large, the mechanism of ionic conduction is usually not important for the applications of dielectric films in CMOS technology.

3.6. Grain-Boundary-Limited Conduction. In a polycrystalline dielectric material, the resistivity of the grain boundaries may be much higher than that of the grains. Therefore, the conduction current could be limited by the electrical properties of the grain boundaries. In this case, the conduction mechanism is called the grain-boundary-limited conduction [10, 34]. The grain boundary will build a grain boundary potential energy barrier (Φ_B) which is inversely

proportional to the relative dielectric constant of the dielectric material. The potential energy barrier can be written as

$$\Phi_B = q\phi_B = \frac{q^2 n_b^2}{2\epsilon N}, \quad (27)$$

where n_b is the grain boundary trap density, ϵ is the relative dielectric constant of the dielectric material, and N is the dopant concentration. From (27), it can be seen that the dielectric constant can significantly affect the potential energy barrier at the grain boundaries.

Figure 29(a) shows the charge distribution across an electron-trapped grain boundary and the existence of depletion regions next to the grain boundary. The potential energy barrier at the grain boundary is shown in Figure 29(b) due to the charge distribution close to the grain boundary. Figure 30 indicates an energy band diagram of the grain-boundary-limited conduction in a metal-insulator-metal MIM diode.

4. Summary

The conduction mechanisms in dielectric films are discussed in detail in this review. There are two types of conduction

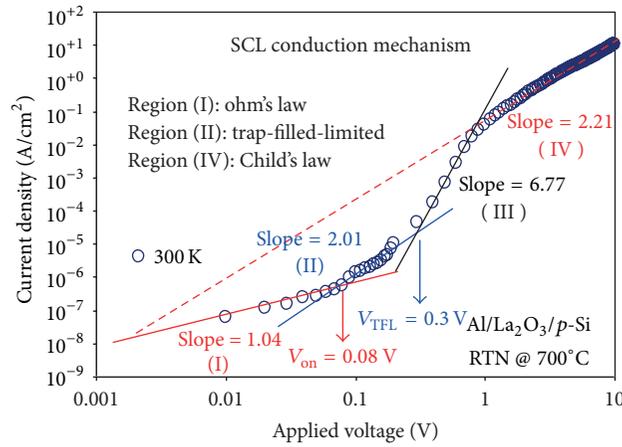


FIGURE 27: Logarithm of the current density plotted as a function of the logarithm of the applied voltage under negative bias at room temperature.

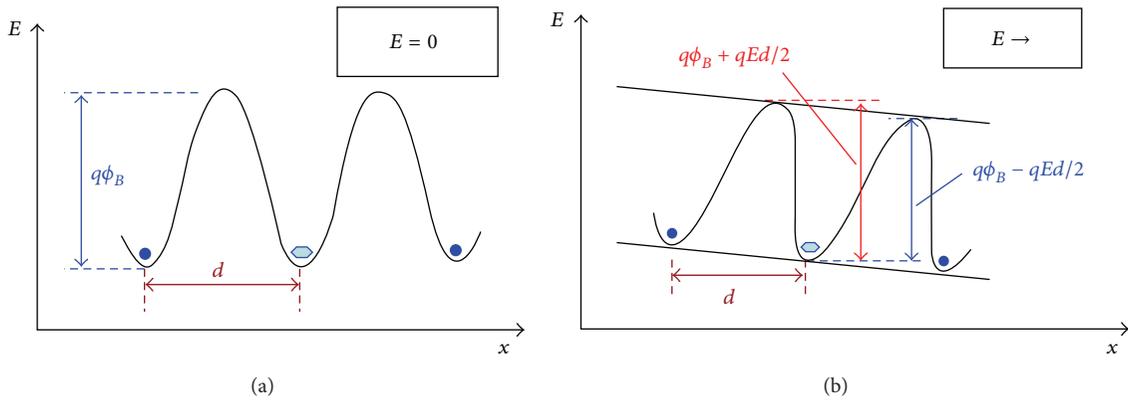


FIGURE 28: Energy band diagram of ionic conduction (a) without the applied electric field and (b) with the applied electric field. E is the applied electric field, d is the spacing between ionic sites, and $q\phi_B$ is the potential barrier height.

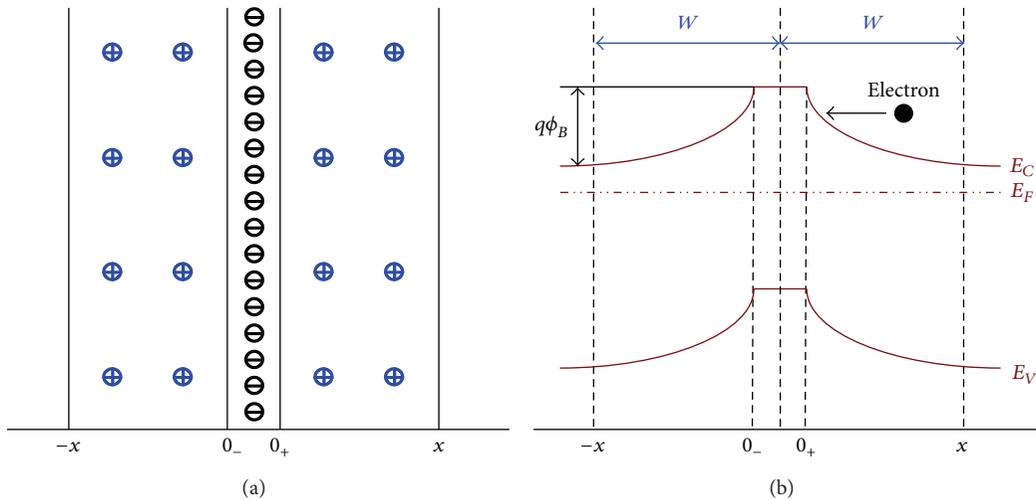


FIGURE 29: (a) The charge distribution of an electron trapping grain boundary and (b) the resulting potential energy barrier at the grain boundary. $q\phi_B$ is the potential barrier and W is the depletion width.

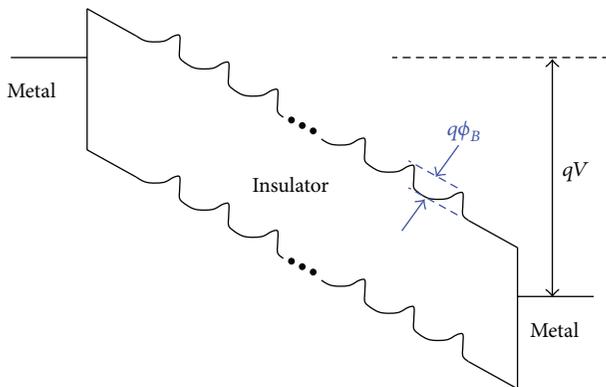


FIGURE 30: Schematic energy band diagram for grain-boundary-limited conduction in metal-insulator-metal structure.

mechanisms in dielectric films, that is, electrode-limited conduction mechanism and bulk-limited conduction mechanism. The most important parameter in the electrode-limited conduction mechanisms is the barrier height at the electrode-dielectric interface; meanwhile, the most important parameter in the bulk-limited conduction mechanisms is the trap energy level in dielectric films. During the analysis of conduction mechanisms, the dielectric constant is a key factor. For the case of thermionic emission process, the dielectric constant should be equal to the optical dielectric constant if the electron transit time is shorter than the dielectric relaxation time. Based on the electrode-limited conduction mechanisms, the physical properties of the barrier height at the electrode-dielectric interface and the effective mass of the conduction carriers in dielectric films can be obtained. Similarly, based on the bulk-limited conduction mechanisms, the physical properties of the trap level, the trap spacing, the trap density, the carrier drift mobility, the dielectric relaxation time, and the density of states of the conduction band in dielectric films can be determined. In general, the conduction mechanism in dielectric films may be influenced by the following factors: temperature, electric field, stress condition, device structure (MIS or MIM), electrode material, film species (SiO_2 , high-dielectric-constant material, or ferroelectric material), film thickness, deposition method, and so on. Because all the mentioned factors can affect the dielectric-electrode interface and/or the dielectric bulk property, all the factors are important in the studies of dielectric conduction mechanisms.

Conflict of Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

Acknowledgment

The author would like to thank the National Science Council of the Republic of China, Taiwan, for supporting this work under Contract no. NSC 102-2221-E-130-015-MY2.

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Research Article

Room-Temperature Voltage Stressing Effects on Resistive Switching of Conductive-Bridging RAM Cells with Cu-Doped SiO₂ Films

Jian-Yang Lin¹ and Bing-Xun Wang²

¹ Department of Electronic Engineering, National Yunlin University of Science and Technology, Douliou 64002, Taiwan

² Graduate School of Engineering Science & Technology, National Yunlin University of Science and Technology, Douliou 64002, Taiwan

Correspondence should be addressed to Jian-Yang Lin; linjy@yuntech.edu.tw

Received 3 October 2013; Revised 30 November 2013; Accepted 15 December 2013; Published 9 January 2014

Academic Editor: Fu-Chien Chiu

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SiO₂ or Cu-doped SiO₂ (Cu:SiO₂) insulating films combined with Cu or W upper electrodes were constructed on the W/Si substrates to form the conductive-bridging RAM (CB-RAM) cells. The CB-RAMs were then subjected to a constant-voltage stressing (CVS) at room temperature. The experimental results show that the room-temperature CVS treatment can effectively affect the current conduction behavior and stabilize the resistive switching of the memory cells. After the CVS, the current conduction mechanisms in the high resistance state during the set process of the Cu/Cu:SiO₂/W cell can be changed from Ohm's law and the space charge limited conduction to Ohm's law, the Schottky emission, and the space charge limited conduction. Presumably, it is due to the breakage of the conduction filaments during the CVS treatment that the conduction electrons cannot go back to the back electrode smoothly.

1. Introduction

As the charge storage memory is approaching its scaling limit [1], the next generation nonvolatile memory (NVM) technologies have been widely investigated in recent years. New types of NVMs include the resistive random access memory (RRAM), magnetic random access memory (MRAM), and the phase-change random access memory (PRAM). The conductive-bridging RAM (CB-RAM) is one of the RRAMs within which metal cations, such as copper or silver, can form conductive bridges or break the conduction filaments between the top and the bottom electrodes via ion migration. The CB-RAMs can be switched between the high resistance state (HRS) and the low resistance state (LRS) under different bias polarities [2, 3]. The insulating materials between the active electrode (e.g., Cu or Ag) and the inert electrode (e.g., W or Pt) play important roles in the resistive switching (RS) operation and are called the solid electrolytes. Several

kinds of the insulating materials, such as chalcogenide [4, 5], oxide-based [6–9], carbide [10], and amorphous silicon [11], have been used for the CB-RAMs. Among these materials, SiO₂-based films have advantages such as simple composition, no toxicity, compatibility with the COMS technology, and low cost. In addition, most of the resistive switching improvement works of the RRAMs were done at elevated temperatures [12–14]. There is no room-temperature process of Cu doping in oxide found in the literature. This work has tried to develop the room-temperature process of Cu doping into oxide following the constant-voltage stressing (CVS) treatment for the RRAM application. In this work, improvement on the switching characteristics of the SiO₂-based CB-RAM cells has been investigated with room-temperature constant-voltage stressing (CVS). The conduction mechanisms and the role of ion migrations in the resistive switching behavior of the conductive SiO₂-based films are also discussed.

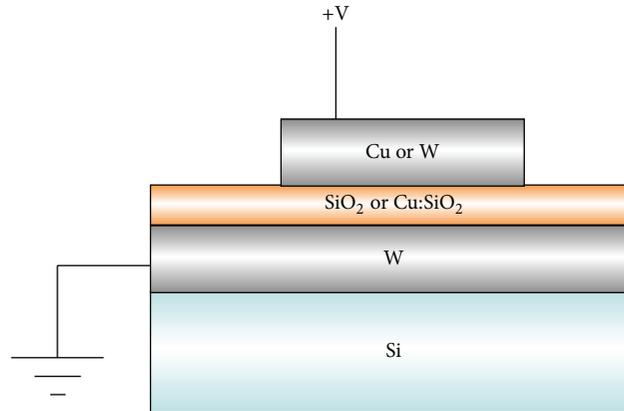


FIGURE 1: Schematic diagram of the CB-RAM cell.

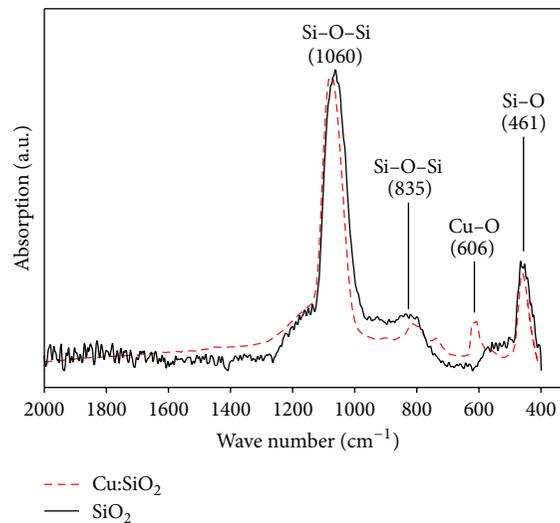


FIGURE 2: FTIR analysis of the deposited SiO₂ and Cu:SiO₂ films.

2. Experiment

In this work, SiO₂ or Cu-doped SiO₂ (Cu:SiO₂) insulating films combined with Cu or W top electrodes were constructed on the W/Si substrate to form the CB-RAM cell as shown in Figure 1. First, the tungsten (W) bottom electrode of 100 nm thickness was deposited onto the Si substrate by DC sputtering. Secondly, SiO₂ or Cu:SiO₂ films of 10 nm in thickness were deposited onto the W/Si substrates by RF sputtering. Then, the Cu or W top electrodes of 100 nm in thickness and 100 μ m in diameter were deposited by DC sputtering with metal mask. The elemental compositions of the as-deposited oxide films have been measured with the X-ray photoelectron spectroscopy (XPS). Analysis of the atomic percentage of the solid-electrolyte films will help the explanation of the resistive switching behavior. The molecular bonding of the oxide films was examined with the middle infrared Fourier transform infrared (FTIR) spectroscopy. The resistive switching characteristics of the SiO₂-based films before and after the electrical stress treatment were measured by the semiconductor parameter analyzer Agilent

4156C. The top electrode was applied with the bias voltage while the bottom electrode was grounded during the electrical measurement. In this work, the electrical CVS of the Cu/Cu:SiO₂/W cell was carried out at -1 V with stress time of 300 sec at room temperature.

3. Results and Discussion

The FTIR results of the as-deposited SiO₂ and Cu:SiO₂ films are shown in Figure 2. The Si-O-Si bonding and the Si-O bonding were observed at 1060 cm⁻¹, 835 cm⁻¹, and 461 cm⁻¹, respectively, in the SiO₂ film. For the Cu:SiO₂ film, there was additional Cu-O bonding appearing at 606 cm⁻¹. Besides, the intensity of the Si-O bonding of the Cu:SiO₂ film is lower than that of the SiO₂ film. It indicates that some of the Cu atoms have bonded with the oxygen atoms in the Cu:SiO₂ film. The bonding energy of the Si-O-Si becomes weaker after the Cu doping in the oxide. Therefore, the Si-O-Si signal of the SiO₂:Cu has shifted to higher wave numbers as compared to pure SiO₂ sample.

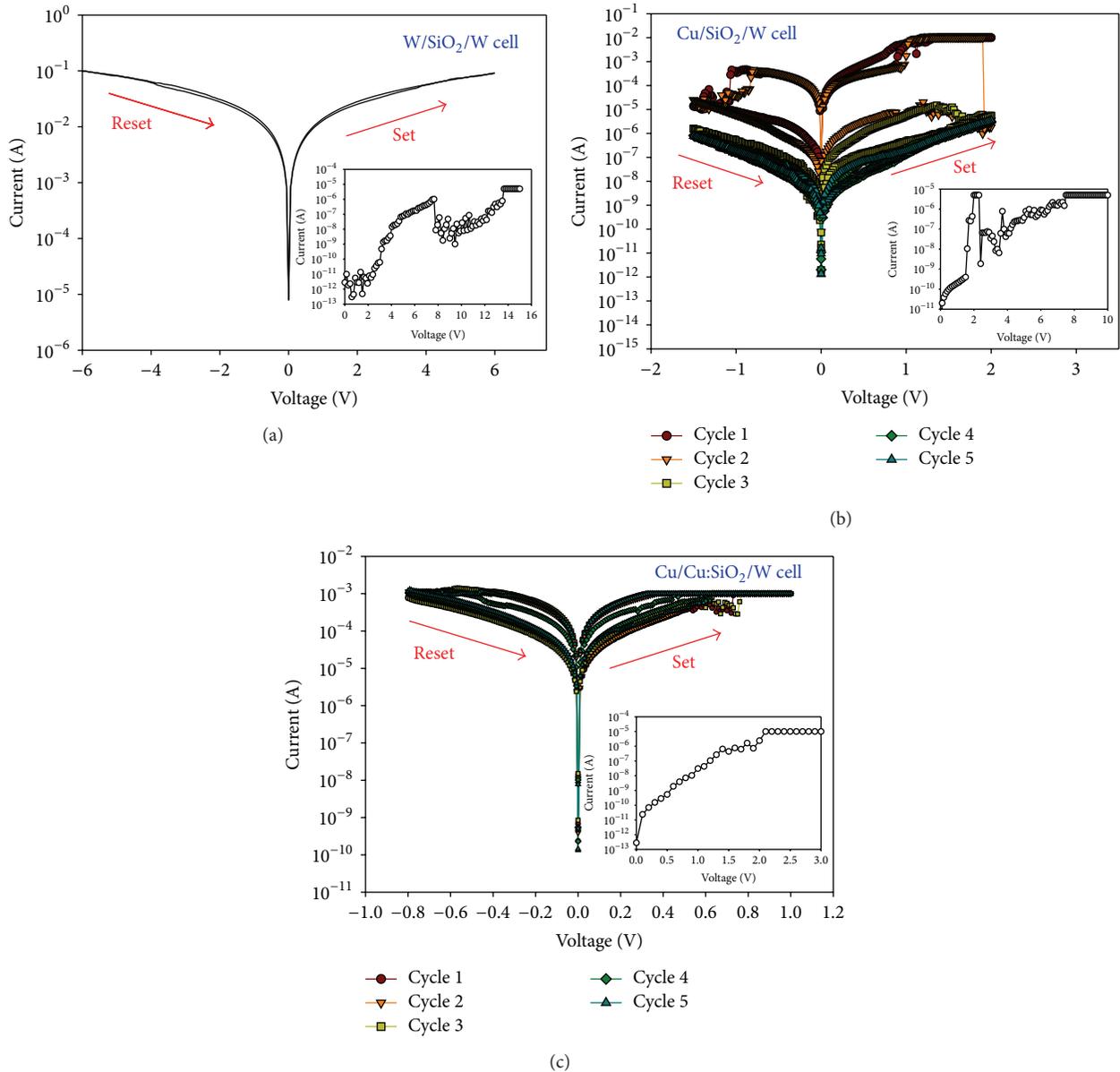


FIGURE 3: *I-V* characteristics of (a) W/SiO₂/W, (b) Cu/SiO₂/W, and (c) Cu/Cu:SiO₂/W cells.

Figure 3 shows the *I-V* characteristics of the W/SiO₂/W, the Cu/SiO₂/W, and the Cu/Cu:SiO₂/W cells, respectively, after the electrical forming process. In Figure 3(a), the W/SiO₂/W cell shows no resistive switching behavior after all. For the W/SiO₂/W device, the W atoms cannot be ionized by the applied electric field to form the conduction paths during the first forming process. After the soft breakdown, the oxide layer is completely damaged and cannot be recovered. That is why the W/SiO₂/W device shows high conductivity.

If the W top electrode is replaced by copper (Cu), the Cu/SiO₂/W cell exhibits the bipolar resistive switching between the HRS and the LRS, as shown in Figure 3(b). For the Cu/SiO₂/W device, the Cu atoms from the top electrode can be ionized by the applied electric field to form the conduction paths in the oxide layer during the forming

process. After the soft breakdown, the oxide layer is not damaged completely. As the Cu/SiO₂/W device is biased reversely, the Cu ions will go back to the Cu electrode forced by the applied electric field and the Cu conduction paths are broken. Therefore, the Cu/SiO₂/W device shows high resistance state. Consequently, replacing the W top electrode with Cu can improve the RRAM behavior. However, the Cu/SiO₂/W cell is not stable after continuous operation with DC sweeping cycles and the resistive switching will eventually go off.

Furthermore, Figure 3(c) shows that the bipolar resistive switching *I-V* characteristics of the Cu/Cu:SiO₂/W cell are more stable than those of the Cu/SiO₂/W cell. For the Cu/Cu:SiO₂/W RRAM device, the set voltage is 0.78 V with a set current of 0.9 mA, and the reset voltage is

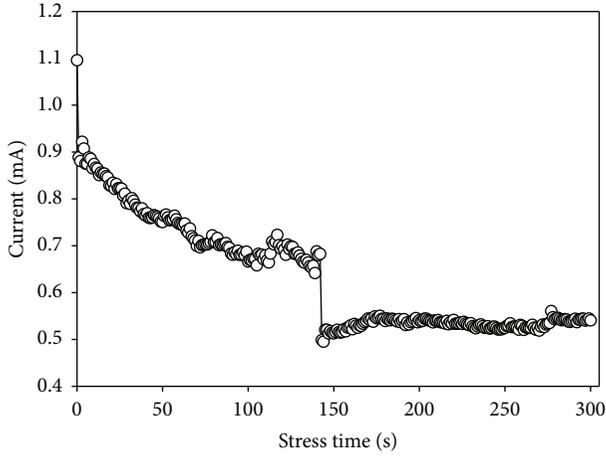


FIGURE 4: Constant-voltage stressing treatment of the Cu/Cu:SiO₂/W cell.

−0.75 V with a reset current of 1.0 mA. According to the XPS analysis results, the SiO₂ film has a Si:O ratio of 30.8 at.% : 69.1 at.%, while the Cu:SiO₂ film has a Cu:Si:O ratio of 6.22 at.% : 29.6 at.% : 64.18 at.%. These results indicate that the oxygen content is richer in SiO₂ film than in the Cu:SiO₂ film. When a positive bias is applied to the Cu electrode, the Cu ion (Cu⁺) will be generated and migrate towards the W electrode along the electric field in the SiO₂ film. The redox reaction will result in thin Cu connecting filaments in the SiO₂ film that exhibits the resistive switching behavior. At the same time, lots of oxygen ions (O[−]) will also be generated and migrate towards the Cu electrode and then recombine with the Cu ions. This will eventually cause the resistive switching behavior to go off. With the Cu:SiO₂ film, the Cu/Cu:SiO₂/W cell shows better stability in resistive switching because extra Cu atoms are doped in the SiO₂ film to effectively trap the extra oxygen ions avoiding the breakage of the Cu connecting filaments.

Figure 4 shows the condition of the CVS treatment to the Cu/Cu:SiO₂/W cell. The current value was slowly decreased with increased CVS time. During the electrical stressing, the current value decreases drastically at a CVS time of 140 sec. It can be attributed to the major breakage of the Cu conduction filaments. In this work, the Cu/SiO₂/W device is biased reversely during the DC stress treatment. The Cu ions will go back to the Cu top electrode forced by the applied electric field and the Cu filaments will be broken eventually.

Figure 5 shows the *I-V* characteristics of the Cu/Cu:SiO₂/W cells without and with the CVS treatment. It shows that the operation power of the cell can be reduced after the CVS treatment. Besides, the $R_{\text{HRS}}/R_{\text{LRS}}$ ratio is more stable after the CVS treatment that the resistive switching behavior of the cell can be enhanced by the CVS treatment. In the HRS during the set process of the Cu/Cu:SiO₂/W cell without the CVS treatment, two different conduction mechanisms, Ohm's law ($I \propto V$) and the trap-fill limited ($I \propto V^n$), are dominant, as shown in Figure 6(a). In the low bias regime, the injected carrier density is lower than the thermally generated carrier density that the Ohm's law conduction mechanism dominates

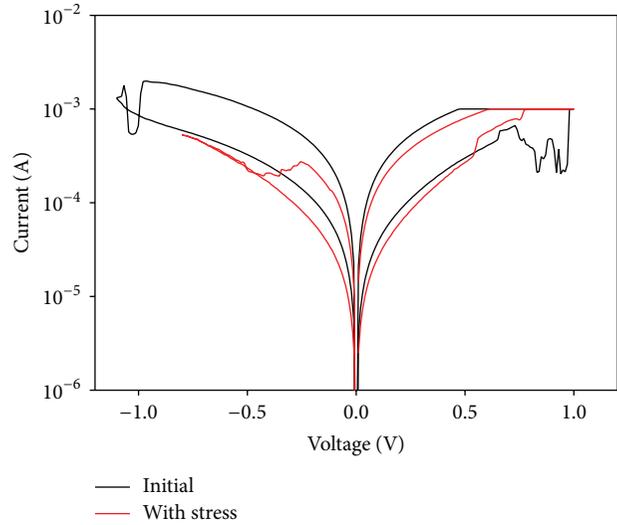


FIGURE 5: *I-V* characteristics of the Cu/Cu:SiO₂/W cells without and with CVS treatment.

the conduction behavior. However, in the high bias regime, the space charge limited conduction (SCLC) with trap model is dominant [15–20]. The SCLC characteristics include the Ohm's law, the trap-filled limit behavior, and the Child's law ($I \propto V^2$) [15, 16]. Figure 6(b) shows that the Cu/Cu:SiO₂/W cell after the CVS treatment has three different conduction mechanisms. In the low bias regime, the Ohm's law conduction mechanism is dominant. As the bias increases, the conduction mechanism changes to the Schottky emission mechanism ($\ln(I) \propto \ln(V^{1/2})$) in the middle bias regime (0.13–0.55 V). The transition of the conduction mechanism might be due to the breakage of the conduction filaments during the CVS treatment that the conduction electrons cannot go back to the back electrode smoothly. As the positive bias increases further to 0.56 V, the conduction current increases drastically. This might be attributed to the reconnection of several conduction filaments and the SCLC mechanism of Child's law is dominant in this regime [21].

In addition, the endurance characteristics of the Cu/Cu:SiO₂/W cell after the CVS treatment have been measured that, after 100 continuous switching cycles, the HRS/LRS ratio remains almost the same, as shown in Figure 7. For the Cu/Cu:SiO₂/W device, there are more Cu conduction filaments and the size of the Cu conduction filaments is larger before the CVS treatment. Some of the Cu filaments cannot be broken completely during the RESET process. Therefore, the RRAM behavior of the device is not stable enough. After the CVS treatment, both the number and the size of the Cu conduction filaments are reduced. The Cu/Cu:SiO₂/W device becomes easier to be operated between the SET and RESET processes so that the RRAM behavior of the device is improved. Therefore, the CVS treatment can effectively affect the current conduction behavior and stabilize the resistive switching of the CB-RAM cell.

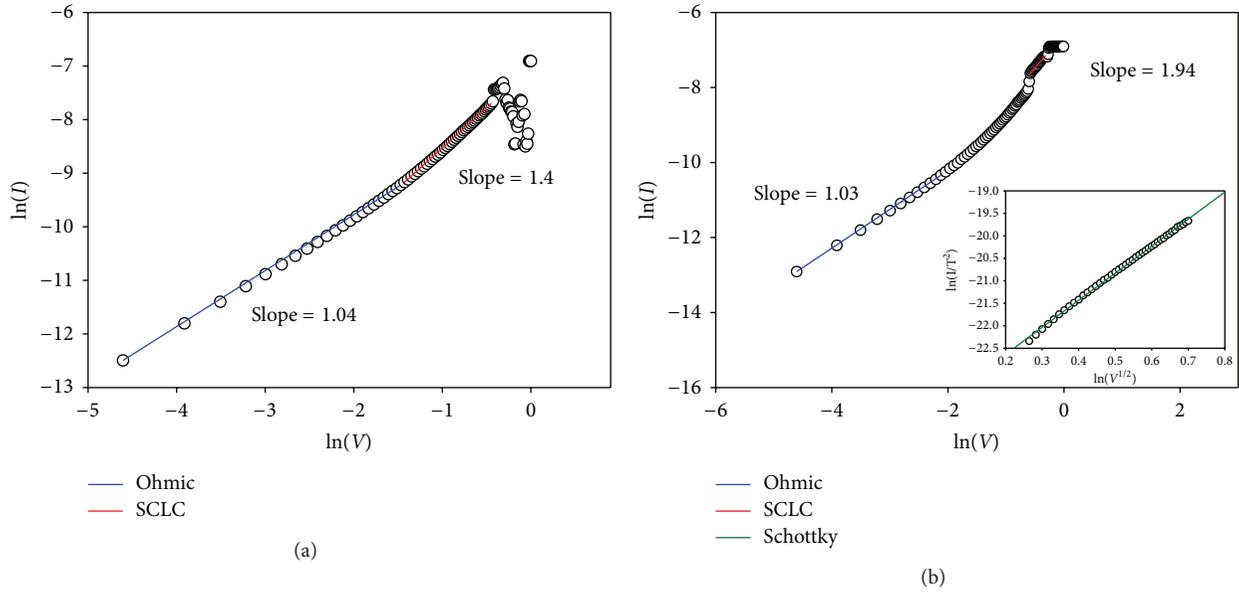


FIGURE 6: Current conduction mechanisms of the Cu/Cu:SiO₂/W cell: (a) without CVS treatment and (b) after CVS treatment.

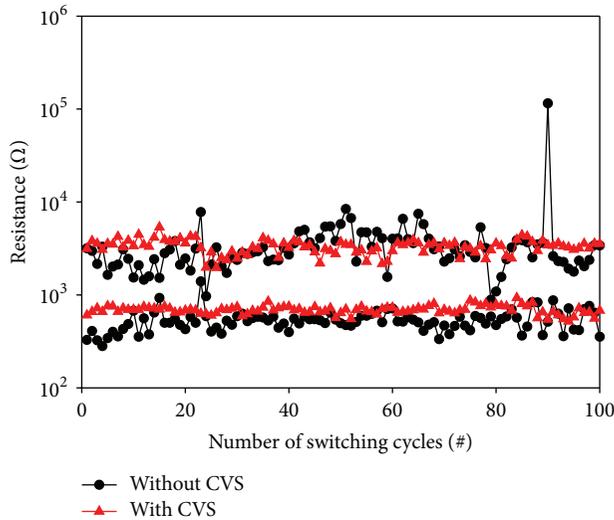


FIGURE 7: Endurance characteristics of the Cu/Cu:SiO₂/W cells without and with CVS treatment.

4. Conclusions

In this work, room-temperature CVS has been used to improve the bipolar resistive switching characteristics of the CB-RAMs with Cu:SiO₂ insulating film. After the CVS treatment, the current conduction mechanisms in the HRS during the set process of the Cu/Cu:SiO₂/W cell can be changed from Ohm’s law and SCLC to Ohm’s law, Schottky emission, and SCLC. Besides, the switching characteristics of the Cu/Cu:SiO₂/W memory cell exhibit a more stable R_{HRS}/R_{LRS} ratio due to the reduction of the conduction filaments. The room-temperature CVS treatment developed

in this work shows high potential to improve the operation performance of the CB-RAM cells.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgment

This work was financially supported by the National Science Council of the Republic of China under Contracts NSC101-2221-E-224-037 and NSC102-2221-E-224-074.

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Research Article

Bipolar Switching Characteristics of RRAM Cells with $\text{CaBi}_4\text{Ti}_4\text{O}_{15}$ Film

Jian-Yang Lin¹ and Chia-Lin Wu²

¹ Department of Electronic Engineering, National Yunlin University of Science and Technology, Douliou 64002, Taiwan

² Graduate School of Engineering Science & Technology, National Yunlin University of Science and Technology, Douliou 64002, Taiwan

Correspondence should be addressed to Jian-Yang Lin; linjy@yuntech.edu.tw

Received 4 October 2013; Revised 28 November 2013; Accepted 15 December 2013; Published 2 January 2014

Academic Editor: Fu-Chien Chiu

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The electrical conduction and bipolar switching properties of resistive random access memory (RRAM) cells with transparent calcium bismuth titanate ($\text{CaBi}_4\text{Ti}_4\text{O}_{15}$ —CBTi144) thin films were investigated. Experimentally, the (119)-oriented CBTi144 thin films were deposited onto the ITO/glass substrates by RF magnetron sputtering followed by rapid thermal annealing (RTA) at a temperature range of 450–550°C. The surface morphologies and crystal structures of the CBTi144 thin films were examined by using field-emission scanning electron microscopy and X-ray diffraction measurements. The on/off ratio and switching behaviors of the transparent Al/CBTi144/ITO/glass RRAM devices were further discussed in this work.

1. Introduction

Recently, various new nonvolatile memory devices were investigated, such as ferroelectric random access memory (FeRAM), resistive random access memory (RRAM), and phase change memory (PCM). Especially, the RRAM that composed of a simple metal-insulator-metal (MIM) structure has the advantages of low power consumption, high speed operation, good retention, and high-density integration capability [1–3]. Recent RRAM research includes perovskite oxides and metal oxides with different electrodes such as VO [4], $\text{Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$ [5], NiO [6], La_2O_3 [7], Dy_2O_3 [8], and ZnO [9].

Several perovskite materials, such as $\text{SrBi}_4\text{Ti}_4\text{O}_{15}$ (SBT) [10], $(\text{Ba}_{0.7}\text{Sr}_{0.3})(\text{Ti}_{0.9}\text{Zr}_{0.1})\text{O}_3$ [11], $\text{CaBi}_4\text{Ti}_4\text{O}_{15}$ (CBT) [12, 13], $\text{CaBi}_{4-x}\text{Nd}_x\text{Ti}_4\text{O}_{15}$ (CBNT) [14], and $\text{Ca}_{1-x}\text{La}_x\text{Bi}_4(\text{Ti}_{0.9}\text{W}_{0.1})_4\text{O}_{15}$ (CLBTW) [15], have been developed and investigated recently. Especially, the CBT film has high Curie temperature and low current density [16, 17]. In this study, we have investigated the bipolar resistive switching properties of the CBTi144 thin films in the metal-insulator-metal (MIM) structure for memory application.

2. Experiment

In this study, the CBTi144 thin films were deposited onto the ITO/glass substrates by RF magnetron sputtering with a ceramic CBTi144 target. Ceramic target of CBTi144 was prepared by conventional solid-state reaction technique. First, raw materials of Bi_2O_3 , CaO, and TiO_2 were weighted first according to the stoichiometric ratio of $\text{CaBi}_4\text{Ti}_4\text{O}_{15}$. After mixing of the raw materials, the mixed material was ball-milled for 5 h. The mixture was then dried and calcined at 1100°C for 4 h. Finally, the CBTi144 target was formed with a diameter of 2 inches. The CBTi144 films of 300 nm thickness were then deposited onto the ITO/glass substrates by RF magnetron sputtering with the CBTi144 target. The preparation conditions of the CBTi144 thin films are summarized in Table 1. To form the transparent MIM Al/CBTi144/ITO/glass RRAM device structure as shown in Figure 1, the top Al electrodes were patterned using a metal mask and deposited on top of the CBTi144 film by thermal evaporation. The phase and the surface morphology of the deposited CBTi144 films were characterized by X-ray diffraction (XRD) and field-emission scanning electron microscopy (FE-SEM). The

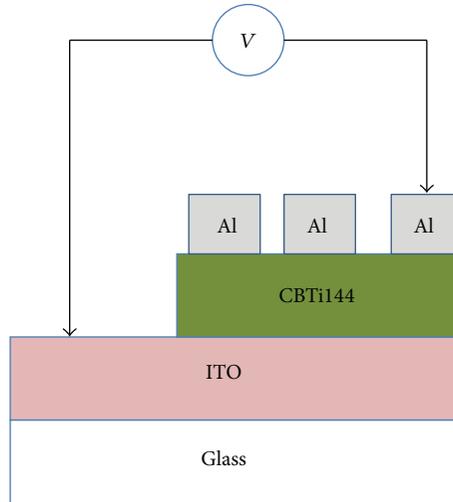


FIGURE 1: Metal-insulator-metal (MIM) capacitor structure of the CBTi144 RRAM device.

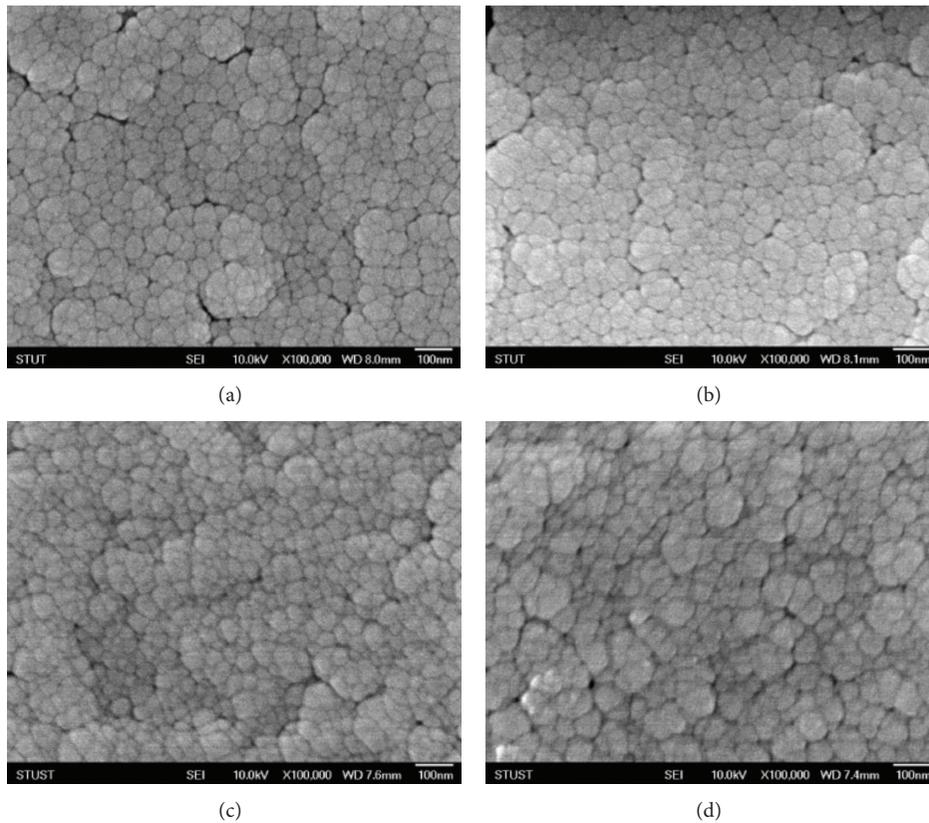


FIGURE 2: Surface morphologies of the CBTi144 films with (a) no annealing, (b) 450°C RTA, (c) 500°C RTA, and (d) 550°C RTA.

leakage current characteristics of the CBTi144 thin films were measured by a gain phase analyzer (HP4156C).

3. Results and Discussion

Figure 2 shows the FE-SEM micrographs of the CBTi144 thin films without annealing and with rapid thermal annealing (RTA) at 450, 500, and 550°C. As the annealing temperature is

increased, the grain size of the CBTi144 film slightly increases and the porosity of the CBTi144 film decreases because the oxygen vacancy concentration in the CBTi144 film decreases [18].

Figure 3 shows the XRD patterns of the CBTi144 thin films without and with 450–550°C RTA. The XRD patterns were used to identify the changes on crystalline structures of annealed CBT thin films. The results of the XRD analysis

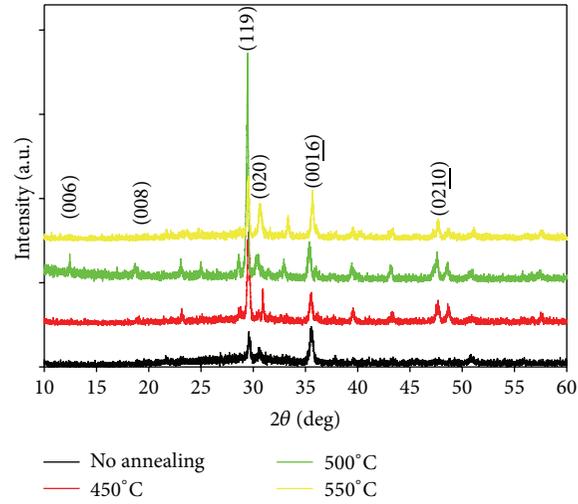


FIGURE 3: XRD patterns of the CBTi144 thin films with different annealing temperatures.

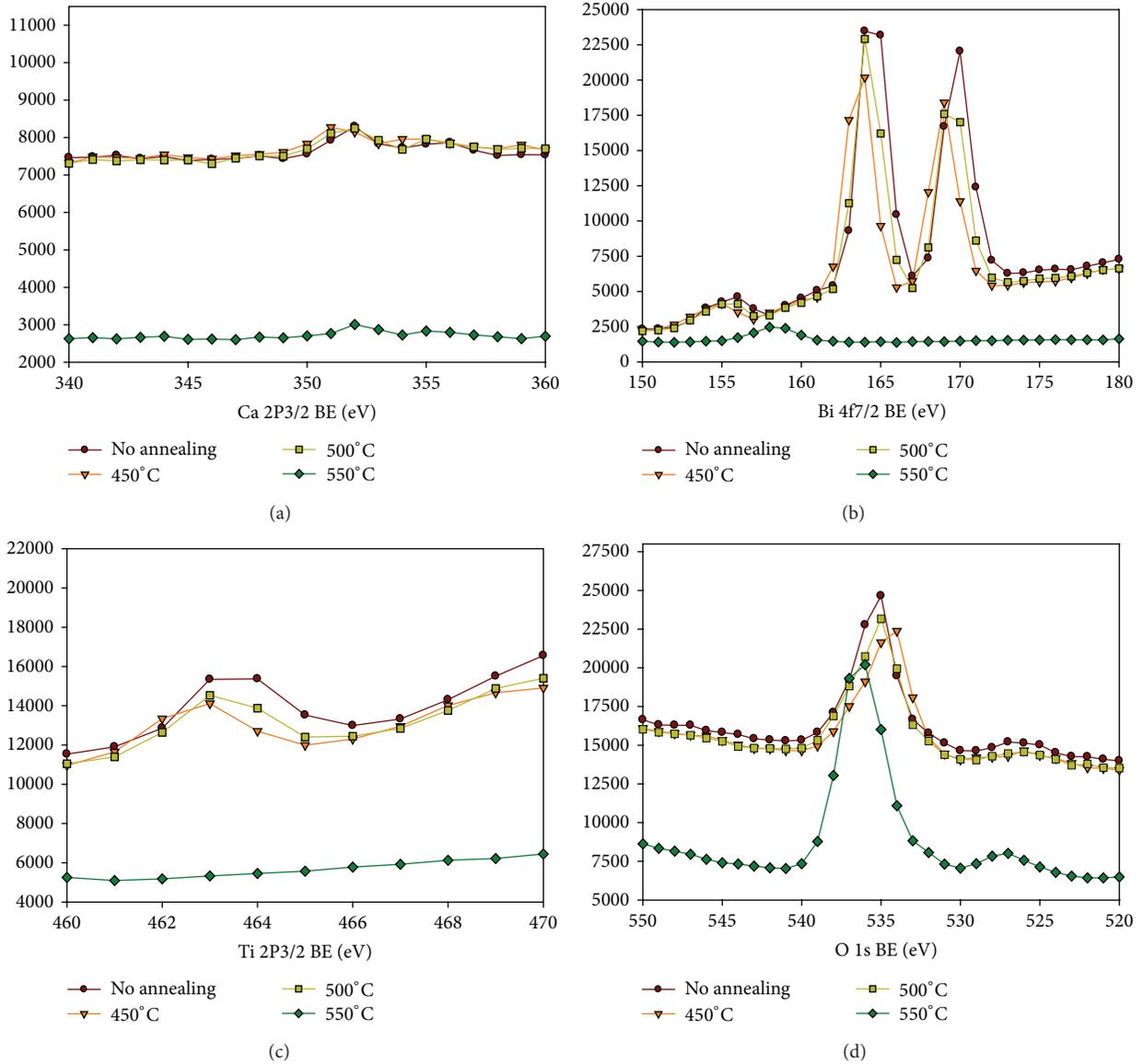


FIGURE 4: XPS of the CBTi144 thin films with different annealing temperatures: (a) Ca 2p_{3/2}, (b) Bi 4f_{7/2}, (c) Ti 2p_{3/2}, and (d) O 1s.

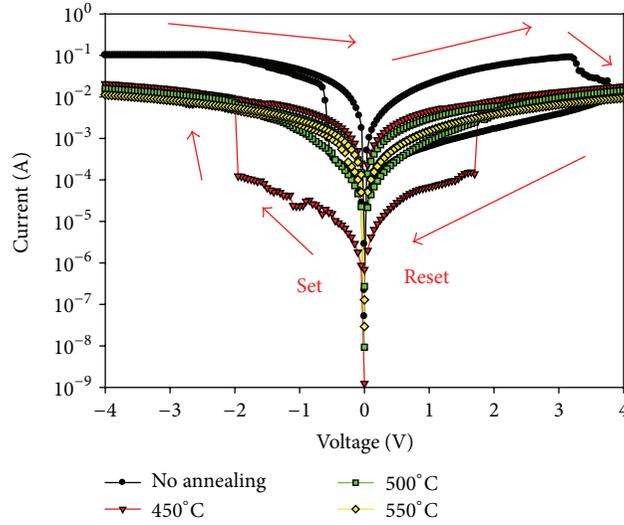


FIGURE 5: *I-V* characteristics of the CBTi144 RRAM cell without and with 450–550°C RTA.

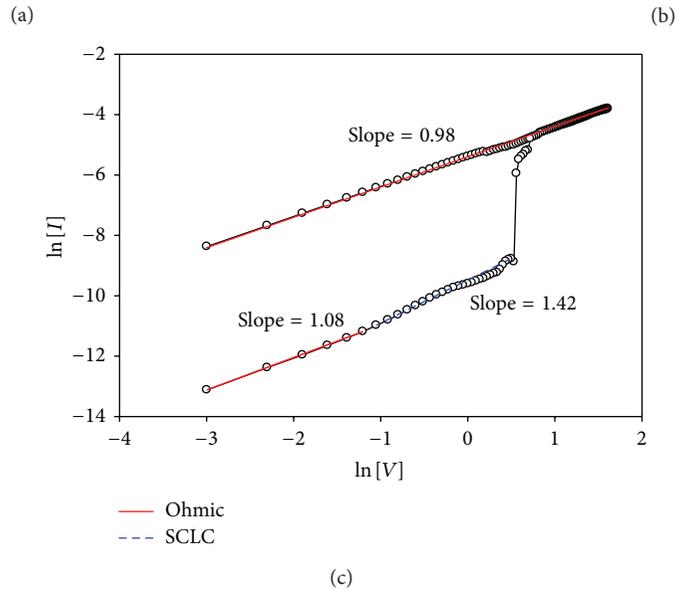
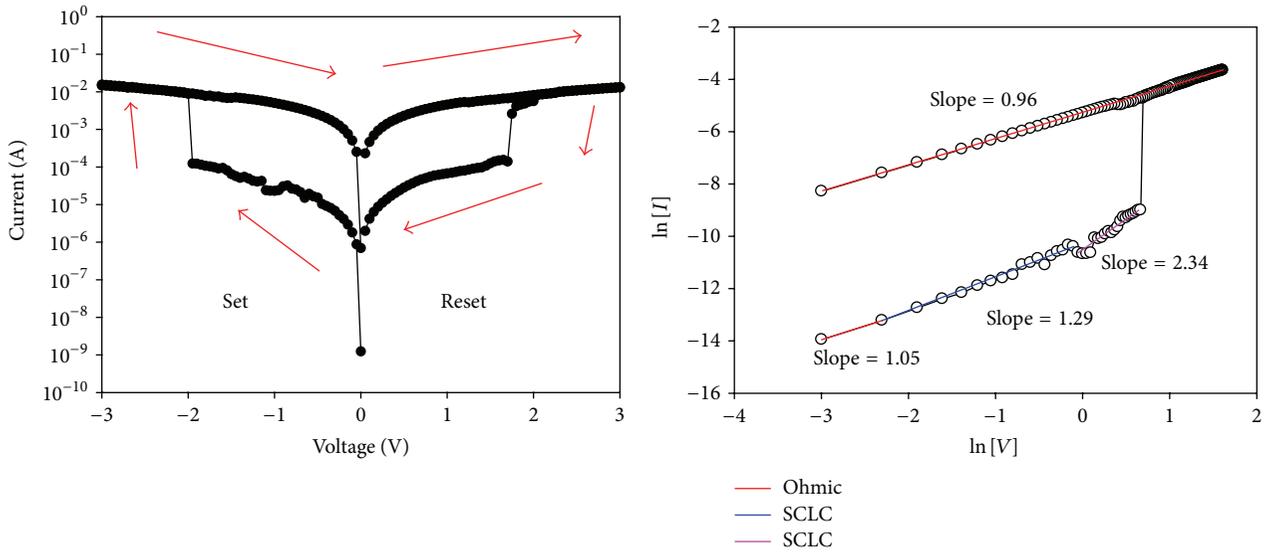


FIGURE 6: Current conduction mechanisms of the Al/CBTi144/ITO/glass RRAM cell annealed at 450°C: (a) in the entire switching operation, (b) during the Set process, and (c) during the Reset process.

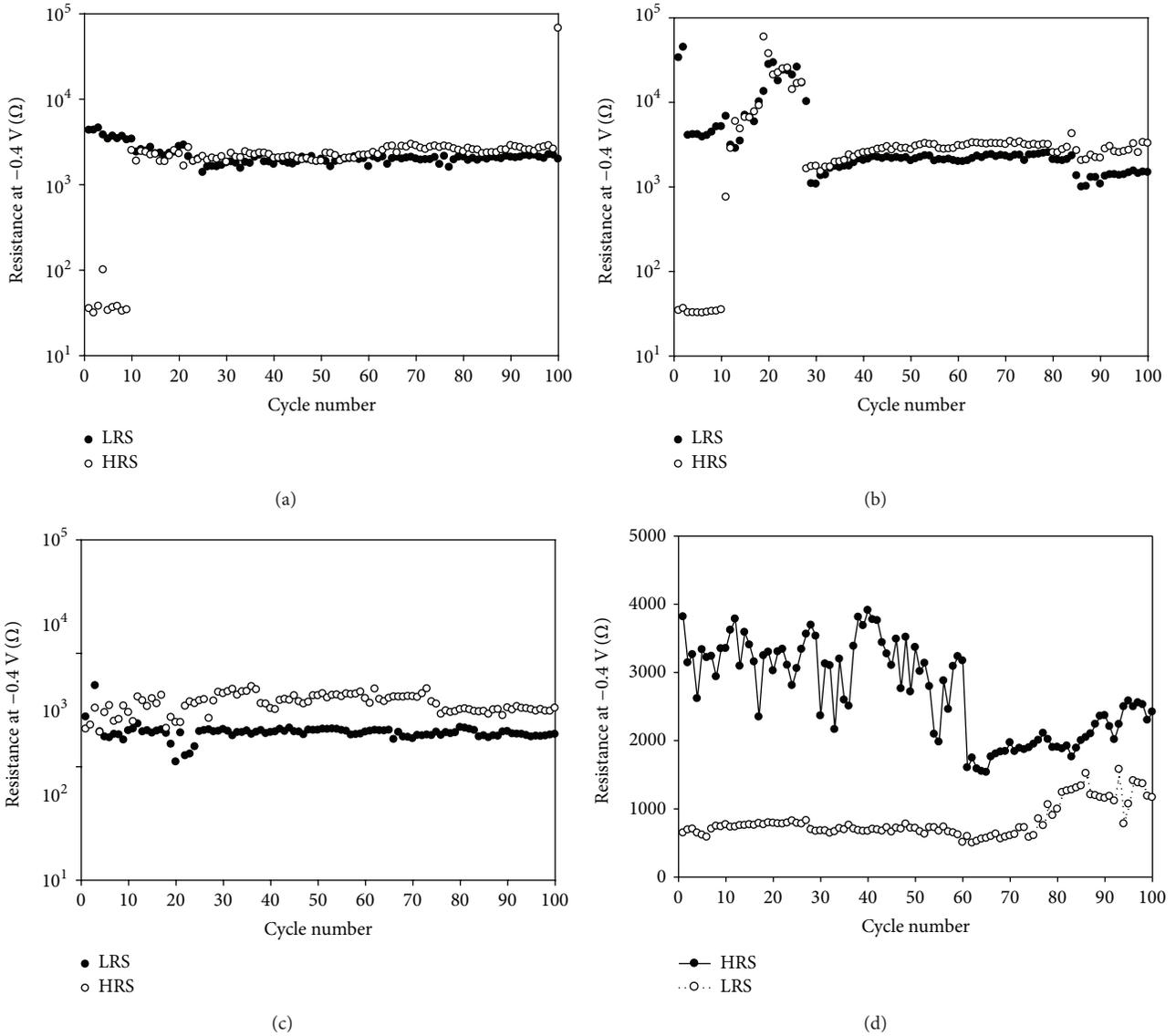


FIGURE 7: Endurance test of the Al/CBT/ITO/glass cell with different CBT annealing conditions: (a) as-deposited, (b) 450°C annealed, (c) 500°C annealed, and (d) 550°C annealed.

show that the CBT films are of polycrystalline and the peaks of the XRD patterns correspond to the (006), (008), (119), (2010), and (220) orientations of the perovskite crystal [19]. As the annealing is increased, most of the intensities of the XRD peaks increase. This indicates that the grain sizes of the CBT films increase with the RTA temperature.

Figure 4 shows the XPS analysis of the CBTi144 thin films with different annealing conditions. It is noted that the amounts of all the compositional elements in the CBT films decrease as the annealing temperature increases. The oxygen content decreases slightly for the cases of 450°C and 500°C annealing that the oxygen vacancies may increase accordingly. However, as the annealing temperature increased to 550°C which is close to the melting point of the glass substrate, the oxygen content decreases drastically presumably due to the increased stress between the CBT film and the ITO/glass substrate.

Figure 5 shows the current-voltage (*I-V*) characteristics of the CBTi144 thin films without and with 450–550°C RTA. From the *I-V* measurement, the CBTi144 thin films show good nonvolatile resistive switching properties. The transport current of the CBTi144 thin film increases as the RTA temperature increases up to 450°C. However, the transport current of the CBTi144 films will decrease if the RTA temperature is increased to 500°C and 550°C. When the annealing temperature increases, the concentration of the oxygen vacancies in the CBTi144 thin film reduces that the bipolar resistive switching characteristics of the CBTi144 RRAM structure will deteriorate.

Figure 6(a) shows the *I-V* characteristics of the transparent Al/CBTi144/ITO/glass RRAM cell exhibiting bipolar resistive switching behavior with different conduction mechanisms during the switching operation. With RTA temperature of 450°C, the *I-V* characteristics of the CBTi144 RRAM

TABLE 1

Target diameter (inch)	2
Substrate temperature (°C)	30
RF power (W)	100
Chamber pressure (mTorr)	20
Oxygen concentration (%)	0
Deposition time (h)	2
Annealing temperature (°C)	450–550

cell exhibit large on/off ratio over 100 at a bias voltage of 0.1 V. There are two conduction mechanisms, the Ohm's law (I/V) and the trap-filled limit (I/V_n), dominant during the Set process of the RRAM cell, as shown in Figure 6(b). The thermally generated carrier density is higher than the injected carrier density in the low bias regime [7, 8]. Therefore, the Ohm's law mechanism dominates the conduction behavior in the low bias regime. The SCLC characteristics include the Ohm's law ($I \propto V$), the trap-filled limit behavior, and the Child's law ($I \propto V^2$) [7, 8]. However, the HRS has two kinds of conduction mechanisms in the high bias regime where the trap model with space-charge-limited conduction (SCLC) is dominant [20]. Figure 6(c) shows the current conduction mechanisms during the Reset process of the RRAM cell. In the LRS and HRS, the Reset process has similar conduction mechanisms to the Set process.

Figure 7 shows the endurance characteristics of the Al/CBT/ITO/glass cells with different annealing conditions. For the case of 450°C annealing as shown in Figure 7(b), the endurance characteristics of the cell in the first 10 continuous switching cycles still show an HRS/LRS ratio of 100. But after 10 continuous switching cycles, the cell shows an unstable HRS/LRS ratio. For the case of 500°C and 550°C annealing as shown in Figures 7(c) and 7(d), the HRS/LRS ratio is even degraded. It is mainly because of the large reduction in oxygen content at higher annealing temperatures that the cell cannot switch properly in the HRS and LRS.

4. Conclusions

In this work, the resistive switching behavior of the transparent Al/CBTi144/ITO/glass RRAM cells has been investigated. Our results show that the conduction switching behavior of the CBTi144 RRAM cells is of bipolar switching. The current conduction mechanisms of the CBTi144 RRAM cells have also been discussed in this work.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

This work was financially supported by the National Science Council of the Republic of China under Contracts NSC101-2221-E-224-037 and NSC102-2221-E-224-074. The authors

would like to thank the National Nano Device Laboratories for the measurement support.

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Research Article

Comparison of H₂ and NH₃ Treatments for Copper Interconnects

Yu-Min Chang,¹ Jihperng Leu,¹ Bing-Hong Lin,² Ying-Lung Wang,² and Yi-Lung Cheng²

¹ Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 30013, Taiwan

² Department of Electrical Engineering, National Chi Nan University, Nantou 54561, Taiwan

Correspondence should be addressed to Yi-Lung Cheng; yjcheng@ncnu.edu.tw

Received 2 September 2013; Accepted 20 November 2013

Academic Editor: Chun-Hsing Shih

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The surface state, electrical, and reliability characteristics of copper (Cu) interconnects after ammonia (NH₃) or hydrogen (H₂) plasma treatment were investigated in this study. The experimental results show that H₂ plasma treatment has excellent Cu oxide removal efficiency, less impact on the formation of Cu hillocks, and less damage on low-dielectric constant (low-*k*) dielectrics in comparison to NH₃ plasma treatment. However, H₂ plasma treatment results in a higher leakage current between the Cu lines and shorter electromigration (EM) failure time due to a weaker adhesion strength at the Cu film interface. On the other hand, NH₃ plasma treatment without the sufficient treatment time would lead to an increased probability of delamination at the Cu/barrier layer interface since the Cu oxide layer can not be completely removed. As a result, extending NH₃ plasma treatment time can efficiently reduce the adhesion failure and enlarge EM resistance as well.

1. Introduction

Owing to the downscaling of devices to the deep sub-micrometer level, the resistance capacitance (RC) delay of interconnects is playing an increasingly important role in determining the performance of an integrated circuit. To reduce this effect, Cu has been used as an interconnect metallization material in deep submicron technology because of its lower resistivity and higher electromigration resistance [1–3]. However, since Cu is easily oxidized and diffused rapidly into interlayer dielectrics (ILD, SiO₂, or low-*k* dielectrics), a diffusion barrier film (SiN, SiC, or SiCN) is required in Cu metallization systems to prevent Cu diffusion [3–7].

However, in a real Cu and low-*k* dielectric dual damascene process, Cu can be oxidized by exposure to air before the diffusion barrier is deposited. Thus the formed Cu oxide layer negatively affects the electrical performance and reliability of devices [8, 9]. Therefore, a chemical reaction to remove this native Cu oxide is required before the barrier layer is deposited to improve the adhesion between the Cu film and the barrier layer. NH₃ and H₂ plasma treatments are used in current Cu metallization as both generate H species,

which can remove the Cu oxide layer from the Cu surface by an oxidation-reduction reaction [10]. Many studies have investigated the effects of NH₃ and H₂ plasma treatments on EM lifetime [11–13]. All such studies have revealed that these plasma treatments improve EM reliability of Cu lines. However, NH₃ and H₂ plasma treatments have also been reported to have opposite effects [11, 13]. Additionally, the effect of interface conditions on EM reliability is still unclear.

This study investigates the Cu surface state and physical properties after NH₃ or H₂ plasma treatment. Additionally, electrical results of the pattern wafers with dual-damascene structures were evaluated and compared. Finally, the effect of various plasma treatment conditions on EM reliability performance was studied.

2. Experimental

Blanket Wafer. A film stack of SiN/Cu/TaN/SiO₂/Si (substrate) was prepared in a clean room for this study. First, a 200 nm thick thermal SiO₂ film was deposited on a blanket Si substrate. Next, a 30 nm-thick TaN layer was deposited by physical vapor deposition (PVD) to improve the adhesion

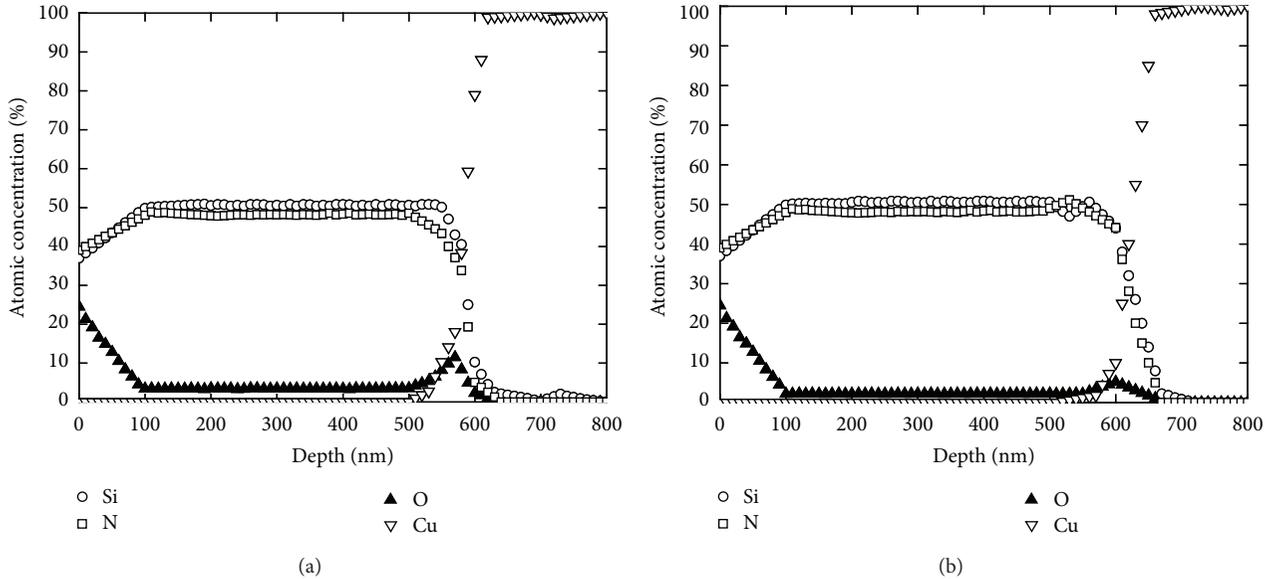


FIGURE 1: AES depth profile of Si, N, O, and Cu atomic concentrations in the Cu/SiN multilayer structures (a) without plasma treatment and (b) with 30 s NH_3 plasma treatment.

between Cu layer and SiO_2 film, followed by PVD Cu layer used as a seed layer with a thickness of 160 nm. A $1.3 \mu\text{m}$ thick electroplated Cu film was subsequently grown. Chemical mechanical polishing (CMP) was then performed to remove the top portion ($\sim 0.4 \mu\text{m}$ -thick) of the Cu layer. Then, the post-CMP clean using citric acid was used to remove the backside Cu contamination. Finally, a 50 nm-thick barrier layer of SiN was deposited in a plasma-enhanced chemical vapor deposition (PECVD) system. Before SiN film deposition, two kinds of plasma treatment (NH_3 and H_2) were conducted in the same PECVD chamber. The plasma treatment temperature were kept at 350°C , with a rf power of 300 W, pressure of 4.2 Torr, and gas flow of 300 sccm (cubic centimeter per minute at STP).

Elemental analysis was carried out using depth-profile Auger electron spectroscopy (AES) to check the oxygen (O) concentrations between Cu film and the barrier layer (SiN). The Cu oxide removal efficiency by NH_3 or H_2 plasma treatment was determined by measuring the Cu reflectance related to silicon substrate using ellipsometer. O_2 plasma was treated on the post-CMP cleaning Cu wafer to form the Cu oxide layer. Then, NH_3 or H_2 plasma treatment with various times was performed to evaluate the reflectance change of Cu film. X-ray photoelectron spectroscopy (XPS) analysis was used to measure the bonding structure of the Cu film. The adhesion ability was measured by stud-pull method.

Pattern Wafer. Three-layer metallization was fabricated based on Cu dual-damascene technology. The dielectric material used here was PECVD SiCOH film with the dielectric constant of 2.8. After completing Cu CMP process, the plasma treatment using NH_3 or H_2 gas and the deposition of SiN barrier layer were subsequently performed and then followed by the dual-damascene dielectric deposition, photo, etch, and Cu processes to complete the next interdielectric

layer. The fabricated pattern wafers were inspected using optical microscopy (OM) and scanning electron microscopy (SEM). The leakage current was monitored on a 0.1 m long serpentine/comb structure with a $0.20 \mu\text{m}$ line-width and line-to-line space. EM testing was carried out on via-line contact configuration, with a length of $250 \mu\text{m}$ and a width of $0.20 \mu\text{m}$. The stress temperature and current density were 350°C and $1.5 \text{ MA}/\text{cm}^2$, respectively. The failure criterion was a 10% relative increase in resistance.

3. Results and Discussion

AES depth-profile analyses were performed to determine the concentration of oxygen at the interface between the Cu film and the barrier layer. Figures 1(a) and 1(b) present the elemental concentrations of Si, N, O, and Cu in the multilayer structures without plasma treatment and with 30 s NH_3 plasma treatment. The interface between the Cu film and the barrier layer in the untreated sample yielded a significant oxygen peak ($\sim 10.8\%$ atomic concentration). Plasma treatment clearly lowered the oxygen peak as shown in Figure 1(b). Figure 2 presents the dependence of oxygen atomic concentration on the treatment time for H_2 and NH_3 plasma treatments. H_2 plasma treatment for 5 s sharply reduced the oxygen atomic concentration to $\sim 2\%$. Under the NH_3 plasma treatment condition, the oxygen atomic concentration decreases as the treatment time increases, reaching a saturated value of $\sim 2\%$ after 30 s of treatment. This result reveals that H_2 plasma treatment yields a higher Cu oxide removal efficiency than NH_3 plasma treatment within the initial period of plasma treatment. A possible cause is that more hydrogen species are generated in the H_2 plasma environment because the dissociation energy of H-H bonds is lower. At longer plasma treatment times ($>30 \text{ s}$), NH_3 and

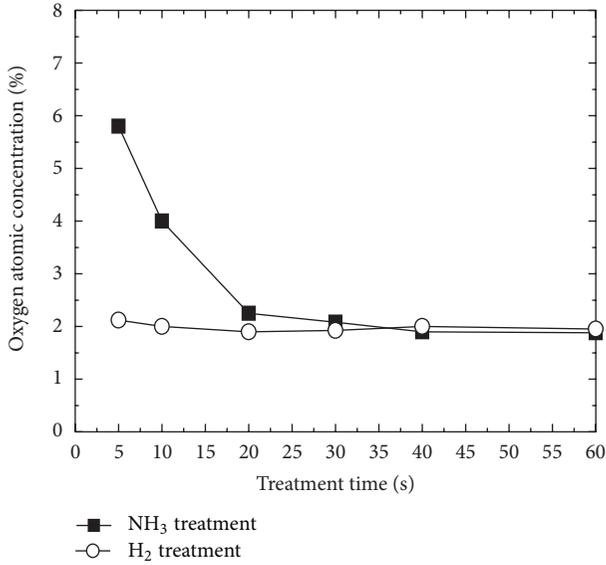


FIGURE 2: Oxygen atomic concentration at the Cu/SiN interface for H₂ and NH₃ plasma treatments as a function of treatment time.

H₂ plasma treatments exhibit a similar Cu oxide removal performance.

To evaluate Cu oxide removal efficiency rapidly, we developed a new method by measuring the Cu reflectance at a wavelength of 480 nm. As the Cu surface was oxidized, the Cu reflectance decreased. Accordingly, the percentage change in the Cu reflectance (*R*%) was calculated by treating the oxidized Cu film with H₂ or NH₃ gas plasma, according to the following expression:

$$R\% = \frac{Cu_{Ri} - Cu_{RO}}{Cu_{RCMP}} \quad (1)$$

where *Cu_{RI}*, *Cu_{RO}*, and *Cu_{RCMP}* denote the Cu reflectance after H₂ or NH₃ gas plasma treatment, O₂ gas treatment, and post-CMP cleaning, respectively. This percentage change in Cu reflectance is an index of Cu oxide removal efficiency. A larger value means a higher Cu oxide removal efficiency. Figure 3 compares the effectiveness of H₂ and NH₃ plasma treatments with various durations. The result is similar to that obtained from AES analyses. For a short treatment duration (<20 s), H₂ plasma treatment causes higher percentage change in Cu reflectance as compared to NH₃ plasma treatment, reflecting a higher Cu oxide removal efficiency. Additionally, as the NH₃ treatment time increases to 30 s, the Cu oxide removal efficiency reaches a value similar to that of H₂ plasma treatment. However, as the NH₃ treatment time is further increased beyond 40 s, the percentage change in Cu reflectance decreases. The results of XPS analysis, shown in Figure 4, suggest that this decline is a result of the formation of Cu–N bonds in a NH₃ plasma environment. No Cu–N bond was detected in the H₂ treated and untreated samples.

Figure 5 plots the adhesion strength between the Cu film and the barrier layer under various treatment conditions obtained from the blanket wafer. Five points were measured under each condition to ensure reliability. As shown, the

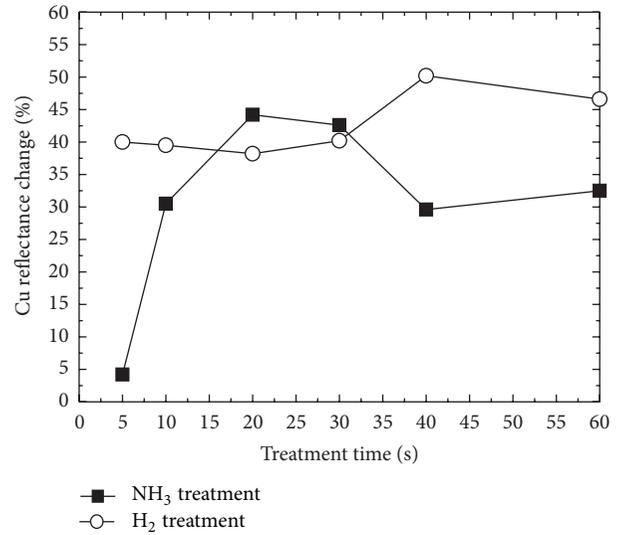


FIGURE 3: Percentage change in Cu resistance on the oxidized Cu surface for H₂ and NH₃ plasma treatments as a function of treatment time.

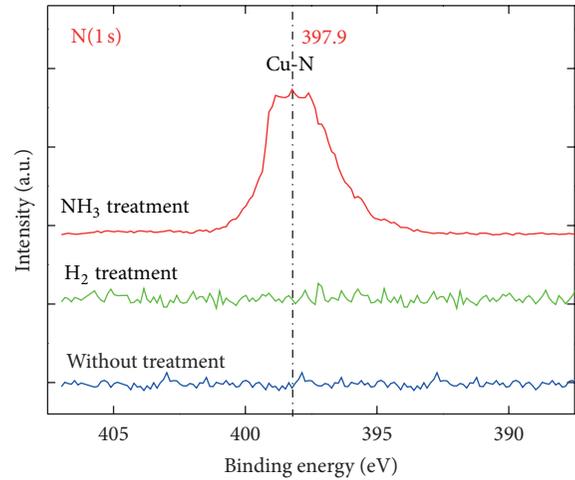


FIGURE 4: N (1s) XPS spectra for different plasma treatments on the Cu surface.

tested sample with NH₃ plasma treatment for a shorter time (10 s) exhibits weaker adhesion than that with H₂ plasma treatment. The reduced adhesion in 10 s NH₃ plasma treated sample is probably due to the remaining Cu oxide at the Cu surface. Increasing the treatment time to 30 s improves the adhesion. Moreover, the tested sample with 30 s NH₃ treatment had a higher adhesion strength than the H₂-treated sample because the former treatment forms Cu–N chemical bonds [14, 15]. The adhesion strength between the Cu film and the barrier layer in H₂-treated samples did not vary significantly with the treatment time.

Following the CMP process, the pattern wafers were conducted with the various plasma treatment conditions before the barrier film was deposited. After completing

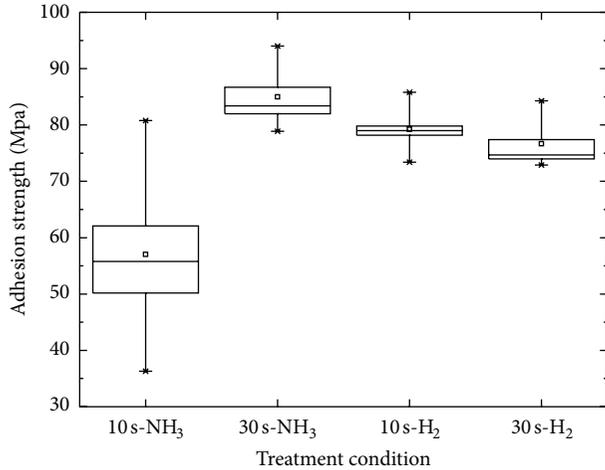
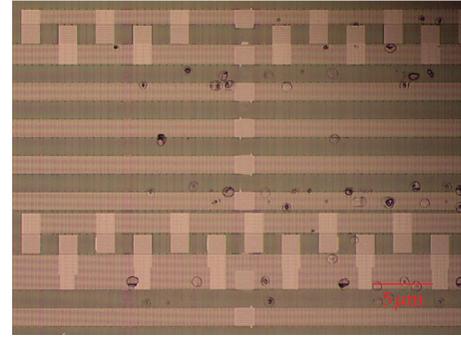


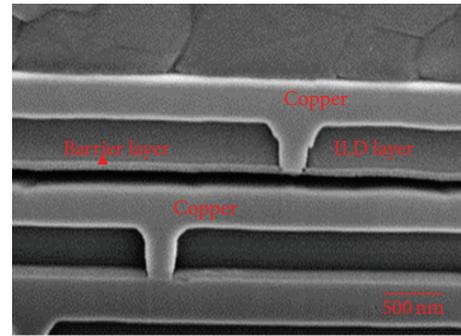
FIGURE 5: Adhesion strength at the Cu/SiN interface for various plasma treatment conditions.

three-layer metallization, these pattern wafers were thermal annealed for 1 h at 425°C with seven cycles. An OM inspection was performed to check the pattern wafers for 25 sites. The NH₃ plasma treatment with short duration (<20 s) produced some bubble-like defects on the Cu lines, as presented in Figure 6(a). These bubble-like defects were examined by SEM, revealing that the delamination occurred at the interface between the Cu layer and the barrier layer, as displayed in Figure 6(b). Figure 7 summarizes the probability of formation of bubble-like defects under NH₃ and H₂ plasma treatments as a function of the treatment time. The probability of formation of bubble-like defects is zero independently of the duration of H₂ plasma treatment. However, the probability is strongly correlated with the duration of NH₃ treatment. The probabilities of formation of bubble-like defects in the treated samples with NH₃ treatment for 5 s and 30 s were ~80 and ~36%, respectively, decreasing to 0% as the treatment time exceeded 20 s. Interestingly, the trend in the probability of bubble-like defect formation with treatment time is consistent with the removal rate of Cu oxide layer from the Cu surface. Based on the above results, the sufficient removal of Cu oxide layer from the Cu surface is critical in the fabrication of high-quality Cu interconnects.

Hillocks are easily formed on a Cu surface in a thermal-plasma environment and this formation must be minimized. A previous study [16] pointed out that the formation of Cu hillocks is related to the thermal budget. This study also demonstrates that the density of Cu hillocks increases with treatment time. However, different plasma gases produce different amounts of Cu hillocks. For a fixed treatment time of 30 s, the density of Cu hillocks in the H₂-treated sample (Figure 8(a)) is much lower than that in the NH₃-treated sample (Figure 8(b)), suggesting that the reactant gas also contributes to the formation of Cu hillocks. The reduction of Cu hillock formation by H₂ gas involves two mechanisms. In the first, H₂ gas donates more reactive H species, which chemically react with Cu lines. NH₃ gas provides more physical sputtering due to N radicals. The other mechanism



(a)



(b)

FIGURE 6: (a) OM image of bubble-like defects; (b) cross-section SEM images of a bubble defect.

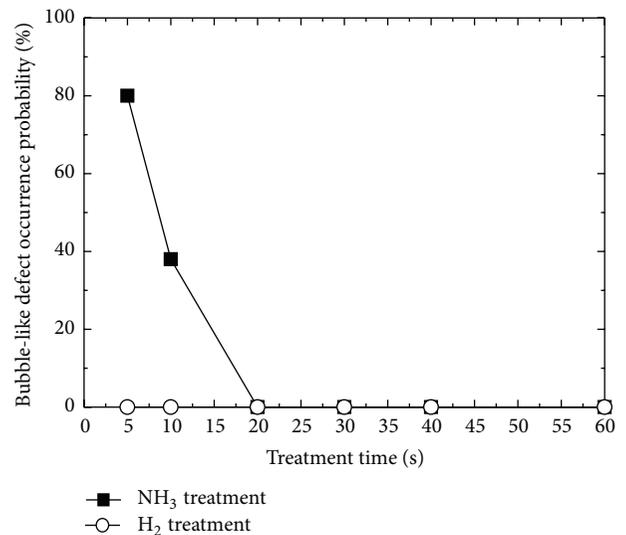


FIGURE 7: Probability of bubble-like defects formation under NH₃ and H₂ plasma treatments as a function of the treatment time.

is that H₂ gas has a better thermal conductive coefficient, resulting in a better heat transfer between the Cu surface and the H₂ molecules.

In a standard Cu dual-damascene architecture, not only the Cu surface but also the neighboring low-*k* ILD are exposed to the plasma environment. Therefore, the effect of

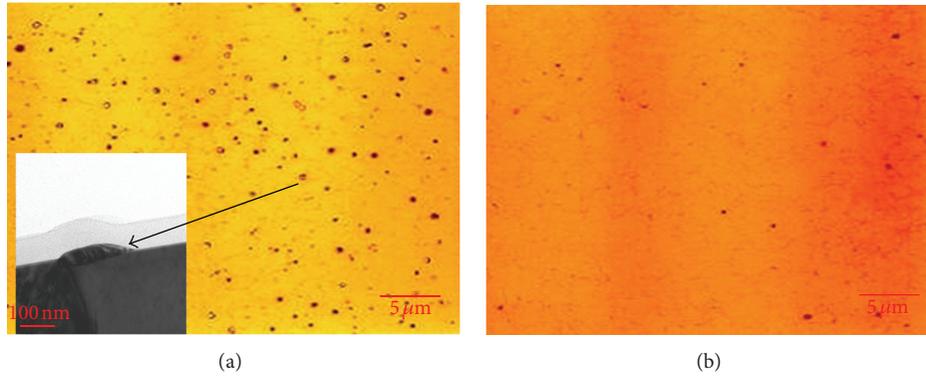


FIGURE 8: OM images of Cu hillocks (a) 30 s H₂ plasma treatment; (b) 30 s NH₃ plasma treatment.

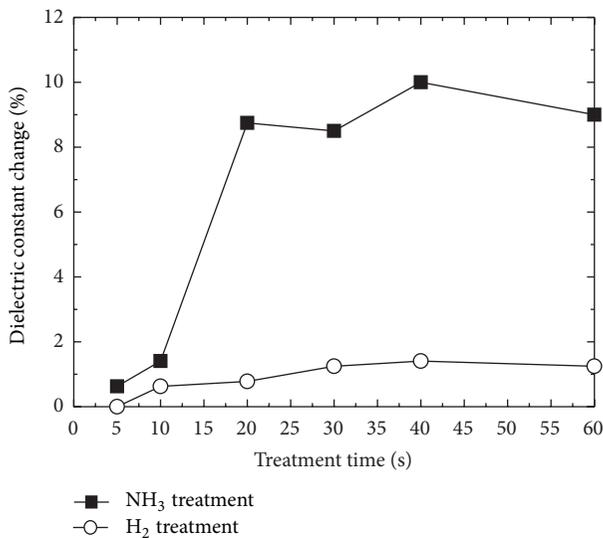


FIGURE 9: Change of dielectric constant of low-*k* dielectrics for H₂ and NH₃ plasma treatments as functions of treatment time.

the plasma treatment on the ILD must be taken into consideration because the dielectric constant of the low-*k* dielectric is the most essential factor in determining the RC delay time of the interconnects. Figure 9 plots the dependence of the plasma treatment conditions on the dielectric constant of low-*k* dielectrics. NH₃ plasma treatment increases the dielectric constant of low-*k* dielectrics more than H₂ plasma treatment. The increase in the dielectric constant of low-*k* dielectrics is caused by the nitridation process in the top part of the ILD by NH₃ plasma treatment. Additionally, the dielectric constant of low-*k* dielectrics increases with plasma treatment time, saturating as the treatment time exceeds 20 s because plasma bombardment reduces the carbon atomic concentration in the low-*k* dielectrics, but the increase is less than 10% for all treatment conditions.

Figure 10 presents the electrical results of sheet resistance of Cu lines and leakage current between Cu lines under various treatment conditions. The presented results were obtained from pattern wafers with three-layer metallization.

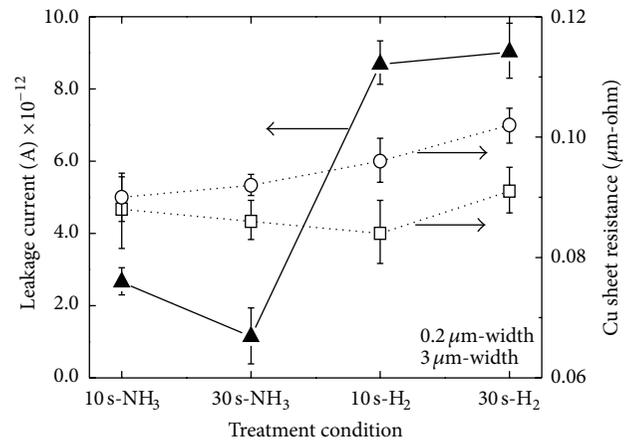


FIGURE 10: Sheet resistance of Cu lines and leakage current between Cu lines after various plasma treatment conditions.

As shown, Cu sheet resistance is independent of the treatment gas and the treatment time for both narrow and wide Cu lines, revealing that plasma treatment did not significantly change the granularity or constitution of the Cu lines. On the contrary, the leakage current between the Cu lines was sensitive to the plasma treatment conditions. Under NH₃ plasma treatment, a lower leakage current was detected in comparison to H₂ plasma treatment. The main current leakage path is along the interface between the Cu layer and the barrier layer [17]. Therefore, the adhesion at the interface between the Cu layer and the barrier layer becomes stronger under NH₃ plasma treatment because of the formation of Cu-N bonds. The increase in adhesion at the Cu interface can effectively block the leakage current path, reducing the leakage current [18]. H₂ plasma treatment time has no significant impact on the leakage current. In contrast, the leakage current is slightly reduced as the NH₃ plasma treatment time increased from 10 s to 30 s.

Figure 11 presents the lognormal plot of EM failure times of via-line test structures under various plasma treatment conditions. The Cu test structure without any plasma treatment is also displayed as a reference. Plasma treatment of

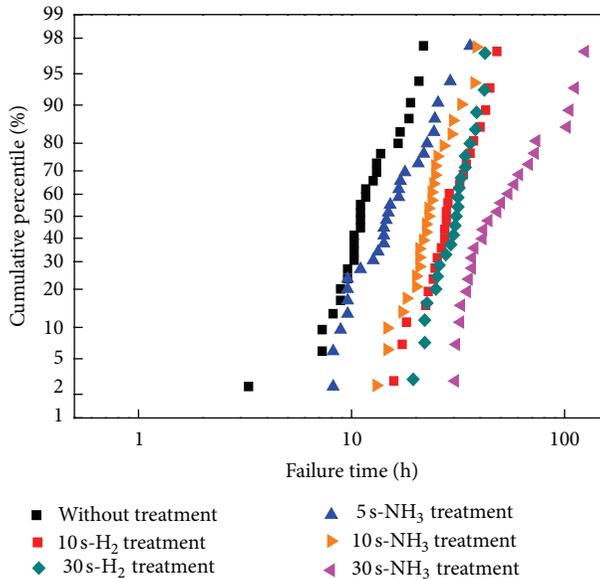


FIGURE 11: Cu EM failure time distribution for various plasma treatment conditions.

the Cu surface clearly increases EM failure times, revealing that the interfacial diffusion dominated the EM failure mechanism [19]. Furthermore, NH_3 plasma treatment with insufficient time (<20 s) yielded shorter failure times in comparison to H_2 treatment. This result is consistent with that of Vairagar et al. [11], because not all of the native Cu oxide layer is removed by NH_3 plasma treatment for insufficient time. The remaining Cu oxide layer at the Cu interface reduces the adhesion strength between the Cu line and the barrier layer under electrical stress, weakening the Cu interface, facilitating the diffusion of Cu ions along the surface, accelerating the formation of voids, and thus, shortening EM failure time. In contrast, when the NH_3 treatment time is increased above 20 s, the failure times are longer than those with H_2 treatment since the Cu oxide layer is sufficiently removed and Cu-N bonds form, reinforcing the adhesion strength of Cu lines with the barrier layer.

4. Conclusions

NH_3 and H_2 plasma treatments on Cu interconnects are used to remove the Cu oxide layer. This study investigated the surface state, electrical, and reliability characteristics of Cu interconnects under these two plasma treatments. H_2 plasma treatment yields an excellent removal rate of the Cu oxide layer and has less impact on the formation of Cu hillocks and the low- k dielectric layer in comparison to NH_3 plasma treatment. However, it created no new detectable bonds with Cu layer, which would have enhanced the adhesion strength between the Cu layer and the barrier layer, resulting in higher leakage currents between Cu lines and shorter EM failure times. In NH_3 plasma treatment, an insufficient treatment time leads to an increased probability of delamination at

the Cu/barrier layer interface. Hence, extending NH_3 plasma treatment time can efficiently reduce the adhesion failures and enlarge EM resistance.

Acknowledgments

The authors would like to thank the National Science Council of the Republic of China, Taiwan, for financially supporting this research under Contract no. NSC 102-2221-E-260-009. Ted Knoy is appreciated for his editorial assistance.

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Research Article

Effect of Coercive Voltage and Charge Injection on Performance of a Ferroelectric-Gate Thin-Film Transistor

P. T. Tue,^{1,2} T. Miyasako,³ E. Tokumitsu,^{1,2,4} and T. Shimoda^{1,2,4}

¹ Japan Science and Technology Agency, ERATO, Shimoda Nano-Liquid Process Project, 2-13 Asahidai, Nomi, Ishikawa 923-1211, Japan

² Green Devices Research Center, Japan Advanced Institute of Science and Technology (JAIST), 2-13 Asahidai, Nomi, Ishikawa 923-1211, Japan

³ Yokkaichi Research Center, JSR Corporation, Yokkaichi 510-8552, Japan

⁴ School of Materials Science, Japan Advanced Institute of Science and Technology, 1-1 Asahidai, Nomi, Ishikawa 923-1211, Japan

Correspondence should be addressed to P. T. Tue; phan-tt@jaist.ac.jp

Received 11 October 2013; Accepted 27 November 2013

Academic Editor: Tung-Ming Pan

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We adopted a lanthanum oxide capping layer between semiconducting channel and insulator layers for fabrication of a ferroelectric-gate thin-film transistor memory (FGT) which uses solution-processed indium-tin-oxide (ITO) and lead-zirconium-titanate (PZT) film as a channel layer and a gate insulator, respectively. Good transistor characteristics such as a high “on/off” current ratio, high channel mobility, and a large memory window of 10^8 , $15.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and 3.5 V were obtained, respectively. Further, a correlation between effective coercive voltage, charge injection effect, and FGT’s memory window was investigated. It is found that the charge injection from the channel to the insulator layer, which occurs at a high electric field, dramatically influences the memory window. The memory window’s enhancement can be explained by a dual effect of the capping layer: (1) a reduction of the charge injection and (2) an increase of effective coercive voltage dropped on the insulator.

1. Introduction

Ferroelectric-gate thin-film transistors (FGTs) have attracted much attention due to their nonvolatility, high write speed, low power consumption, and high endurance. Various types of FGTs composed of different stacked structures have been investigated [1–11]. Nevertheless, these devices exhibited very short retention time up to now, except for the case of epitaxial growth of the stacked ZnO/PZT/SrRuO_3 structure by pulsed laser processing [6, 12]. The main causes of the short retention time have widely been approved to be the effect of depolarization field from an interlayer and leakage current in the ferroelectric film on the Si surface channel [13–18]. In recent, the directly stacked oxide semiconductor/ferroelectric structure using pulsed laser processing is considered to be effective for forming a “clean” interface [6, 12, 19]. The costly pulsed laser processing, however, is unfavorable for industrial applications.

On the other hand, chemical solution processing can offer many advantages such as low fabrication cost, high

throughput, large area deposition, direct patternability, and direct printing of devices. We have been challenging to use solution-processed indium-tin-oxide (ITO) as a channel layer with combination of ferroelectric PZT gate insulator for FGTs. However, it seems to be more difficult to obtain a “clean” solution-processed ITO/PZT interface as compared with its counterpart by means of vacuum process. That is because of component interdiffusion (such as Pb, Zr, Ti, and In) or reaction between ITO and PZT layer, which occurs even at as low as 450°C treatment [20–22]. In order to solve the interface problem, we have proposed the use of a lanthanum oxide (LO) as a capping layer between ITO and PZT to prevent the reaction and interdiffusion between these layers, as well as to improve the retention properties [23]. As a result, the ITO/LO/PZT interface with atomically flat and no undesirable interface layer was obtained. The fabricated device exhibited a typical n-channel memory transistor with a high “on/off” current ratio ($I_{\text{on}}/I_{\text{off}}$) of more than 10^8 and a large memory window (M_w) of 3.0 V.

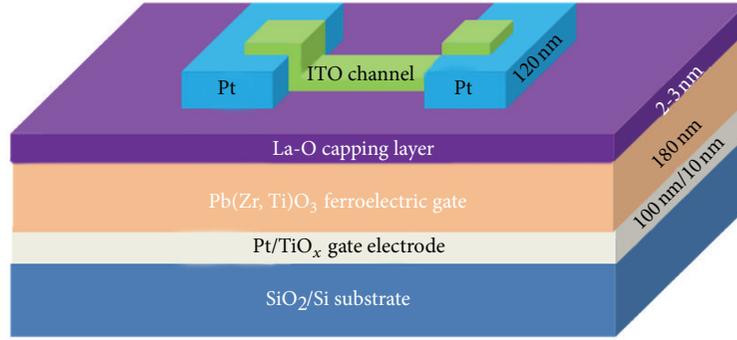


FIGURE 1: The cross-sectional structure of the fabricated FGT device.

Furthermore, in the ferroelectric-gate FETs, the memory window is theoretically equal to twice the coercive voltage [24]. However, in the practical cases, the memory window is not equivalent to double coercive voltage due to the voltage drop across an interlayer between the ferroelectric and the semiconductor. When a gate bias is applied to the ferroelectric gate structure, the unsaturated electric field applied to the ferroelectric film and the charge injection from the semiconductor to the interlayer can dominantly reduce the memory window because a high electric field is applied to the interlayer. Thus, it has usually suggested inserting a buffer insulator between the ferroelectric and the semiconducting channel, resulting in decreasing the electric field applied to the interlayer [25, 26]. In this work, the influence of coercive voltage and charge injection on device performance was investigated. It is found that the charge injection from the channel to the insulator layer dramatically influences on the memory window. The memory window's enhancement can be explained by a dual effect of the capping layer: (1) a reduction of the charge injection and (2) an increase of effective coercive voltage dropped on the insulator.

2. Experimental Details

To fabricate a FGT device, first Pt/Ti (100 nm/10 nm) film was deposited on a thermally grown SiO₂ (500 nm)/Si substrate by a radio-frequency magnetron sputtering as a bottom gate [27]. Then, PZT gate insulator (180 nm) was formed by the sol-gel method using alkoxide-based PZT (120/40/60) precursor solution (8 wt%, Mitsubishi Chemical Co.). This solution was spin coated and dried at 240°C in air for 5 min. The process was repeated 4 times to get the desire film thickness. After that, the PZT layer was crystallized at 600°C for 20 min in ambient air environment. Next, a LO layer was fabricated by spin coating using a nitrate-based precursor solution (0.1 mol/kg, Sigma-Aldrich Co.), and then slowly heated up to 550°C (10°C/min) and held for 10 min in O₂. In the following fabrication steps, Pt source and drain electrodes were sputtered at room temperature and patterned by a lift-off process. After that, an ITO layer (~30 nm) was deposited by spin-coating using carboxylate-based precursor solution (5 wt % SnO₂-doped, Kojundo Chemical Laboratory Co.) followed by annealing at 450°C for 30 min in air. Device

region was patterned and isolated by the reactive ion etching. The channel length and width of the fabricated devices were 30 and 60 μm, respectively. For comparison, we also fabricated the conventional ITO/PZT sample by the solution process [23]. A cross-sectional structure of the fabricated FGT device is shown in Figure 1.

Cross-section high-resolution transmission electron microscope (HRTEM) image and selected area electron diffraction (SAED) patterns were obtained with a scanning TEM, JEM-ARM200F system (JEOL). Polarization-voltage (*P-V*) hysteresis loops of the PZT films were measured by a Ferroelectric Characterization Evaluation System (TOYO Corporation Model FCE-1). Capacitance-Voltage (*C-V*) measurements were carried out using a precision component analyzer (Wayne Kerr 6440B Model) at 1.0 kHz. Device characterization was carried out at room temperature by using a Semiconductor Parameter Analyzer (Agilent 4155C Model).

3. Results and Discussion

3.1. Structural and Electrical Properties of the Solution-Processed ITO/LO/PZT FGT Device. Figure 2 shows AFM images of the conventional PZT (Figure 2(a)) and new LO/PZT surface (Figure 2(b)). We found that the LO/PZT surface, which consisted of small and uniform grains, was much smoother than the conventional PZT surface. Namely, the RMS values of the conventional PZT and the new LO/PZT surface were 2.28 nm and 0.63 nm, respectively. Also, this difference in surface roughness can be clearly seen when comparing 3D-AFM images of the PZT and LO/PZT surface as shown in the insets. From this result one can expect that the carrier scattering at the interface between ITO and LO/PZT layers would be less than that in the conventional ITO/PZT structure.

The cross-sectional image of the ITO/LO/PZT structure by HRTEM exhibited an atomically flat interface with no defective layer (Figure 3). The thickness of the LO layer was as thin as 2-3 nm. In addition, the high angle annular dark-field scanning TEM (HAADF-STEM) image and the TEM-EDX line analysis crossing ITO/LO/PZT interfaces apparently showed high uniformity of PZT layer and negligible out-diffusion of Pb, Zr, and Ti elements. Also, two dimensional

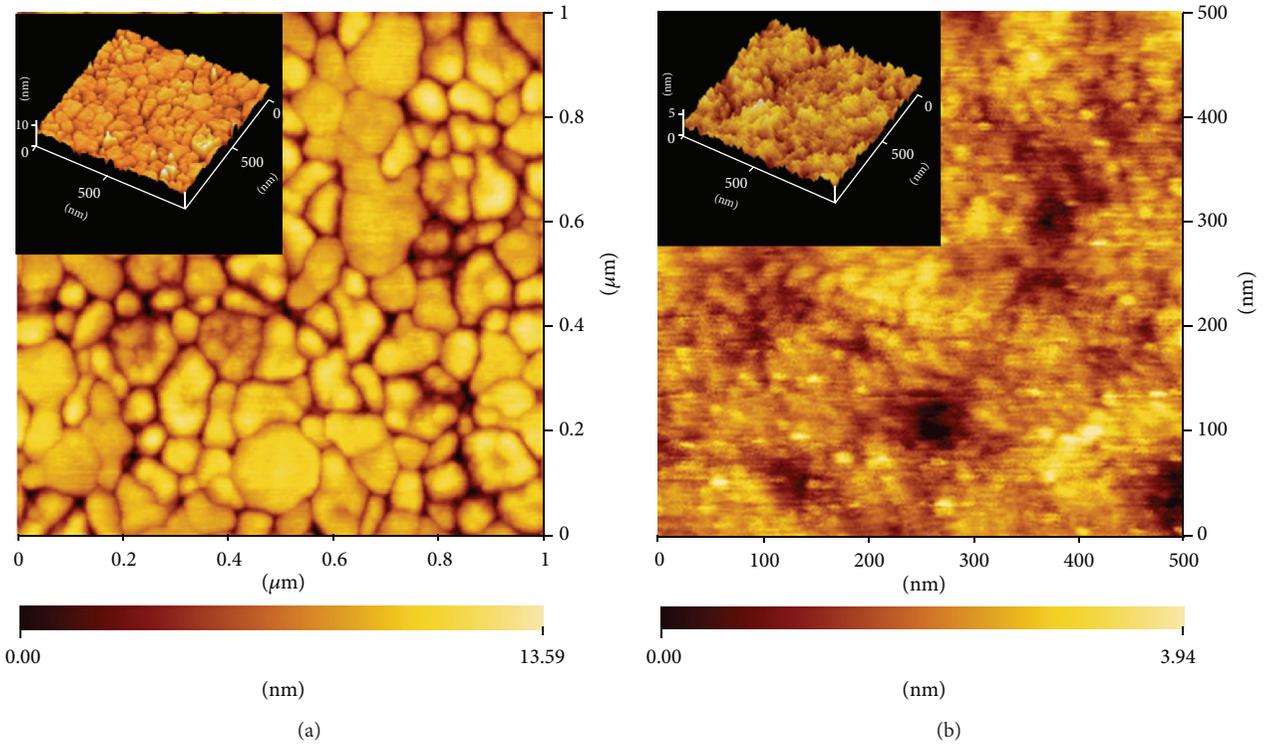


FIGURE 2: AFM images of (a) PZT and (b) LO/PZT surface. The insets of (a) and (b) are 3D-topography images, respectively.

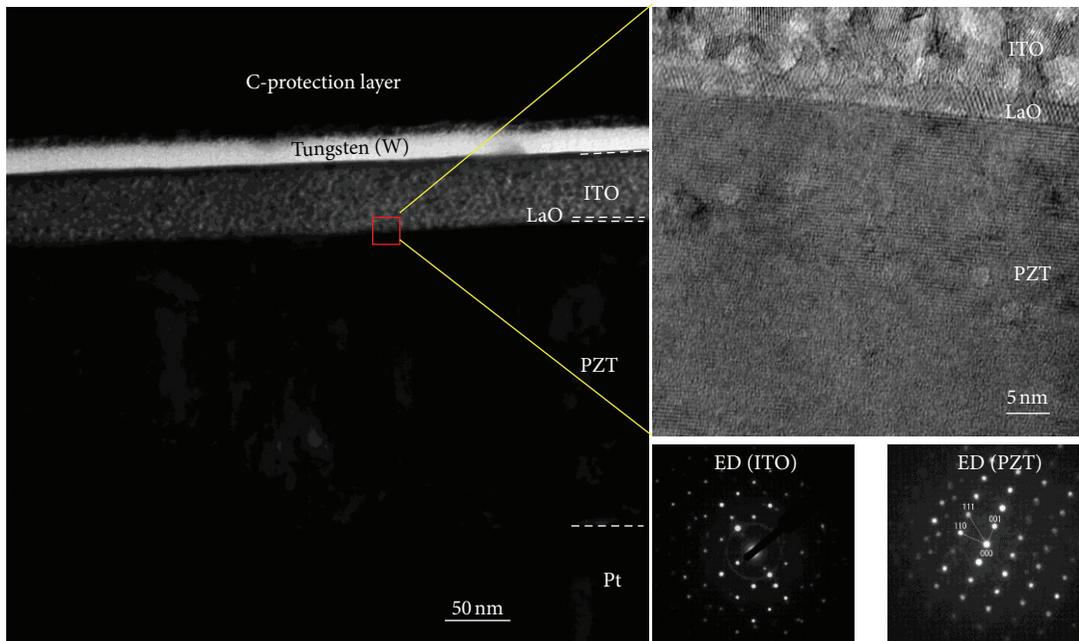


FIGURE 3: Cross-sectional HR-TEM images of the ITO/LO/PZT/PT stacked structure and electron diffraction patterns of ITO and PZT layers.

(2D) EDX element mapping exhibited homogeneous compositional distribution of the ITO and PZT layers (not shown here) [19]. In contrast, a HRTEM image at ITO/PZT interface revealed an amorphous interlayer having a thickness of 7–10 nm. In addition, approximately 10 at % loss of Pb and

Ti atoms were observed in 10 nm thickness from the PZT surface by their diffusion into the ITO layer. Therefore, the ITO layer actually contains Pb atoms as impurity [19, 21]. The electron diffraction patterns of ITO and PZT layers indicate their polycrystalline structures, which are consistent with

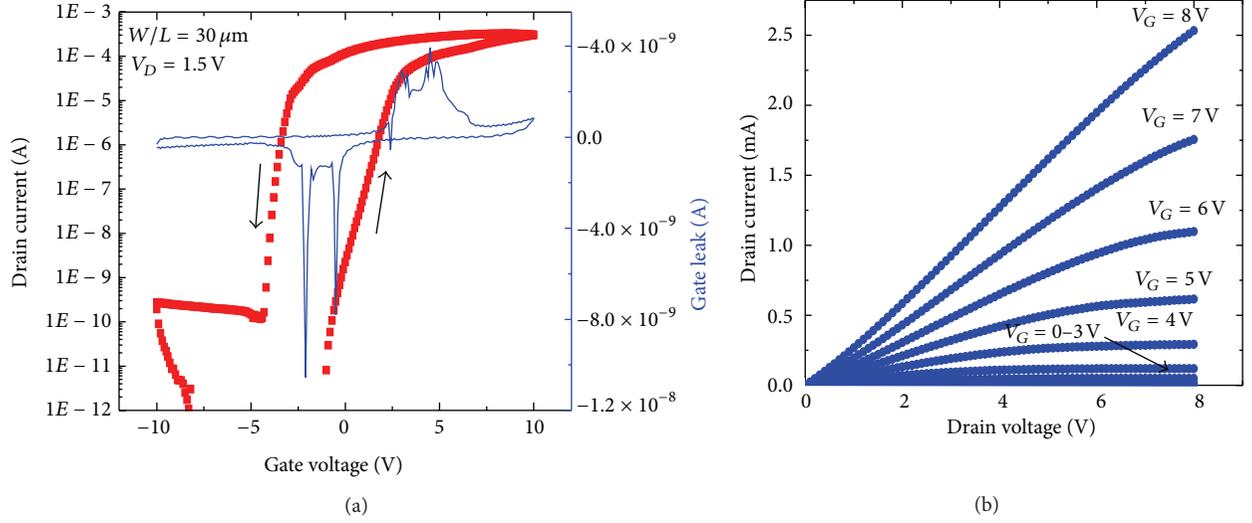


FIGURE 4: (a) Transfer and (b) output characteristics of the fabricated FGT device.

XRD analysis, with preferential orientation of (222) and (111), respectively.

Figure 4 shows the transfer (I_D - V_G) and output (I_D - V_D) characteristics of the fabricated FGT device. The I_D - V_G curve exhibited counterclockwise hysteresis loop due to ferroelectric polarization of the PZT as indicated by the arrows, which confirmed the nonvolatile memory function of this device. The I_D - V_D curve shows a typical n-type transistor behavior with a good drain current saturation. We can see that the gate leakage currents (in both negative and positive regions) are relatively small (~ 10 pA). The observed peaks in the gate leakage current resulted from the polarization currents of the ferroelectric PZT layer. Therefore, we may consider that the rounded behaviour in the transfer curve at the negative region is not mainly caused by the gate leakage current. Once the device is turned on, it is not completely switched off as the negative voltage applied, leading to the rounded characteristic. We speculate that carriers in some part of the channel layer might not be completely depleted.

In the conventional ITO/PZT structure, a relatively large $I_{\text{on}}/I_{\text{off}}$ ratio was obtained but the drain current ratio, that is, the binary states, at a zero gate voltage, which is indispensable for nonvolatile memories, was not sufficiently large owing to a shift in the threshold voltage to the negative voltage side [19, 21, 23, 25]. On the other hand, the new ITO/LO/PZT structure presented an excellent $I_{\text{on}}/I_{\text{off}}$ and a ΔV_{th} of more than 10^8 and 3.5 V, respectively, which are much better than those of previous reported FGTs [1–6]. The field-effect mobility of $15.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was estimated from the saturation region of the device's output characteristics, which is comparable to or higher than other reported oxide-channel TFTs by means of vacuum processes [1, 12]. Furthermore, the threshold voltage from a negative bias to a positive one was very close to a zero gate voltage, which indicated that the amount of space charge in the PZT film and at the ITO/LO/PZT interfaces was relatively low [12].

It was demonstrated that the LO layer acted as a good barrier film not only for preventing the interdiffusion between the ITO semiconductor and PZT insulator layers, but also for stabilizing the PZT surface structure. We speculate that La^{3+} ions are incorporated into PZT structure by substituting for Pb^{2+} ions, which effectively stabilizes PZT structure by preventing Pb evaporation and formation of oxygen vacancies. Consequently, the interdiffusion between ITO and PZT layers were suppressed resulting in good ITO/PZT interface properties [23].

3.2. Analysis on the Influence of Charge Injection on the Memory Window of the ITO/LO/PZT FGT Device. In the ferroelectric-gate structure, a differential form of Gauss's law describes the relationship between the maximum electric field in the semiconducting layer, E_{sc} , the ferroelectric displacement, D_{fe} , and any free charge, Q_i , which might reside near the ferroelectric/semiconductor interface [28]:

$$\epsilon_{\text{sc}} E_{\text{sc}} = Q_i + D_{\text{fe}}, \quad (1)$$

where ϵ_{sc} is the dielectric constant of the semiconductor. Depending on the signs of D_{fe} and Q_i , the semiconducting layer may either be inverted, depleted, or accumulated. D_{fe} is known from ferroelectric hysteresis measurements. Typical values of E_{sc} calculated from (1) are so large that it is probable that some carriers will be injected into the ferroelectric. For our case, the relative dielectric constant of the semiconductor is approximately 10, and D_{fe} is $30 \mu\text{C}/\text{cm}^2$, then E_{sc} is $\sim 3 \times 10^7 \text{ V}/\text{cm}$. This injected "homocharge" is opposite in site to D_{fe} , and if it becomes trapped (as Q_i), E_{sc} will drop, slowing the injection process. Consequently, we might anticipate that interface charge could play a role in device operation.

Figure 5(a) shows the P - V hysteresis loops of the Pt/LO/PZT/Pt capacitor. As clearly seen, as increasing applied voltage both the coercive voltage and remnant polarization value increase due to switching of ferroelectric

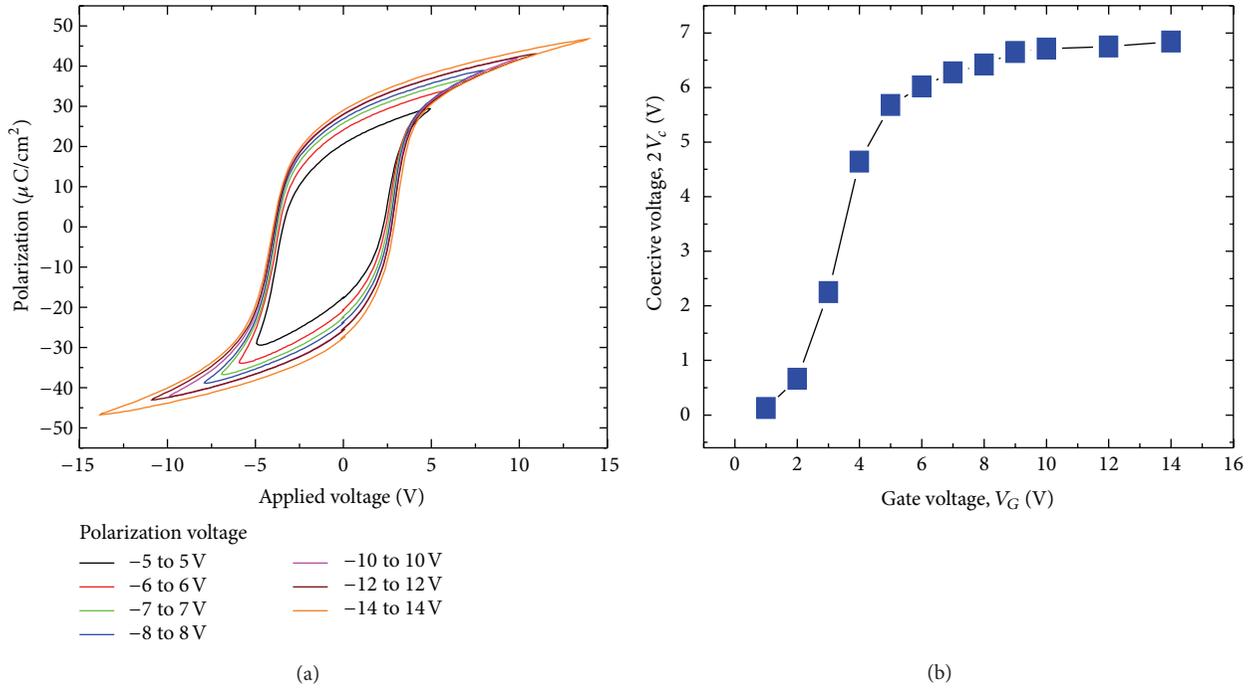


FIGURE 5: (a) *P-V* hysteresis loops and (b) the twice of the coercive voltages of the Pt/LO/PZT/Pt capacitor.

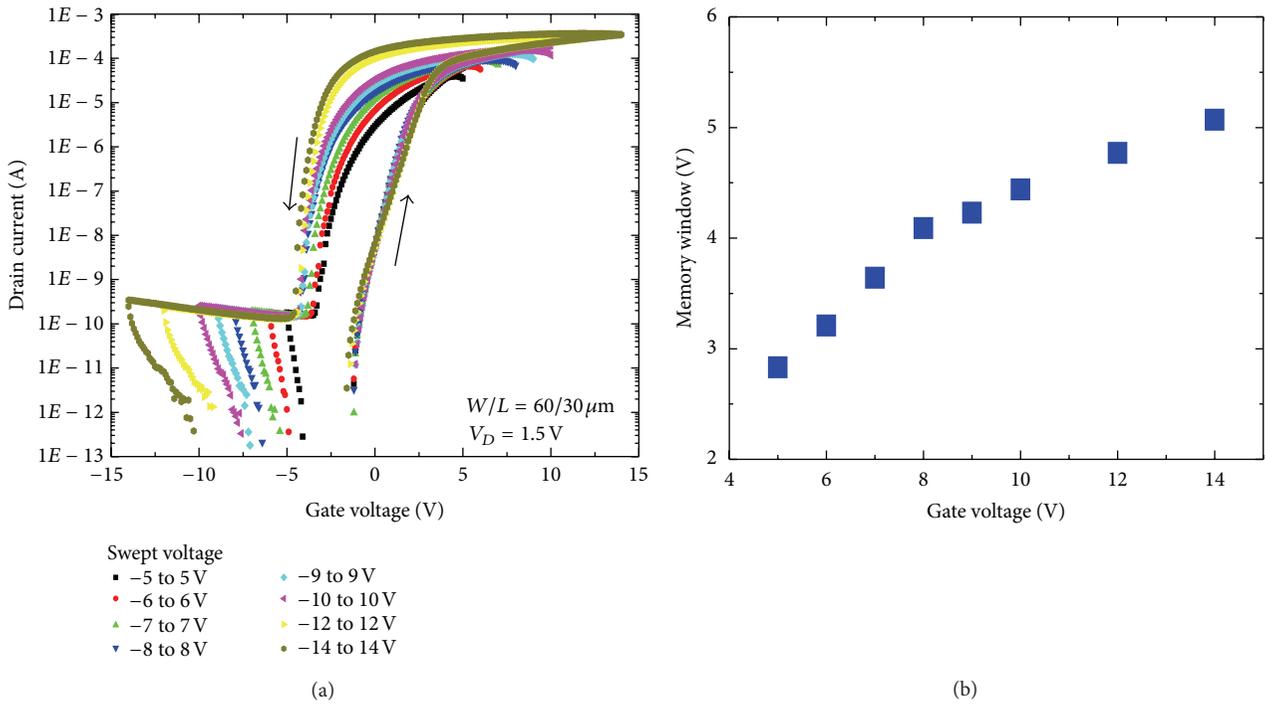


FIGURE 6: (a) Transfer curves and (b) memory window as a function of gate sweep voltage.

domains. A variation of the coercive voltage as a function of the applied voltage is summarized in Figure 5(b), which indicates that hysteresis loops get saturated at approximately 5 V.

Figure 6(a) shows the transfer characteristics of the ITO/LO/PZT FGT device when the gate voltage was swept from ± 5 to ± 14 V. Increasing the gate voltage, the memory

window increases symmetrically, which reveals the excellent ferroelectric polarization switching property. Figure 6(b) summarizes the change of memory windows as a function of gate voltage.

As mentioned above, the memory is severely reduced by the charge injection from the ITO into the interlayer between ITO and PZT layers. The following relationship

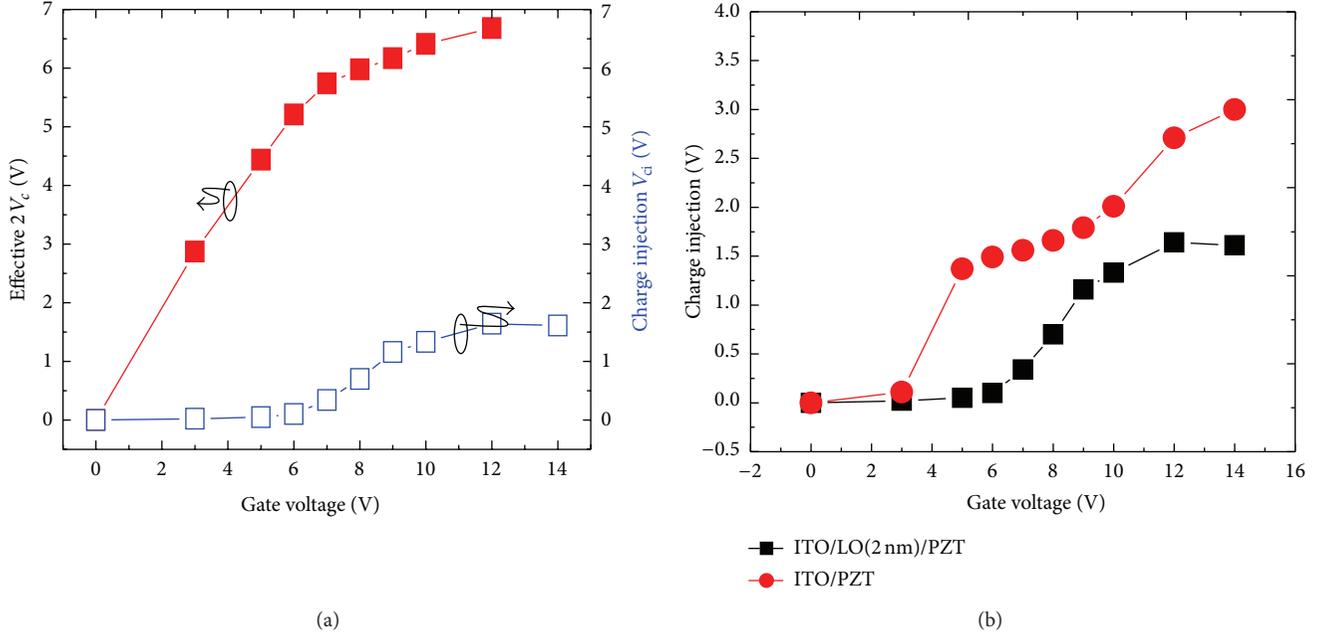


FIGURE 7: Effective coercive voltage ($2V_c$) applied to PZT films and reduction values ($2V_c - V_m$) of memory window by charge injection in the ITO/LO/PZT structure. The values of charge injection are $2V_c - V_m$, at the same gate voltage, where $2V_c$ is twice the coercive voltage at the real applied voltage on the PZT film only.

clearly expresses how much the memory window will be reduced:

$$V_m = 2V_c - V_{ci}, \quad (2)$$

where V_m is the memory window, $2V_c$ is the effective double coercive voltage, and V_{ci} is the flat band voltage shift due to charge injection. Here, the effective coercive voltage can be derived from Figure 5(a) after calculating the voltage distribution across the series capacitance consisting of the PZT, LO, and ITO layer. We have determined the effective voltage applied to the capacitor by following relations:

$$\begin{aligned} V_f &= \frac{\epsilon_s \epsilon_i d_f}{\epsilon_s \epsilon_i d_f + \epsilon_s \epsilon_f d_i + \epsilon_f \epsilon_i d_s} V_G, \\ V_i &= \frac{\epsilon_s \epsilon_f d_i}{\epsilon_s \epsilon_i d_f + \epsilon_s \epsilon_f d_i + \epsilon_f \epsilon_i d_s} V_G, \\ V_s &= \frac{\epsilon_i \epsilon_f d_s}{\epsilon_s \epsilon_i d_f + \epsilon_s \epsilon_f d_i + \epsilon_f \epsilon_i d_s} V_G, \end{aligned} \quad (3)$$

where V , ϵ , and d are the effective voltages applied to the capacitor, the dielectric constant, and the thickness, respectively. The subscripts of i , s , f , and G stand for the insulator (LO), semiconductor (ITO), ferroelectric (PZT), and gate, respectively.

To calculate the dielectric constants of the capacitors, we assumed a dielectric constant value of the 7 nm-thick interlayer between ITO and PZT films to be 5. The thickness and dielectric constant of the LO layer are 2 nm and 27, respectively. Based on the equivalent circuit of the

ITO/LO/PZT structure, the calculated dielectric constants of PZT and ITO using the accumulation region of the C - V curve are about 457.6 and 50.8, respectively. Using these values and (3) we can calculate the electric field distribution in the series capacitor as follows: $V_f = 0.493V_g$ and $V_i = 0.246V_g$. Using (2) we can extract the $2V_c$ and the V_{ci} dependence on the gate voltage as shown in Figure 7(a).

Figure 7(a) shows a dependence of the effective coercive voltage and the charge injection on the gate voltage. It is found that the ITO/LO/PZT structure causes the memory window enhancement due to the increase in the $2V_c$ and the decrease in the V_{ci} . Interestingly, when the gate bias goes up to 7 V the $2V_c$ seems to be saturated and the V_{ci} starts to rise from zero. Increasing the gate voltage led to the slight change of V_{ci} . There was no severe charge injection observed even when the gate voltage rises up to 14 V, which can be confirmed by the measurement of the memory window as shown in Figure 6(b).

As for the conventional ITO/PZT structure, the calculated voltage distributions across the series capacitance consisting of the PZT, interlayer ($d_i \sim 5$, $t_i \sim 7$ nm), and ITO layer are $V_f = 0.189V_g$ and $V_i = 0.711V_g$. Therefore, most of the applied voltage dropped on the interlayer, which may cause severe charge injection from the semiconductor layer to it. As shown in Figure 7(b), the charge injection in the conventional structure was severely raised at a rather small V_g of about 4 V.

This result suggests that the memory window can be enhanced by adjusting the LO layer thickness or thickness ratio of LO to PZT layer. Inserting a thin LO layer, although the effect field on the PZT is reduced, the memory window of the ITO/LO/PZT structure increases since the electric field

applied to the interlayer decreases, resulting in the reduction of charge injection.

4. Conclusion

We fabricated and investigated operation of a solution-processed ITO-channel ferroelectric-gate thin-film transistor memory (FGT) which uses the LO as a capping layer. Good transistor characteristics such as a high “on/off” current ratio, high channel mobility, and a large memory window of 10^8 , $15.0 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and 3.5 V were obtained, respectively. The impacts of effective coercive voltage and charge injection effect on the FGT’s performance were also investigated. The experimental and theoretical analysis reveals that the memory window equals the difference between the effective coercive voltage ($2V_c$) ($2V_c$) applied to the ferroelectric film and the flat band voltage shift due to charge injection (V_{ci}). The memory window’s enhancement can be explained by a dual effect of the capping layer: (1) a reduction of the charge injection and (2) an increase of effective coercive voltage dropped on the insulator.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this article.

Acknowledgments

The authors would like to thank the researchers of the Japan Science and Technology Agency, ERATO, Shimoda Nano-Liquid Process Project, and Green Devices Research Center, Japan Advanced Institute of Science and Technology, for their discussion. This work was financially supported by the ERATO project.

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Research Article

Electric and Magnetic Properties of Sputter Deposited BiFeO₃ Films

N. Siadou,¹ I. Panagiotopoulos,¹ N. Kourkoumelis,² T. Bakas,³
K. Brintakis,^{4,5} and A. Lappas⁴

¹ Department of Materials Science and Engineering, University of Ioannina, 45110 Ioannina, Greece

² Department of Medical Physics, University of Ioannina, 45110 Ioannina, Greece

³ Department of Physics, University of Ioannina, 45110 Ioannina, Greece

⁴ Institute of Electronic Structure and Laser, Foundation for Research and Technology-Hellas, Vassilika Vouton, 711 10 Heraklion, Greece

⁵ Department of Physics, Aristotle University of Thessaloniki, 541 24 Thessaloniki, Greece

Correspondence should be addressed to I. Panagiotopoulos; ipanagio@cc.uoi.gr

Received 4 October 2013; Accepted 17 October 2013

Academic Editor: Tung-Ming Pan

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Polycrystalline BiFeO₃ films have been magnetron sputter deposited at room temperature and subsequently heat-treated ex situ at temperatures between 400 and 700°C. The deposition was done in pure Ar atmosphere, as the use of oxygen-argon mixture was found to lead to nonstoichiometric films due to resputtering effects. At a target-to-substrate distance $d = 2''$ the BiFeO₃ structure can be obtained in larger range process gas pressures (2–7 mTorr) but the films do not show a specific texture. At $d = 6''$ codeposition from BiFeO₃ and Bi₂O₃ has been used. Films sputtered at low rate tend to grow with the (001) texture of the pseudocubic BiFeO₃ structure. As the film structure does not depend on epitaxy similar results are obtained on different substrates. A result of the volatility of Bi, Bi rich oxide phases occur after heat treatment at high temperatures. A Bi₂SiO₅ impurity phase forms on the substrate side, and does not affect the properties of the main phase. Despite the deposition on amorphous silicon oxide substrate weak ferromagnetism phenomena and displaced loops have been observed at low temperatures showing that their origin is not strain. Ba, La, Ca, and Sr doping suppress the formation of impurity phases and leakage currents.

1. Introduction

Recently there is a revival of the interest in magnetoelectric materials for novel multifunctional devices [1] and spintronic [2] applications. BiFeO₃ (BFO) is both ferroelectric ($T_C = 1100$ K) and antiferromagnetic ($T_N = 643$ K) at room temperature, and thus it is very promising for such applications [3]. Pulsed laser deposition [4–6] and sputtering [7–10] are standard methods to deposit BFO films. Magnetron sputtering is a very reproducible and easily controlled deposition technique that can be used to prepare heterostructures combining different types of layers. However, when magnetrons are used to prepare binary oxide materials, severe resputtering of the film during deposition can alter its composition [11]. In order to find the conditions which lead to formation of the crystalline BFO phase sputtering at different

substrate-to-target distances and process gas pressures have been tested. Here, we present a study of magnetron sputtered deposition of polycrystalline BiFeO₃ films in view of their use as exchange-biasing layers.

2. Experimental

Polycrystalline BFO and iron oxide films have been magnetron sputter deposited at room temperature using a MAN-TIS deposition system from a commercial BiFeO₃ (2'' and 3''), Bi₂O₃ (2''), and Fe₃O₄ (3'') targets of Kurt J. Lesker. The substrates are placed opposite to the sputtering targets (on axis). Pure (5N) Ar was used as a process gas. Three different methods have been applied: (i) deposition from a 2'' BFO at a substrate-to-target distance of 2'', (ii) low rate deposition from a 2'' BFO at a substrate-to-target distance of 6'', and

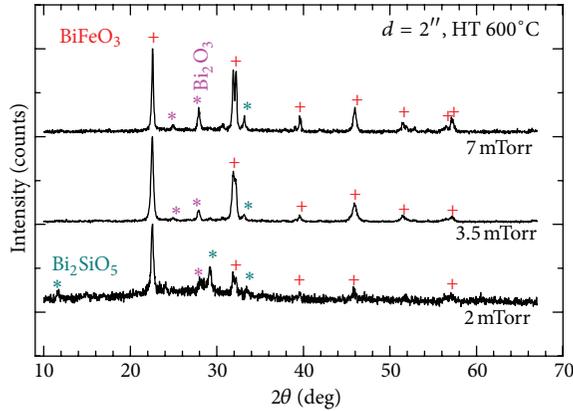


FIGURE 1: XRD patterns of bismuth ferrite films deposited under different sputtering gas pressures at a distance $d = 2''$.

(iii) codeposition from a BFO ($3''$) and Bi_2O_3 ($2''$) targets at a distance of $6''$. In order to achieve doping by elements as Ba, La, Sr, and Ca, corresponding oxide powders have been added either on the BiFeO_3 or on the Bi_2O_3 target for heavy or low doping, respectively. The BFO films have been sputter deposited and subsequently heat-treated ex situ at temperatures between 400 and 700°C . The X-ray diffraction (XRD) diagrams were collected with a Bruker D8 Advance Diffractometer. The magnetic measurements were performed with a Lake Shore vibrating sample magnetometer (VSM) and Quantum Design SQUID magnetometer. The microstructure was investigated with a JEOL JSM-5600 Scanning Electron Microscope. The leakage currents have been measured by a RT66B test system of Radiant technologies.

3. Optimization of the Deposition Conditions

In Figure 1, the XRD patterns of films deposited under different sputtering gas pressures at a distance $d = 2''$ are presented. The applied power is 100 W RF. In all cases, BiFeO_3 is the main phase, and the stoichiometry (determined by EDX) does not vary considerably, but it is close to $\text{Bi}_{47}\text{Fe}_{53}\text{O}_x$. More specifically, the atomic percent of Bi was determined to be 46.2, 47.5, and 47.1, for 2, 3.5, and 7 mTorr of Ar gas, respectively.

There is presence of bismuth oxide, mainly at higher Ar pressure, and Bi_2SiO_5 at lower Ar pressures. The former is a result of the volatility of Bi and the decomposition of the bismuth ferrite phase. If additional oxygen is used as a reactive gas, then the films are severely Bi deficient (EDX shows $\text{Bi}_{40}\text{Fe}_{60}\text{O}_x$) and the BiFeO_3 phase does not form. This may be attributed to resputtering as a result of oxygen anions bombardment of the substrate [11]. The Bi_2SiO_5 phase forms on the substrate side, as suggested by the presence of Si, and does not affect the properties of the main phase.

This can be proven by examining grazing incidence XRD patterns acquired at different incidence angles. The Bi_2SiO_5 peak intensity increases with the angle of incidence (Figure 2).

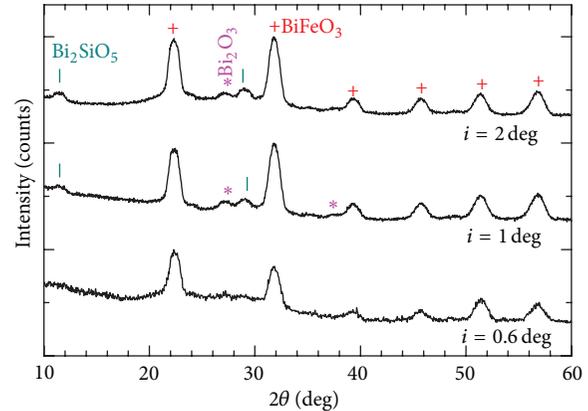


FIGURE 2: Grazing incidence XRD patterns of BFO films measured under different incidence angles. BiFeO_3 peaks are indicated by crosses, those of Bi_2SiO_5 by lines, and those of Bi_2O_3 by stars.

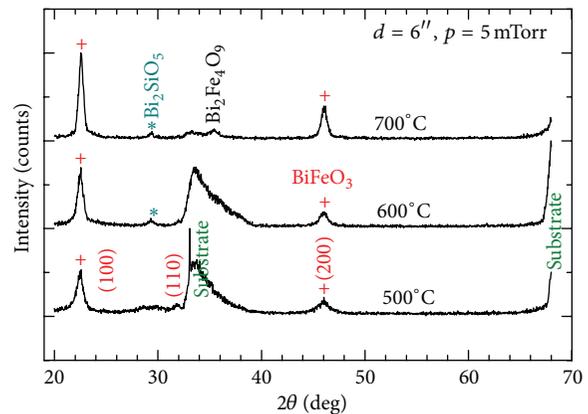


FIGURE 3: XRD patterns of bismuth ferrite films deposited Ar gas pressure $p = 5$ mTorr at a distance $d = 6''$ on oxidized Si wafers. The films show (100) texture of the pseudocubic unit cell which corresponds to the (012) of R3c.

In Figure 3 the XRD patterns of 20 nm thick heat-treated films deposited at $d = 6''$ at Ar pressure of 5 mTorr with deposition rate 0.03 nm/min. Similar results are obtained for films deposited at Ar pressure of 2 mTorr (0.25 nm/min). After ex situ heat treatment at 500°C , the BiFeO_3 phase with (100) texture of the pseudocubic unit cell appears. This corresponds to the (012) of rhombohedral phase (space group R3c) which is the bulk unit cell, resulting from the symmetry reduction due to the ferroelectric and accompanying distortions. The optimum heat-treatment temperature is 600°C while heat treatment at higher temperatures leads to the formation of the undesired phases as silicate, bismuth oxide, and in some cases other ferrites as $\text{Bi}_2\text{Fe}_4\text{O}_9$.

The degree of texture was estimated by profile refinement of the XRD patterns using the WinPLOTR package (Figure 4). The March preferred orientation function was used. The March parameter estimated to 0.22 which gives an average grain misalignment consistent with the rocking curves around the (001) pseudocubic reflection. In general, it was found that, under these conditions, the stoichiometry

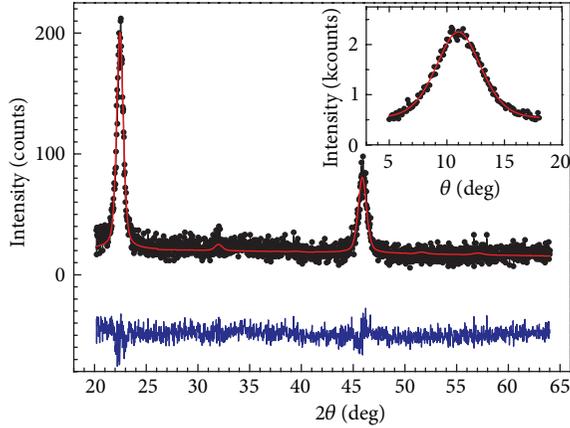


FIGURE 4: Rietveld fit of an XRD pattern of bismuth ferrite films deposited Ar gas pressure $p = 2$ mTorr at a distance $d = 6''$ and heat-treated at 500°C . The line at the bottom shows the difference between the theoretical and the experimental line. The inset shows a rocking curve around the (001) reflection.

and BiFeO_3 formation thereof was very sensitive to target usage partially due to magnetic field limitations of the $2''$ source. Therefore, we have chosen to use a $3''$ BiFeO_3 and enhance Bi content by codepositing from $2''$ Bi_2O_3 target. The rates were 1.38 nm/min and 0.25 nm/min, respectively. This small stoichiometry correction is crucial in reproducibly achieving the BiFeO_3 phase. In thicker films (260 nm) prepared under the same conditions, there is a strong presence of the cubic $\text{Bi}_{25}\text{FeO}_{40}$ phase. The impurity phases can be leached by 10% diluted HNO_3 for 30 minutes.

4. Microstructure and Domains

SEM studies have been performed to heat-treated BFO films which have been field cooled under 2 kOe from above the Néel temperature. Thus the formation of the ferroelectric domains is expected to be influenced by the coupling to the existing AF domains, due to the multiferroic nature of BFO that implies coupling between the two types of order [12]. The ferroelectric domain structure can be revealed by SEM using the brightness contrast between antiparallel ferroelectric domains on an unmetallized polar crystal surface [13–15]. Low accelerating voltage (down to 2 kV) and small beam current are used, in order to avoid severe charge accumulation on the insulating surface of the sample.

In BFO, the ferroelectric polarization can point along any of the eight directions defined by the four diagonals of the pseudocubic perovskite unit cell (with two antiparallel polarities for each direction). Between these eight possible different polar domains in BiFeO_3 $[\pm 1 \pm 1 \pm 1]$ there are three possible types of ferroelectric domain walls 71° , 109° , and 180° degrees typical of rhombohedral crystals. Different types of domains can be favored on the growth conditions [16]. These domains are stripe-like, and their width scales with film thickness. Very different irregular domain morphology has been observed in thin epitaxial films

[13]. In our case, the use of Si wafers covered with amorphous Si oxide layers excludes the possibility of strain appearance as relaxation mechanism in the morphology of domains. On the contrary, the polycrystalline nature and grain boundaries create complex multidomain structures.

SEM images of 125 nm thick films prepared at $d = 2''$ show that the films consist of large 20 – 100 μm island-like grains (Figure 5). The domain patterns are cloud-like irregular with size 3 – 7 μm . This complex domain structure may be attributed to the fact that, due to the existence of isolated islands, a unique global minimum cannot be achieved. Films prepared at $d = 6''$ look homogenous at larger areas and are also characterized by a fine mosaic-like domain structure in the range of 10 μm (Figure 6).

5. Weak Ferromagnetism Phenomena

Weak ferromagnetism phenomena have been observed long ago in antiferromagnetic (AF) fine particles and have been explained as a result of unbalanced magnetic moments of the two magnetic sublattices due to their finite size [17]. The presence of uncompensated surface spins leads to anomalous magnetic properties, such as large moments, coercivities, and hysteresis loop shifts. The antiferromagnetic ordering of BiFeO_3 is G-type that is, each spin is surrounded by six antiparallel spins on the nearest Fe neighbors. This ordering should give rise to magnetically compensated interfaces which is not favorable to exchange biasing. Thus surface magnetic heterogeneities, complexity of the underlying BFO film and nanoscale domain wall features, are crucial for the development of exchange biasing [14]. In sufficiently small particles the reduced coordination of surface spins can cause a fundamental change in the magnetic order throughout the particle [18]. In this case, a clear distinction between surface and bulk spin contributions to the total magnetic moment cannot be done. In AF thin films these phenomena are expected to dominate at low film thickness due to the increased contribution of the surfaces. The hysteresis loops at low temperatures (Figure 7) show ferromagnetic contributions, coercivity of 150 Oe, and a small exchange biasing evidenced by the vertical displacement of the loops, which is maximal (120 Oe) for the 87 nm film. The high field slope corresponds to the canting of the AF moments which is maximal for the 43 nm thin film. The remanence values are low and must be attributed to both bulk and surface contributions.

These different contributions become clearer in the magnetization versus temperature plots (Figure 8). The surface contribution is enhanced below 20 K. The thickness dependence implies that there is a surface contribution of 6.4 $\mu\text{emu}/\text{cm}^2$ and volume contribution of 1.16 emu/cm^3 at 5 K which become 4.3 $\mu\text{emu}/\text{cm}^2$ and 0.7 emu/cm^3 , respectively, at 300 K. These values range from 0.065 to 0.04 μ_B/Fe atom. As the magnetization values are higher for thinner films they must be attributed to surface contributions and should not be confused with some weaker contributions due to intrinsic mechanisms which could reflect an underlying competition between antiferromagnetic and ferromagnetic

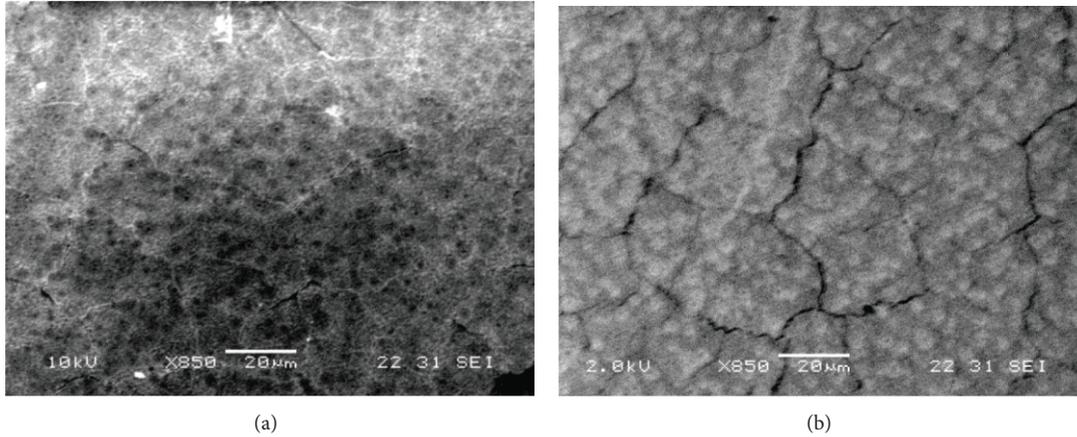


FIGURE 5: SEM images of a 125 nm thick BiFeO_3 film prepared at a source-to-substrate distance of $2''$. (a) was obtained with accelerating voltage of 10 kV. (b) was obtained with 2.5 kV. Large ($\sim 50 \mu\text{m}$) grains are observed along with smaller features related to the ferroelectric domain structure.

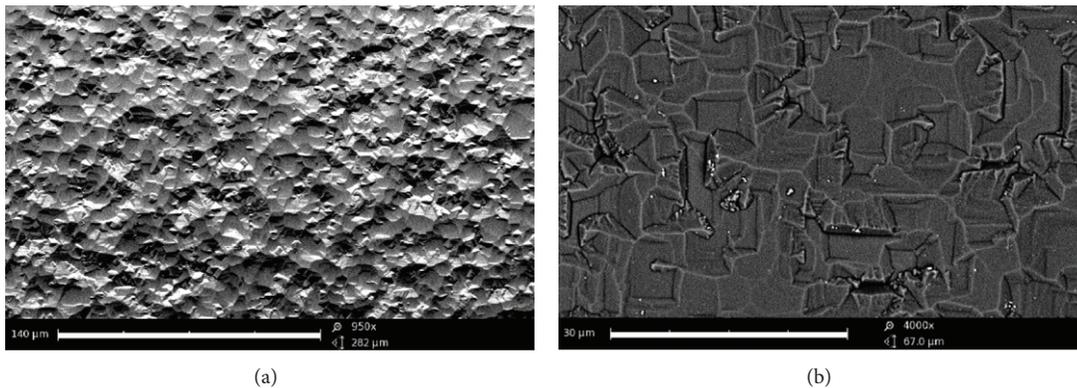


FIGURE 6: SEM images of an 87 nm thick BiFeO_3 film prepared at a source-to-substrate distance of $6''$.

interactions and the appearance of spin-glass state in the intermediate temperature range. Similar thickness dependence has been reported for spin-glass phenomena observed in compressively strained BiFeO_3 films from 19 to 114 nm epitaxially grown on LaAlO_3 [19]. The observation of similar behavior in our films deposited on the amorphous silicon oxide layers shows that strain mechanisms that have been revoked are not the only possible causes leading to the appearance of low temperature ferromagnetic contributions.

6. Effects of Doping

The XRD patterns of the $\text{Bi}_{1-x}\text{Ba}_x\text{FeO}_3$ series are shown in Figure 9. Ba doping suppresses the formation of impurity phases. In Figure 10, the variation of unit cell with Ba content is shown. The data are compared with the simple Vegard's law for a solid solution, extrapolating between the end members BiFeO_3 and BaFeO_3 (dashed line). The continuous line is a fit based on a simple geometrical relation for the size of the perovskite cell with the ionic radii as free parameters, yielding 1.35 nm, 1.42 nm, and 1.45 nm for Bi^{3+} , Ba^{2+} , and

oxygen, respectively. These values differ from those tabulated by Shannon [20] (1.03 nm, 1.35 nm, and 1.40 nm, resp.). The systematic increase of the cell constant with doping shows that Ba enters the main perovskite phase.

Low doping range is more interesting as it does not affect the ferroelectric properties, and it is sufficient to suppress the leakage currents. A compilation of the leakage current measurements, under different doping, is shown in Figure 11. Reduction of leakage is believed to occur because of the reduced oxygen vacancy which stabilizes the oxygen octahedral [21]. However, the abrupt enhancement of current at a threshold voltage can be attributed to an electronic localization-delocalization transition through band-filling control since oxygen vacancy distribution should be continuously varied by sweeping the applied voltage [22]. In general, the effect of substitutions is not limited to the "chemical pressure" due to ionic-radius mismatch with respect to Bi (minimal for Ca, La, moderate for Sr, and highest for Ba) but also to the effects to the stereochemically active ($6s^2$) lone-pair activity. In this case, the best results have been obtained for Sr and Ca substitutions.

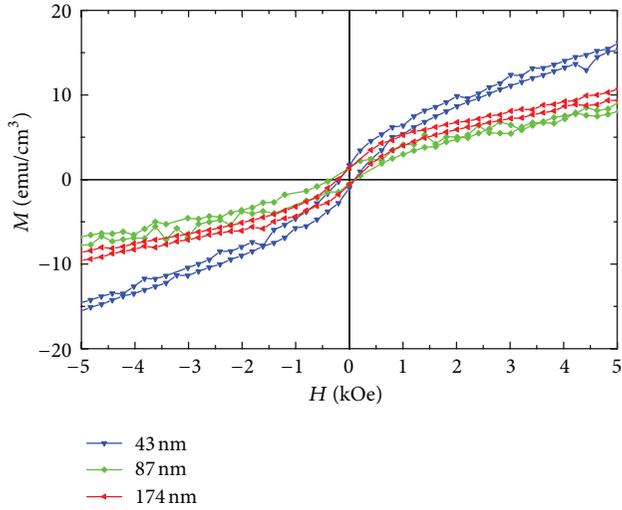


FIGURE 7: Hysteresis curves at 5 K after field cooling under a field of 70 kOe. Only the low field range is shown.

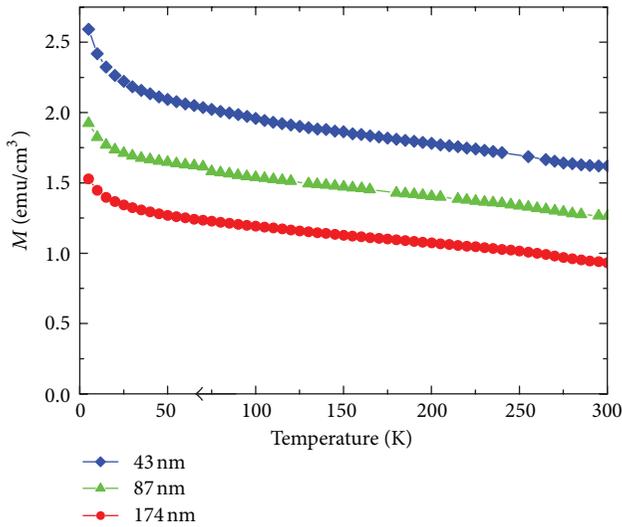


FIGURE 8: Magnetization as a function of temperature for BFO films of different thickness. The measurements have been done upon warming from 5 K to 300 K in the presence of a 100 Oe field after cooling under a field of 70 kOe.

7. Conclusion

Polycrystalline BFO films have been grown by RF magnetron sputtering on different substrates. The formation of the BFO depends very sensitively on sputtering conditions and heat-treatment temperature. In general, it was found that, when the substrate is placed close to the target $d = 2''$, the formation of BFO is more stable, that is, the phase can be obtained within a wide range of conditions but the films do not show a specific crystallographic texture, in contrast to those sputtered at $d = 6''$. As the films have been grown on the amorphous oxide layers of silicon wafers, it is proven that texture can be achieved without epitaxy of 20 nm films and furthermore that the low temperature weak ferromagnetism phenomena

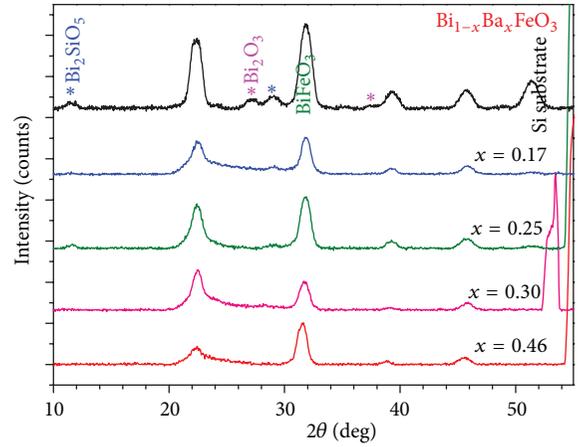


FIGURE 9: Grazing incidence XRD patterns $\text{Bi}_{1-x}\text{Ba}_x\text{FeO}_3$ films.

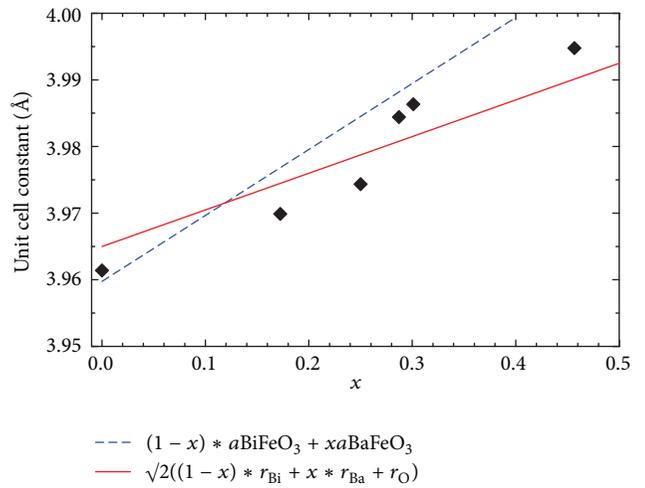


FIGURE 10: Pseudocubic unit cell parameter of $\text{Bi}_{1-x}\text{Ba}_x\text{FeO}_3$ films.

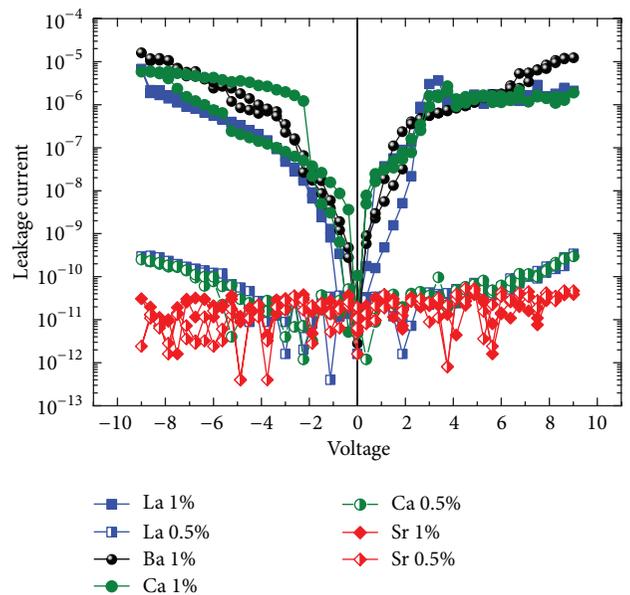


FIGURE 11: Leakage current across 90 nm thick doped BFO films (i.e., the maximum voltage corresponds to 100 kV/cm).

are not related to epitaxial strains. Doping suppresses the formation of impurity phases and leakage currents.

Acknowledgments

This research has been cofinanced by the European Union (European Social Fund—ESF) and Greek national funds through the Operational Program “Education and Lifelong Learning” of the National Strategic Reference Framework (NSRF)—Research Funding Program: Heracleitus-II. Investing in knowledge society through the European Social Fund. The authors would like to thank the authors John Kafegidakis and Ruud Bernsen at Phenom-World BV for recording some of the SEM images.

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Research Article

Surface State Capture Cross-Section at the Interface between Silicon and Hafnium Oxide

Fu-Chien Chiu

Department of Electronic Engineering, Ming Chuan University, Taoyuan, Taiwan 333, Taiwan

Correspondence should be addressed to Fu-Chien Chiu; fcchiu@mail.mcu.edu.tw

Received 5 August 2013; Accepted 30 September 2013

Academic Editor: Chun-Hsing Shih

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The interfacial properties between silicon and hafnium oxide (HfO_2) are explored by the gated-diode method and the subthreshold measurement. The density of interface-trapped charges, the current induced by surface defect centers, the surface recombination velocity, and the surface state capture cross-section are obtained in this work. Among the interfacial properties, the surface state capture cross-section is approximately constant even if the postdeposition annealing condition is changed. This effective capture cross-section of surface states is about $2.4 \times 10^{-15} \text{ cm}^2$, which may be an inherent nature in the HfO_2/Si interface.

1. Introduction

Hafnium oxide (HfO_2) has emerged recently as an essential dielectric material in the semiconductor industry, currently being used in logic gate stacks [1] and considered a promising candidate for resistance switching memory devices [2, 3] as well as surface passivation of advanced Si solar cells [4, 5]. Therefore, the determination of surface state capture cross-section at the interface between silicon and hafnium oxide is of great importance for the semiconductor industry, the photovoltaic industry, and the scientific community. The known characteristics of HfO_2 thin films include a large band gap ($\sim 6 \text{ eV}$) [6], a relatively high dielectric constant (>20) [7], an acceptable breakdown strength ($>4 \text{ MV/cm}$) [7], excellent thermodynamic stability [8], and an effective mass of carrier transportation [9]. In this work, the interface characteristics of the interface-trapped charge density (N_{it}), the interface-trapped charge density per area and energy (D_{it}), the effective capture cross-section (σ_s) of surface states, the surface recombination velocity (s_o), and the minority carrier lifetime (τ_{F1}) are identified. The typical electrical measurements of current-voltage (I - V) and capacitance-voltage (C - V) characteristics were performed on the $\text{Al}/\text{HfO}_2/\text{p-Si}$ metal-oxide-semiconductor (MOS) capacitors and metal-oxide-semiconductor field-effect transistors (MOSFETs). Both gated-diode method [10, 11] and subthreshold measurement [12] were applied to evaluate

the capture cross-section of interface states for the HfO_2 -gated MOSFETs. The gated-diode method is a simple way to accurately identify the interfacial characteristics using only a sweeping dc gate voltage, which was introduced in 1966 by Grove and Fitzgerald [10] to determine the surface-state density in MOS structures. According to the gated-diode measurements, the surface recombination velocity and the minority carrier lifetime (τ_{F1}) in the field-induced depletion region were extracted. In addition, the interface-trapped charge density per area and energy (D_{it}) was determined by using the device subthreshold measurement. Consequently, the effective capture cross-section of surface states was determined to be about $2.4 \times 10^{-15} \text{ cm}^2$ by the combination of gated-diode and device subthreshold measurements.

2. Experiment

Here, (100) p -type silicon wafers ($1\text{--}5 \Omega\text{-cm}$) were used as the starting material. Following the standard cleaning procedures, a 500 nm SiO_2 film was grown on silicon wafers by wet oxidation. The source and drain windows were defined by wet etching and doped by phosphorous diffusion. The HfO_2 films were deposited by RF magnetron sputtering in argon ambient at room temperature. The flow rate of argon was 13.5 standard cubic centimeters per minute (sccm). The total pressure during deposition was 20 mtorr. The refractive

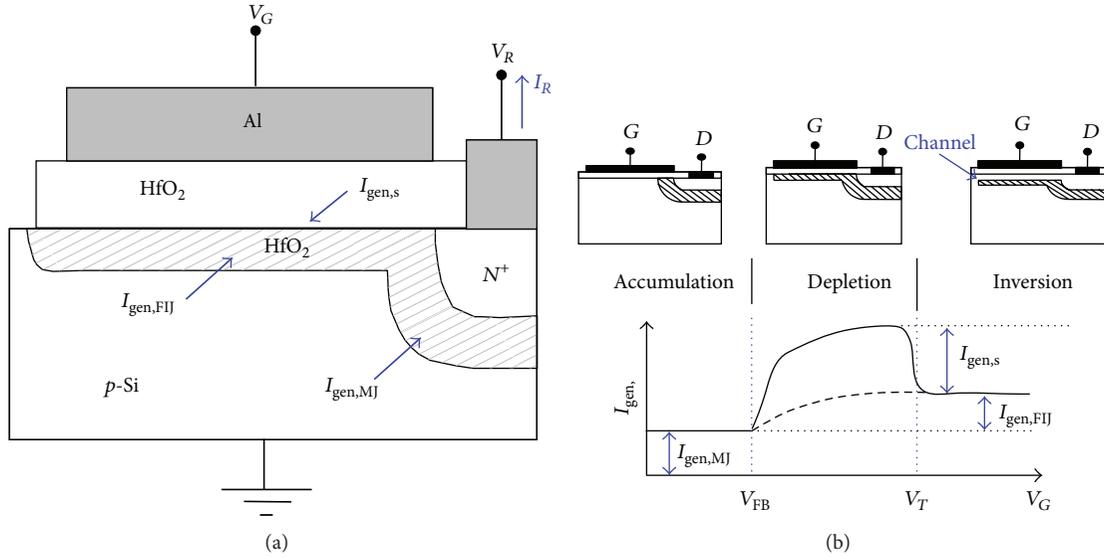


FIGURE 1: (a) Cross-sectional diagram of an HfO₂ gated diode. (b) Effect of the depletion region on the reverse current I_R of the gated diode at various gate voltages given a fixed reverse drain voltage V_R .

index, energy bandgap, and thickness of these thin films were measured by an N&K analyzer. The optical refractive index (n) and energy bandgap (E_G) were around 1.9–2.1 and 5.6–5.8 eV, respectively. The deposited thicknesses of HfO₂ thin films ranged from 12 nm to 47.1 nm. After HfO₂ deposition, the postdeposition anneal (PDA) was performed in either N₂ or N₂/O₂ (i.e., 50% N₂ and 50% O₂) with a flow rate of 3 sccm for 60 s at 500°C. According to the X-ray diffraction analysis, the HfO₂ films annealed at 500°C were amorphous. The aluminum (Al) electrodes were evaporated and patterned using a wet etching process. Postmetallization annealing (PMA) was performed at 400°C in N₂ for 30 s. The Al/HfO₂/p-Si MOS capacitors and MOSFETs were measured by Agilent 4156C semiconductor parameter analyzer and Agilent 4284A impedance analyzer. All the measurements were performed under dark condition. Based on the high-frequency (1 MHz) C-V measurements for the MOS capacitors, the effective dielectric constant of HfO₂ films annealed at 500°C in N₂ or N₂/O₂ was evaluated as 18.9 or 19.3, respectively (not shown here). In this work, the relatively large devices were chosen to avoid the short channel effects which may cause the distortion in analysis of surface state capture cross-section. The channel width (W) is 100 μm and the channel length (L) is 19 μm.

3. Results and Discussion

The drastic irregularity of the oxide/Si interface should introduce a large amount of density of states into the forbidden gap near the interface. The interface state may cause the charge trapping and lead to the device instability as well as the degradation of subthreshold swing, off-state current, carrier mobility, and oxide reliability. Charge carriers can be trapped or captured while they come to the physical vicinity of the center of the interface state. The capture cross-section (σ_s) of the center is a measure of how close the carrier has

to come to the center to be captured. In this work, the gated-diode method is used to identify the interface-trapped charge density (N_{it}), the surface recombination velocity (s_o), and the minority carrier lifetime (τ_{FIJ}) in the field-induced depletion region for the nMOSFET devices using HfO₂ gate dielectrics annealed at 500°C. The test structure described by Grove and Fitzgerald to investigate surface properties in MOS structures is identical to a MOSFET without or with an unconnected source region. In this work, the gated-diode measurement was made using a floating source and a grounded substrate on MOSFET structures, as shown in Figure 1(a). The drain is reversely biased with respect to the substrate ($V_R = V_{DB}$). According to the theory of gated-diode method, the reverse current of P-N junctions (I_R) is a function of the gate bias (V_G). The I_R - V_G characteristics may exhibit three distinct regions [10], as indicated in Figure 1(b). The reverse current of P-N junctions comes from the generation of electron-hole pairs at generation-recombination centers in the depletion region at room temperature. Hence, the magnitude of reverse current depends on the density of such centers and the volume of the depletion region. As the volume of the depletion region in gated diodes depends on the gate voltage, reverse current also depends on the gate voltage. The HfO₂/silicon interface is in the accumulation mode when V_G is less than the flat band voltage V_{FB} , and the reverse diode current originates from the generation-recombination centers in the depletion region of the metallurgical junction ($I_{gen,MJ}$). When $V_{FB} < V_G < V_T$ (where V_T is the threshold voltage), the field-induced junction is depleted, and the rapid increase in the reverse diode current is caused by the generation of electron-hole pairs at the generation-combination centers of the surface region ($I_{gen,s}$) and the field-induced junction depletion region ($I_{gen,FIJ}$). At $V_G > V_T$, the field-induced junction is in the inversion mode and the reverse diode current is reduced by the filling of the interface-trapped

charge states by the minority carriers. The magnitude of the reverse diode current is the sum of the generation currents in the depletion volume of the field-induced junction and in that of the metallurgical junction. Based on the Shockley-Read-Hall theory for the single-level centers [10], the equations for the gated-diode are written as follows [13–15]:

$$I_{\text{gen,MJ}} = qU_{\text{MJ}}WA_{\text{MJ}}, \quad (1)$$

$$I_{\text{gen,s}} = \frac{qn_i s_o A_g}{2}, \quad (2)$$

$$I_{\text{gen,FIJ}} = qU_{\text{FIJ}}A_g x_{d\text{max}} = \frac{qn_i A_g x_{d\text{max}}}{2\tau_{\text{FIJ}}}, \quad (3)$$

$$s_o = \sigma_s v_{\text{th}} N_{\text{it}} = \sigma_s v_{\text{th}} (\pi k T D_{\text{it}}), \quad (4)$$

$$W = \sqrt{\frac{2\epsilon_{\text{Si}} (N_A N_D)}{q(N_A + N_D)}} (V_{\text{bi}} + V_R), \quad (5)$$

$$x_{d\text{max}} = \sqrt{\frac{2\epsilon_{\text{Si}}}{qN_A}} (2\phi_F + V_R), \quad (6)$$

where $n_i = 9.65 \times 10^9 \text{ cm}^{-3}$ is the intrinsic carrier concentration in silicon [12]; A_{MJ} represents the area of the metallurgical junction; $A_g = 1.9 \times 10^{-5} \text{ cm}^2$ is the gate area; s_o is the surface recombination velocity; σ_s is the effective capture cross-section area; $v_{\text{th}} = 10^7 \text{ cm/s}$ is the thermal velocity; V_{bi} is the built-in potential of the P - N junction; ϕ_F is the quasi-Fermi potential of the majority carriers of the substrate; W is the width of the depletion region of the metallurgical junction; $x_{d,\text{max}}$ is the maximum width of the surface depletion region; $\tau_{0,\text{FIJ}}$ is the minority carrier lifetime in the field-induced depletion region; N_{it} is the interface-trapped charge density (i.e., density of the single-level surface generation-recombination centers per unit area); D_{it} is the interface-trapped charge density per area and energy (i.e., the density of uniformly distributed surface generation-recombination centers per unit area and energy); and U_{MJ} , U_s , and U_{FIJ} are the generation and recombination rates of carriers per unit volume in the depletion regions of the metallurgical, the surface region, and field-induced region, respectively.

Figure 2 shows the reverse diode current I_R versus V_G for the HfO_2 gated-diodes at $V_R = 2 \text{ V}$. Through the gated diode method, the surface recombination velocity (s_o) and the minority carrier lifetime (τ_{FIJ}) in the field-induced depletion region can be extracted. For HfO_2 films annealed in N_2/O_2 , s_o and τ_{FIJ} are determined to be $4.1 \times 10^3 \text{ cm/s}$ and 16 ns . On the other hand, for HfO_2 films annealed in N_2 , s_o and τ_{FIJ} are determined to be $8.9 \times 10^3 \text{ cm/s}$ and 22 ns . Obviously, the reverse diode current of nMOSFETs for HfO_2 annealed at 500°C in N_2/O_2 is smaller than that annealed in N_2 . The reduction in reverse current may be attributed to the decrease in oxygen vacancy related defects [16–19] in HfO_2 . The oxygen vacancy is one type of trapping centers and is easily formed in HfO_2 due to the transportation of oxygen atoms from HfO_2 into Si [18, 19]. During the thermal treatment of PDA in N_2/O_2 ambient, the oxygen atoms can

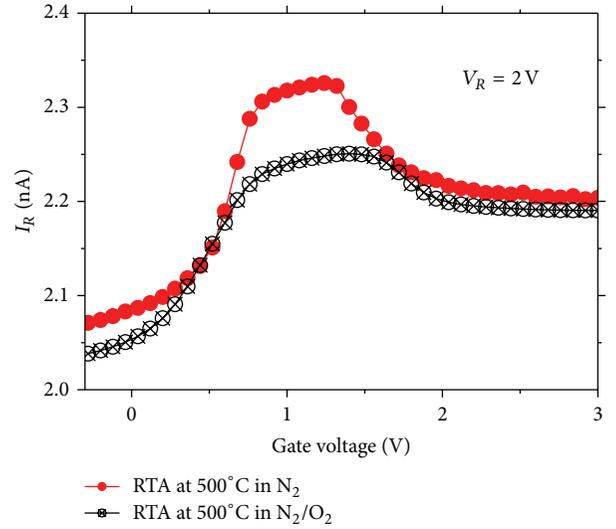


FIGURE 2: Reverse diode current I_R of the HfO_2 gated diode versus gate voltage V_G at $V_R = 2 \text{ V}$. V_R is the reverse bias of the N^+ region of the metallurgical junction.

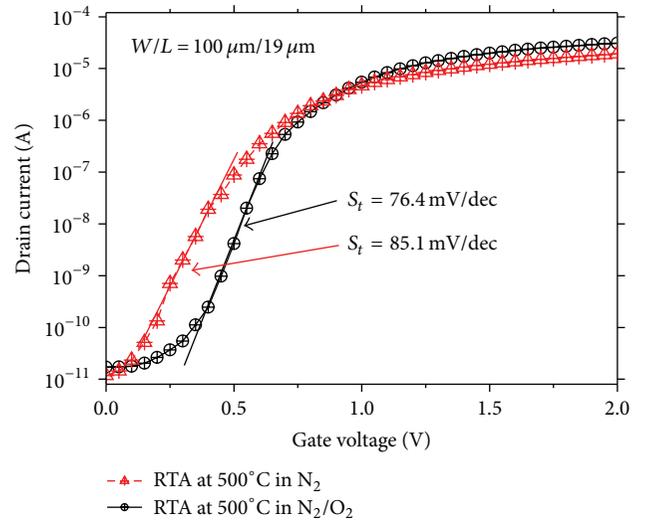


FIGURE 3: $I_{\text{DS}}-V_{\text{GS}}$ characteristics of nMOSFETs fabricated with HfO_2 gate dielectrics annealed in N_2 and N_2/O_2 at 500°C for 60 s.

diffuse into the HfO_2 films to partially passivate the existing oxygen vacancies. Hence, the reverse diode current can be reduced by N_2/O_2 annealing.

Figure 3 shows the $I_{\text{DS}}-V_{\text{GS}}$ characteristics. The $I_{\text{on}}/I_{\text{off}}$ ratio is larger than 10^6 at $V_D = 0.05 \text{ V}$, indicating that the nMOSFETs with amorphous HfO_2 gate dielectrics have a good current switch capability. The subthreshold swings (S_t) for the HfO_2 gate dielectrics annealed at 500°C in N_2 and N_2/O_2 are about 85.1 and 76.4 mV/dec, respectively. According to Figure 3, the density of interface traps per area and energy (D_{it}) can be determined from the subthreshold swing measurement, because S_t is expressed as $2.3(kT/q)[1 + (C_D + C_{\text{it}})/C_{\text{ox}}]$ [12], where C_D is the depletion-layer capacitance, C_{it} is the capacitance associated with the interface traps,

TABLE 1: Capture cross-section of surface states at the oxide/Si interface.

Oxide material	Capture cross-section	Deposition method	Measurement technique
SiO ₂	$1-4 \times 10^{-16} \text{ cm}^2$	Thermal oxidation	Charge pumping [22–24]
ZrO ₂	$5.8 \times 10^{-16} \text{ cm}^2$	rf sputtering	Gated diode [25]
Al ₂ O ₃	$1.7 \times 10^{-15} \text{ cm}^2$	PECVD	DLTS [26]
CeO ₂	$8.7 \times 10^{-15} \text{ cm}^2$	rf sputtering	Gated diode [27]
CeO ₂	$9.0 \times 10^{-15} \text{ cm}^2$	rf sputtering	Charge pumping [28]
HfO ₂	$9.4 \times 10^{-15} \text{ cm}^2$	ALD	Charge pumping [29]
HfO ₂	$2.4 \times 10^{-15} \text{ cm}^2$	rf sputtering	Gated diode (this work)

PECVD: plasma-enhanced chemical vapor deposition, DLTS: deep-level transient spectroscopy, and ALD: atomic layer deposition.

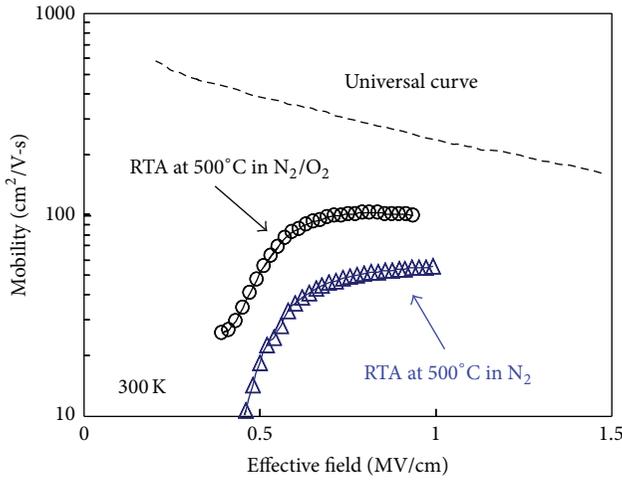


FIGURE 4: Channel electron mobility versus effective surface field for the HfO₂ MOSFETs annealed at 500°C for 60 s in N₂ and N₂/O₂.

and C_{ox} is the dielectric capacitance. The determined D_{it} is about 4.6×10^{12} and $2.1 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ for HfO₂ annealed at 500°C in N₂ and N₂/O₂, respectively. Once D_{it} is determined, σ_s and N_{it} can be extracted using (4). For HfO₂ annealed in N₂, σ_s and N_{it} are extracted to be about $2.4 \times 10^{-15} \text{ cm}^2$ and $3.7 \times 10^{11} \text{ cm}^{-2}$, respectively; for HfO₂ annealed in N₂/O₂, σ_s and N_{it} are extracted to be $2.4 \times 10^{-15} \text{ cm}^2$ and $1.7 \times 10^{11} \text{ cm}^{-2}$, respectively. It is worthy of note that the same σ_s value is obtained for HfO₂ annealed both in N₂ and in N₂/O₂. This finding may imply that the capture cross-section of surface states is an inherent nature at the HfO₂/Si interface. The universal constant of surface state capture cross-section is around $2.4 \times 10^{-15} \text{ cm}^2$.

Figure 4 shows the channel electron mobility versus the effective electric field. The effective surface field (E_{eff}) and effective channel mobility (μ_{eff}) can be expressed as $E_{\text{eff}} = (0.5Q_{\text{inv}} + Q_B)/\epsilon_{\text{Si}}$ and $\mu = (I_{\text{DS}}/V_{\text{DS}})(L/W)/Q_{\text{inv}}$, respectively, where Q_{inv} is the inversion layer charge, Q_B is the bulk depletion layer charge, and ϵ_{Si} is the dielectric constant of Si. The linear approximation of Q_{inv} , $Q_{\text{inv}} = C_{\text{ox}}(V_{\text{GS}} - V_T)$, is used in evaluating the mobility. The rest of the symbols have been defined earlier. The maximum channel electron mobility for the HfO₂ annealed in N₂/O₂ and N₂ was determined to be 102 and 43 cm²/V s, respectively. Evidently the HfO₂ film

annealed in N₂ shows lower channel electron mobility than the film annealed in N₂/O₂ condition. In addition, the HfO₂ device has a lowered mobility as compared to a universal mobility curve in SiO₂ MOSFETs [20]. The lowered mobility may come from the larger surface states which cause the increased interface charge scattering [21].

Table 1 lists the capture cross-sections of surface states (σ_s) at the interface between silicon and oxides, for example, SiO₂, ZrO₂, Al₂O₃, CeO₂, and HfO₂ [22–29]. For SiO₂, the σ_s value is $1-4 \times 10^{-16} \text{ cm}^2$ [22–24] which is smaller than those of high-k dielectrics. For CeO₂, the σ_s value is around $9 \times 10^{-15} \text{ cm}^2$ even if the adopted measurement method is different [27, 28]. In this work, the experimental results show that the HfO₂ films annealed in N₂/O₂ have lower interface state density (N_{it}) and higher channel electron mobility (μ_e) compared to the HfO₂ films annealed in N₂. Although the different PDA conditions lead to the different values of N_{it} and μ_e , the same σ_s for HfO₂ deposited by rf magnetron sputtering is obtained to be around $2.4 \times 10^{-15} \text{ cm}^2$. This finding may suggest that the capture cross-section of surface states for some thin film deposition method may be an inherent nature at the interface between silicon and hafnium oxide. It is worthy to note that the capture cross-section of surface states may be influenced by the factors of environment temperature, film thickness, film deposition method, and especially surface preparation of Si substrate prior to HfO₂ deposition.

4. Conclusions

The electrical properties at the HfO₂/Si interface are investigated by the gated-diode method and the subthreshold measurement. Although the HfO₂ films annealed in N₂/O₂ result in lower interface state density and higher channel electron mobility compared to the HfO₂ films annealed in N₂, the determined surface state capture cross-section at the HfO₂/Si interface is the same. This suggests that the surface state capture cross-section may be an inherent nature at the interface between silicon and hafnium oxide.

Conflict of Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

Acknowledgment

The author would like to thank the National Science Council of Taiwan, for supporting this work under Contract no. NSC 102-2221-E-015-MY2.

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Research Article

Comparison of Microstructural and Morphological Properties of Electrodeposited Fe-Cu Thin Films with Low and High Fe : Cu Ratio

Umut Sarac¹ and M. Celalettin Baykul²

¹ Department of Elementary Education, Bartın University, 74100 Bartın, Turkey

² Department of Physics, Eskişehir Osmangazi University, 26480 Eskişehir, Turkey

Correspondence should be addressed to Umut Sarac; usarac428@hotmail.com

Received 25 May 2013; Revised 12 August 2013; Accepted 27 August 2013

Academic Editor: Fu-Chien Chiu

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Fe-Cu films with low and high Fe : Cu ratio have been produced from the electrolytes with different Fe ion concentrations at a constant deposition potential of -1400 mV versus saturated calomel electrode (SCE) by electrodeposition technique onto indium tin oxide (ITO) coated conducting glass substrates. It was observed that the variation of Fe ion concentration in the electrolyte had a very strong influence on the compositional, surface morphological, and microstructural properties of the Fe-Cu films. An increase in the Fe ion concentration within the plating bath increased the Fe content, consequently Fe : Cu ratio within the films. The crystallographic structure analysis showed that the Fe-Cu films had a mixture of face-centered cubic (fcc) Cu and body centered cubic (bcc) α -Fe phases. The average crystallite size decreased with the Fe ion concentration. The film electrodeposited from the electrolyte with low Fe ion concentration exhibited a morphology consisting of dendritic structures. However, the film morphology changed from dendritic structure to cauliflower-like structure at high Fe ion concentration. The surface roughness and grain size were found to decrease significantly with increasing Fe ion concentration in the electrolyte. The significant differences observed in the microstructural and morphological properties caused by the change of Fe ion concentration in the electrolyte were ascribed to the change of Fe : Cu ratio within the films.

1. Introduction

The fabrication of electrodeposited thin film multilayers or granular alloys consisting of magnetic and nonmagnetic metals has attracted great interest due to their technological applications [1]. Among them, Fe-Cu films find applications in electronic industry [2]. Electrodeposition is a versatile growth process for the fabrication of metallic thin film materials, which find applications in electronics, magneto-electronics, magnetic recording, and microsystems industries due to its some unique features [3-7]. Aside from this, electrodeposition process also provides the deposition under ambient temperature and pressure and does not require relatively expensive equipment [6, 8]. It is well known that a small change in the growth parameters has a strong influence on the properties of the electrodeposited films.

It has been shown that the composition of electrolyte is one of the most important growth parameters affecting strongly the properties of the electrodeposited thin film materials deposited onto indium tin oxide (ITO) coated glass substrates [9-11]. In previous works, we investigated the properties of electrodeposited Fe-Cu films grown onto ITO coated glass substrates at different electrolyte temperatures and current densities [12, 13]. However, the effect of Fe : Cu ratio caused by the change of Fe ion concentration in the electrolyte on the structural and morphological properties of Fe-Cu films prepared onto ITO coated glass substrates has not been reported. The surface morphology of the films produced by electrodeposition technique is critically important and it can be controlled by varying the deposition parameters. Therefore, in this research, electrodeposited Fe-Cu films with low and high Fe : Cu ratio were produced from

the electrolytes with low and high Fe ion concentrations onto ITO coated glass substrates under potentiostatic conditions. The variations of the microstructures, compositions, and morphologies of the films were analyzed with respect to Fe ion concentration in the electrolyte. In this study, it is shown that the Fe ion concentration in the electrolyte has a significant effect on the microstructural, compositional, and surface morphological properties of electrodeposited Fe–Cu thin films.

2. Materials and Methods

Fe–Cu specimens were grown from the electrolytes composed of low, intermediate, and high Fe ion concentrations (0.02, 0.04, and 0.08 M, resp.), but the same Cu sulfate (0.01 M) and boric acid (0.1 M) concentrations. All chemicals were dissolved in deionized water. The bath temperature and pH were $25 \pm 1^\circ\text{C}$ and 3.8 ± 0.1 , respectively. Although the pH of the electrolytes decreased during the electrodeposition process of the films, we did not use any additive in order to obtain the stable electrolyte pH because of its possible effect on the electrodeposition process. For the deposition process, the electrodeposition system consisting of a potentiostat/galvanostat (VersaSTAT 3) with a conventional three-electrode electrochemical cell was used. Throughout the electroplating process, a saturated calomel electrode (SCE) was served as the reference electrode. A platinum wire and indium tin oxide (ITO) coated conducting glass substrate were used as counter electrode and working electrodes, respectively. The working area was about 0.8 cm^2 . The ITO electrodes were cleaned with acetone followed by ethanol and then ultrasonically rinsed for 10 min in water before deposition of the films. In all cases, the films were produced at a constant deposition potential of -1400 mV versus SCE, and the electroplating time was controlled to obtain equal cathodic charge. In the present study, the thickness of all films was set around 500 nm.

The structure of Fe–Cu deposit samples was characterized by means of Panalytical–Empyrean XRD diffractometer using $\text{CuK}\alpha$ radiation ($\lambda = 0.154059\text{ nm}$). The XRD data were recorded in a range from 42° to 54° with a step width of 0.02° . The elemental constitutions were analyzed using an energy dispersive X-ray spectroscopy (EDX). The surface morphological structure of resultant films was studied with the help of Zeiss Supra 50 Vp model SEM and AFM (Veeco Multimode V) techniques. To avoid possible oxidation of the surfaces, surface topographic images were obtained immediately after the production process at ambient temperature and pressure.

3. Results and Discussion

The electrodeposition of Fe–Cu films has been carried out from the electrolytes containing low, intermediate, and high Fe ion concentrations. Firstly, the potentiostatic current–time transients for the Fe–Cu films electrodeposited from electrolytes with low and high Fe ion concentrations were employed as a function of electroplating time during the

electroplating process in order to study the stability of electrodeposition of the Fe–Cu films. The potentiostatic current–time transients of the films grown from the electrolytes with low and high Fe ion concentrations recorded for the first 50 s of electroplating process are illustrated in Figure 1. It is clearly seen that the current density remains almost stable, indicating that the proper films are electrodeposited from the electrolytes with different Fe ion concentrations at a constant deposition potential. As can be seen from Figure 1, the current density was also observed to decrease towards more negative values as the Fe ion concentration in the electrolyte increased.

As a second step of this investigation, the elemental analysis of the films was done using EDX with respect to Fe ion concentration in the electrolyte. The film produced from the electrolyte with low Fe ion concentration consists of 33.5 at.% Fe and 66.5 at.% Cu. However, for the film electrodeposited from the electrolyte with high Fe ion concentration, the composition is 80.2 at.% Fe and 19.8 at.% Cu. These results reveal that an increase in the Fe ion concentration in the electrolyte increases the Fe:Cu ratio within the films. As mentioned above, the value of the current density decreased towards more negative values with increasing Fe ion concentration in the electrolyte. Thus, a decrease in the current density towards more negative values with the Fe ion concentration in the electrolyte leads to Fe–Cu film with higher Fe:Cu ratio. It has been shown that the Fe–Cu films are Fe-rich as the films are produced at more negative current densities [13]. On the other hand, the ratio of Fe:Cu within the films is found to be lower than the ion concentration ratio of $\text{Fe}^{+2}:\text{Cu}^{+2}$ in the electrolyte. The possible reason for this effect may be preferential Cu reduction process within the electrolyte containing the Fe and Cu ions, since Cu is a more noble metal [14]. Consequently, according to results obtained from the EDX measurements, it can be obviously said that the Fe:Cu ratio within the films is affected significantly by the Fe ion concentration in the electrolyte.

XRD measurements were performed in order to study the effect of Fe ion concentration on the crystal structure of the electrodeposited Fe–Cu films. XRD patterns of Fe–Cu films electrodeposited from the electrolytes with low and high Fe ion concentrations are presented in Figure 2. As the fcc Cu peak positions are distinct from those of bcc Fe, it is easy to determine and compare the bcc versus fcc phase in the film [15]. In the XRD patterns, diffraction peaks related to the fcc Cu (111), fcc Cu (200), and bcc Fe (110) are observed irrespective of Fe ion concentration studied in the experiment. These results obtained from the XRD patterns pointed to the coexistence of fcc Cu (111) and bcc α -Fe (110) phases. It has been shown that the structure of the Fe particles in Cu matrix is strongly related to the Fe content depending on the growth technique [16, 17]. In equilibrium, the Fe and Cu elements have very small mutual solid solubility, and the equilibrium Fe–Cu phase diagram does not exhibit intermediate phases [18]. The iron is incorporated in the fcc–Cu structure, giving rise to a Cu-based fcc Fe–Cu solid solution for high Cu content. A single phase bcc structure is obtained for Fe–Cu films for high Fe content. However, the films show mixed fcc and bcc phase in intermediate

composition range [15–17]. In electrodeposited Fe–Cu films, the structure of Fe grains in Cu matrix is bcc as the Fe content within the films is higher than 30%, while the structure of them is fcc for the Fe content lower than 27% [19]. Thus, in the present study, it is concluded that the Fe–Cu films electrodeposited onto ITO coated glass substrates from the electrolytes with low and high Fe ion concentrations consist of a mixture of fcc Cu and bcc Fe particles with respect to their Fe content. These results obtained about our electrodeposited Fe–Cu films are in good agreement with the results found in previous published papers [12, 13, 20]. On the other hand, it is found from the XRD patterns given in Figure 2 that the relative intensity of bcc Fe (110) diffraction peak increases with the Fe ion concentration in the electrolyte. In opposition to that, a decrease in the relative intensity of fcc Cu (111) and Cu (200) diffraction peaks with increasing Fe ion concentration in the electrolyte is also observed, as can be clearly seen from Figure 2. These differences observed in the structural properties can be ascribed to the increase of Fe : Cu ratio within the films with increasing Fe ion concentration in the electrolyte.

The average crystallite size in the direction perpendicular to the plane of the sample was analyzed by application of Scherrer's formula [21]. The increase of Fe ion concentration in the electrolyte induces change in the full width at half maximum (FWHM) of the diffraction peaks. The average crystallite sizes for the bcc Fe (110) peaks are determined to be 35 and 26 nm for the films electrodeposited from the electrolytes with low and high Fe ion concentrations, respectively, indicating a nanocrystalline structure of the films. This result also reveals that the average crystallite size of the films decreases with increasing Fe ion concentration in the electrolyte. As seen in Figure 1, the current density decreased towards more negative values as the Fe ion concentration within the electrolyte increased. Thus, it is expected that a decrement of the current density towards more negative values observed at high Fe ion concentration increases the nucleation densities and consequently reduces the crystallite size [13, 22–25].

SEM measurements were performed to characterize the effect of Fe ion concentration on the surface morphology of Fe–Cu films. It is observed that the electrodeposited Fe–Cu films prepared from the electrolytes with low and high Fe ion concentrations have also different morphological features. SEM topographic images of electrodeposited Fe–Cu films grown from the electrolytes with low and high Fe ion concentrations are shown in Figure 3(a) and b, respectively. Figure 3(c) shows the SEM image of Fe–Cu film electrodeposited from the electrolyte with high Fe ion concentration at lower magnification. It is clearly seen that the surfaces of the films exhibit a compact and crack-free morphology. As shown from Figure 3, there is notable change in the surface morphology of Fe–Cu films with respect to Fe ion concentration in the electrolyte. It is also clearly seen that the film grown from the electrolyte with low Fe ion concentration exhibits a morphology having dendritic structures (Figure 3(a)). The dendritic growth observed in the electrodeposited Fe–Cu film prepared from the electrolyte with low Fe ion concentration may be attributed to

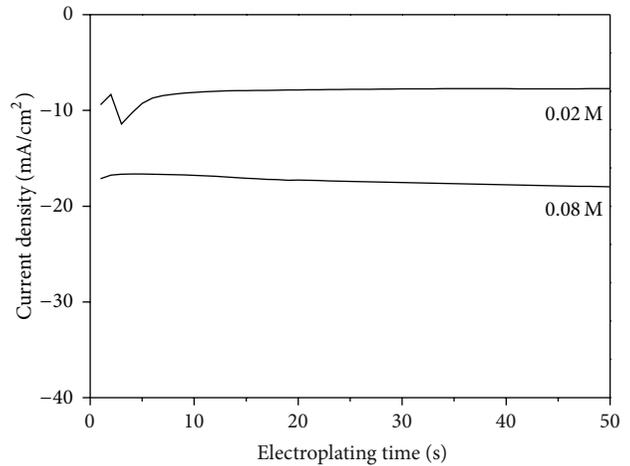


FIGURE 1: Potentiostatic current–time transients of the Fe–Cu films electrodeposited from the electrolytes with low and high Fe ion concentrations.

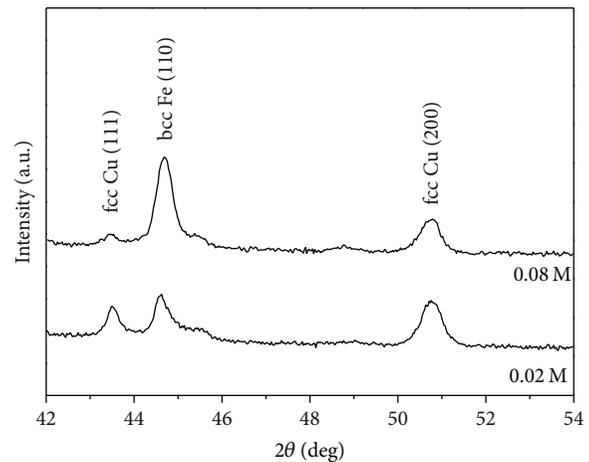


FIGURE 2: XRD patterns of electrodeposited Fe–Cu films prepared from the electrolytes with low and high Fe ion concentrations.

the high Cu content within the film. Dendritic growth of electrodeposited films with high Cu content was ascribed to the diffusive growth mechanism of Cu [14, 26]. On the other hand, on the surface of the film grown from the electrolyte with high Fe ion concentration, the dendritic structures disappear (Figure 3(b)). Such a disappearance of the dendritic structures for the film deposited from the electrolyte with high Fe ion concentration may be due to the change of major component of the film from Cu to Fe as confirmed by the EDX measurements. It can be clearly seen that the surface of the film prepared from the electrolyte with high Fe ion concentration is smoother and more uniform than that of the film grown from the electrolyte with low Fe ion concentration (Figure 3(b)); however, the cauliflower-like structures formed due to the agglomeration of the smaller grains are also observed in some regions on the surface as seen from Figure 3(c). According to results obtained from the SEM and EDX analyses, it is concluded that the surface

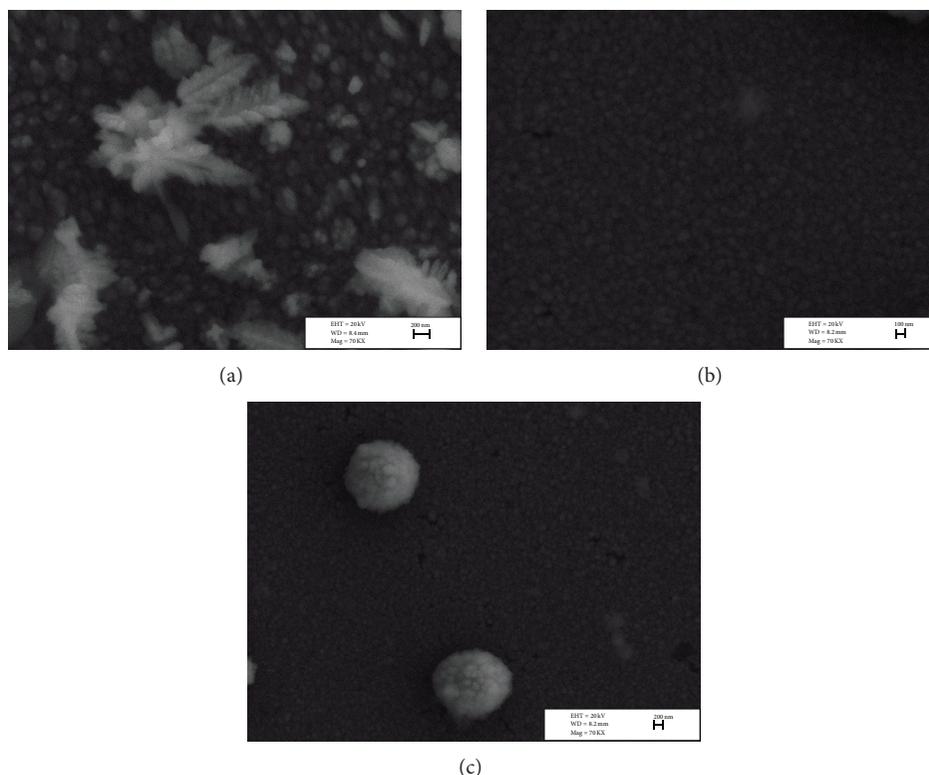


FIGURE 3: SEM topographic images of Fe–Cu films electrodeposited from the electrolytes with low and high Fe ion concentrations (a) 0.02 M, (b) 0.08 M, and (c) 0.08 M at lower magnification, respectively.

morphological structure of electrodeposited Fe–Cu films is affected strongly by the change of Fe:Cu ratio within the films caused by the change of Fe ion concentration in the electrolyte. The film morphology changes from a dendritic structure to a cauliflower-like structure by the increase of Fe:Cu ratio within the films. Similar changes in the surface morphology have been also observed in very recent studies performed about electrodeposited Fe–Cu films prepared at different growth conditions and have been also attributed to the compositional differences [12, 13].

Significant changes observed in the surface morphology with the Fe:Cu ratio may be also related to the amount of hydrogen evolution reaction. As shown in Figure 1, the current density is more negative as the Fe–Cu film is produced from the electrolyte with higher Fe ion concentration. At more negative current densities and/or more negative cathode potentials, the hydrogen evolution reaction takes place and it is vigorous enough to change the electrochemical conditions at the vicinity of the cathode, which gives rise to change of morphological structure [27, 28]. Thus, it is concluded that the reason of the differences observed in the morphological structure with respect to Fe:Cu ratio may be also attributed to the increase of the hydrogen evolution reaction with increasing Fe ion concentration in the electrolyte. In recent studies, the changes of surface morphology of metal films produced by electrodeposition technique at different growth conditions have been also related to the amount of hydrogen evolution reaction [29–33].

The surface morphology of electrodeposited Fe–Cu films prepared from the electrolytes with different Fe ion concentrations was also studied using an AFM. Two- and three-dimensional AFM images over a scan area of $1\ \mu\text{m} \times 1\ \mu\text{m}$ and one-dimensional line scans of the films deposited from the electrolytes with low, intermediate, and high Fe ion concentrations are shown in Figures 4(a), 4(b), and 4(c), respectively. Fe–Cu films exhibited granular growth morphology irrespective of Fe ion concentration as seen in Figure 4. The one-dimensional line scans given also in Figure 4 show that the height and the width of the grains are considerably affected by the Fe ion concentration in the electrolyte. It is clearly seen that both the height and the width of the grains decrease as the Fe ion concentration in the electrolyte increases. Accordingly, it can be concluded that an increase in Fe ion concentration in the electrolyte leads to higher nucleation density and thus encourages the formation of smaller grains on the film surface. The AFM image shown in Figure 4(c) for the film grown from the electrolyte with high Fe ion concentration confirms the existence of the smaller grains. It is well known that the surface roughness of electrodeposited thin films is generally related to the grain size [34]. The variation of the average and the root-mean square (RMS) surface roughness in Fe–Cu films as a function of Fe ion concentration in the electrolyte is illustrated in Figure 5. The root-mean square (RMS) surface roughness values are determined to be 71.4, 43, and 18.2 for the films electrodeposited from the electrolytes with low, intermediate, and high Fe ion concentrations,

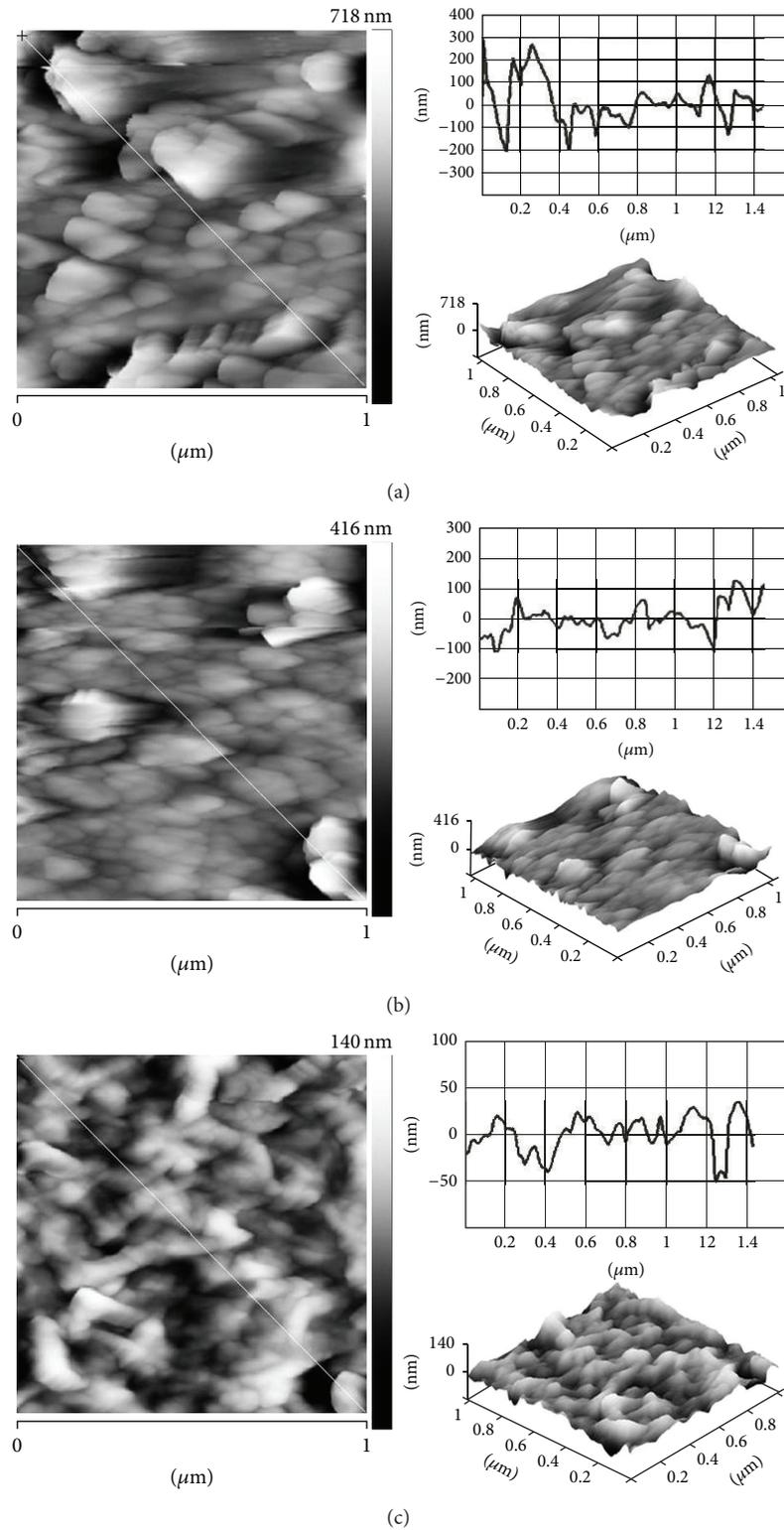


FIGURE 4: Two- and three-dimensional AFM topographic images and one-dimensional line scans of electrodeposited Fe-Cu films grown from the electrolytes with low, intermediate, and high Fe ion concentrations (a) 0.02 M (b) 0.04 M, and (c) 0.08 M, respectively.

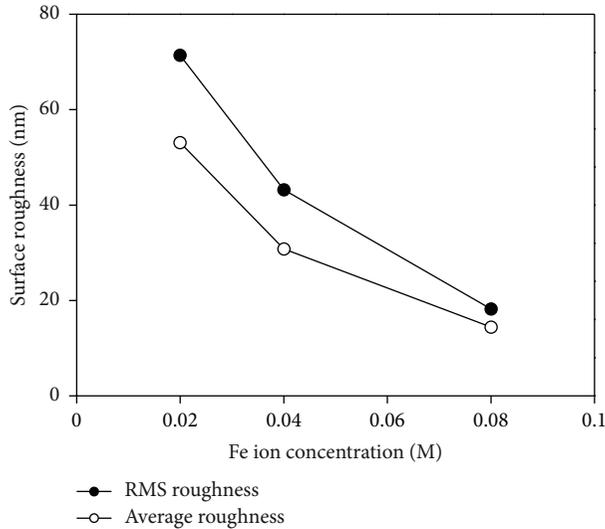


FIGURE 5: The variation of the average and the rms surface roughness in Fe-Cu films as a function of Fe ion concentration in the electrolyte. All lines are guide for the eye.

respectively, indicating the surface roughness of the films decreases strongly with increasing Fe ion concentration in the electrolyte. As a result, the surface roughness of the films decreases significantly with the increase of Fe ion concentration in the electrolyte, and finally the film exhibits a morphology having of smaller grains.

4. Conclusions

We examined and reported-the-variations of the microstructures, compositions, and morphologies of electrodeposited Fe-Cu films with low and high Fe:Cu ratio synthesized onto ITO coated glass substrates from the electrolytes with different Fe ion concentrations. The variation of the Fe ion concentration in the electrolyte changed the Fe:Cu ratio within the films and, hence strongly affected the microstructural and morphological properties of the films. XRD results showed the existence of separated fcc Cu and bcc Fe phases. The relative intensity of the fcc Cu (111) and Cu (200) peaks decreased, whereas the relative intensity of bcc Fe (110) peak increased as the Fe ion concentration in the electrolyte increased. The average crystallite size of the films decreased as the Fe ion concentration in the electrolyte increased. At low Fe ion concentration, the dendritic structures on the film surface were observed; however, the cauliflower-like structures appeared on the surface of the film at high Fe ion concentration due to the change of the Fe:Cu ratio within the films. Fe-Cu film electrodeposited from the electrolyte with high Fe ion concentration exhibited a relatively smooth surface. At low Fe ion concentration, the surface become rougher. The RMS surface roughness was found to decrease significantly from 71.4 to 18.2 nm with increasing Fe ion concentration in the electrolyte. There was also a significant decrease in average grain size as the Fe ion concentration in the electrolyte increased, and finally the film surface

morphology consisted of smaller grains. Accordingly, the significant differences observed in the morphological and microstructural properties might be related to the change of Fe:Cu ratio within the films, which can be controlled by the change of Fe ion concentration in the electrolyte.

Acknowledgments

This work was financially supported by the Scientific Research Projects Commission of Eskisehir Osmangazi University under the project number 200819039. The authors gratefully acknowledge Mustafa Arkel for technical help during the AFM measurements. The authors thank K. O. Ay for providing the EDX measurements. Thanks also go to the Bilecik Şeyh Edebali University, Turkey, for XRD measurements and Anadolu University, Department of Materials Science and Engineering, Turkey, for SEM measurements.

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