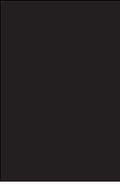


Advanced RF and Analog Integrated Circuits for Fourth Generation Wireless Communications and Beyond

Guest Editors: Ramesh Pokharel, Leonid Belostotski,
Akira Tsuchiya, Ahmed Allam, and Mohammad S. Hashmi





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Editorial

Advanced RF and Analog Integrated Circuits for Fourth Generation Wireless Communications and Beyond

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Fourth generation wireless communications are approaching to market, and recent innovations are at peak to come up with RF and analog circuit solutions to provide low power and high speed tiny chips at very low cost. This special issue presents the researches and technical know-how suitable for critical advanced researches in ICs development. After rigorous review of numerous research and review articles, this special issue finalizes one review article and three research articles which address the recent developments in IC design and are suitable for publication in this peer journal.

Oscillators are one of the most critical components of transceiver, and designing low phase noise oscillators operating at several GHz is a challenging task. To help researchers understand the design implementation and its performance with different topologies and architectures, the recent advances in CMOS VCOs are discussed. Recently, innovations in CMOS oscillators have extended to higher end of millimeter-wave region maintaining their performance comparable to microwave oscillators.

Present and future communication systems demand that electronic devices be suitable for a range of applications with different bandwidth, speed, and accuracy. This necessitates the need for reconfigurable devices, and to cover this flavor, innovation in reconfigurable LNA for UWB receivers has been addressed. This LNA exploits the programmable circuit to control the mode of operation and with current reuse

improves the gain and flatness. The designed LNA operates in two subbands of MB-OFDM UWB, UWB mode-1 and mode-3, as a single or concurrent mode.

Miniaturization is the key for CMOS technology and bulky inductors are the main hindrance. Therefore, circuit topology without a bulky inductor is highly desired and promoted. Inductorless PLL with subharmonic pulse injection locking has been introduced. A half-integral subharmonic locking technique helped to improve phase noise characteristics.

Although, recent developments and scaling of CMOS technology are pushing the signal processing into digital domain, the hard truth is that the real world is analog, and, therefore, analog-to-digital converter is an integral part of chip design. Delta-sigma modulator is gaining more and more attention and popularity because of its potential to achieve high resolution and high speed. Continuous-time delta-sigma modulator helps to design low power modulator, and hence a systematic design methodology to design such modulator is presented.

Acknowledgments

We hope our readers can enrich their knowledge through our variety of papers, and we would like to thank all our editors,

reviewers, and technical staffs who are directly or indirectly involved in making this special issue concisely informative and successful.

Ramesh Pokharel
Leonid Belostotski
Akira Tsuchiya
Ahmed Allam
Mohammad S. Hashmi

Research Article

CMOS Ultra-Wideband Low Noise Amplifier Design

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This paper presents the design of ultra-wideband low noise amplifier (UWB LNA). The proposed UWB LNA whose bandwidth extends from 2.5 GHz to 16 GHz is designed using a symmetric 3D RF integrated inductor. This UWB LNA has a gain of 11 ± 1.0 dB and a NF less than 3.3 dB. Good input and output impedance matching and good isolation are achieved over the operating frequency band. The proposed UWB LNA is driven from a 1.8 V supply. The UWB LNA is designed and simulated in standard TSMC 0.18 μm CMOS technology process.

1. Introduction

CMOS technology is one of the most prevailing technologies used for the implementation of radio frequency integrated circuits (RFICs) due to its reduced cost and its compatibility with silicon-based system on chip [1]. The use of ultra-wideband (UWB) frequency range (3.1–10.6 GHz) for commercial applications was approved in February 2002 by the Federal Communications Commission. Low cost, reduced power consumption, and transmission of data at high rates are the advantages of UWB technology. UWB technology has many applications such as wireless sensor and personal area networks, ground penetrating radars, and medical applications [2].

Low noise amplifier is considered the backbone of the UWB front-end RF receiver. It is responsible for signal reception and amplification over the UWB frequency range. LNA has many desired design specifications such as low and flat noise figure, high and flat power gain, good input and output wide impedance matching, high reverse isolation, and reduced DC power consumption [1, 3].

Nowadays one of the most suitable configurations suggested for LNA implementation is current reuse cascaded

amplifier. This LNA configuration can attain low DC power consumption, high flattened gain, minimized NF, and excellent reverse isolation while achieving wide input and output impedance matching [1–3].

Radio frequency integrated inductors play a significant role in radio frequency integrated circuits (RFICs) implementation. Design, development, and performance improvement of RF integrated inductors represent a challenging work. Achieving high integration level and cost minimization of RFICs are obstructed because of the difficulties facing the RF integrated inductors designers which are related to obtaining high quality factors [4–6].

In this paper, the implementation of LNAs using 3D integrated inductors will be investigated. A symmetric 3D structure is proposed as a new structure of integrated inductors for RFICs.

This paper discusses the design procedure of current reuse cascaded UWB LNA and its bandwidth expansion. In addition, the employment of suggested symmetric 3D RF integrated inductor will be demonstrated. This paper is organized as follows. Section 2 introduces the suggested UWB LNA circuit. Section 3 gives simulation results and discussion. Conclusion is driven in Section 4.

2. Circuit Description

As shown in Figure 1, the proposed UWB LNA is a current reuse cascaded core based on a common source topology with a shunt resistive feedback technique implemented over the input stage.

This current reuse cascaded amplifier achieved good wideband input impedance matching through the use of source degeneration input matching technique. Figure 2 shows the small signal equivalent circuit of this LNA input stage. The input port of this UWB LNA is desired to match source impedance R_s at resonance frequency ω_o . This matching circuit bandwidth is defined through the quality factors of source degeneration and gain-peaking inductors (L_s and L_g) where the input impedance is given by

$$\begin{aligned} Z_{in} &= j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \omega_T L_s \\ &= j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + R_s, \end{aligned} \quad (1)$$

where Z_{in} is the UWB LNA input impedance and ω_T is the current-gain cut-off frequency, where $\omega_T = g_m/C_{gs}$ and g_m and C_{gs} are the input stage transconductance and gate-source capacitance, respectively. V_s represents the RF signal source. R_s is the output impedance of V_s .

Although the shunt resistive feedback loop leads to LNA noise performance degradation [7], it is widely used in recently proposed LNAs due to its superior wideband characteristics. Shunt capacitive-resistive feedback technique is employed to widen the input-matching bandwidth and increase the LNA stability.

Shunt-peaked amplifiers are known to have wide gain bandwidth and high low frequency power gain [8]. To have a high flattened gain of the proposed UWB LNA, shunt-peaking technique is used. In addition the gate-peaking technique is used to enhance the LNA gain at high frequencies. Besides the shunt- and gate-peaking techniques, the shunt resistive feedback loop is used in gain flattening [2, 8]. The LNA approximate gain is given by

$$\begin{aligned} A &\cong \frac{V_{out}}{V_s} \\ &\cong \frac{g_{m1}g_{m2} [R_L // (R_{d2} + sL_{d2})] [sL_{d1}]}{2 \cdot sC_{gs1} [s(L_{s1} + L_{g1}) + 1/sC_{gs1}]}. \end{aligned} \quad (2)$$

Ultra-wideband applications require good noise performance in addition to high and flat gain. Low noise design techniques which are suitable for narrowband applications cannot be used for wideband applications. Main contribution of cascaded matched stages noise figure is due to first stage [9]. The reduction of noise figure of input stage will lead to the reduction of the overall noise figure of the proposed design. Optimization and control of factors affecting the NF will improve this UWB LNA noise performance. An equivalent circuit of the input stage for noise factor calculation is shown in Figure 3 [1].

An estimated value of the noise figure ($NF = 10 \log_{10} f$) of this topology is given in [1] where f is the noise factor of the UWB LNA. The noise factor f can be given by

$$\begin{aligned} f &= 1 + \frac{R_g + R_{lg} + R_{ss} + R_{ls}}{R_s} + \frac{\delta\alpha\omega^2 C_{gs1}^2 R_s}{5g_{m1}} \\ &\quad + \frac{R_{FB} ((L_{g1} + L_{s1}) C_{gs1})^2}{R_s (g_{m1} R_{FB} - 1)^2} \\ &\quad \cdot \left[s^2 + s \left(\frac{\omega_{o,rfbn}}{Q_{rfbn}} \right) + \omega_{o,rfbn}^2 \right]^2 \\ &\quad + \frac{\gamma g_{m1} (R_{FB} + R_s)^2 ((L_{g1} + L_{s1}) C_{gs1})^2}{\alpha R_s (g_{m1} R_{FB} - 1)^2} \\ &\quad \cdot \left[s^2 + s \left(\frac{\omega_{o,dn}}{Q_{dn}} \right) + \omega_{o,dn}^2 \right]^2, \\ f &= 1 + \frac{R_g + R_{lg} + R_{ss} + R_{ls}}{R_s} + f_{gn} + f_{rfbn} + f_{dn}, \end{aligned} \quad (3)$$

where

$$\begin{aligned} \omega_{o,rfbn} &= \sqrt{\frac{1 + g_{m1} R_s}{(L_{g1} + L_{s1}) C_{gs1}}}, \\ Q_{rfbn} &= \frac{1}{R_s + \omega_{T1} L_{s1}} \cdot \sqrt{\frac{(1 + g_{m1} R_s) (L_{g1} + L_{s1})}{C_{gs1}}}, \\ \omega_{o,rfbn} &= \sqrt{\frac{1}{(L_{g1} + L_{s1}) C_{gs1}}}, \\ Q_{dn} &= \frac{1}{(R_s || R_{FB}) + \omega_{T1} L_{s1}} \cdot \sqrt{\frac{(L_{g1} + L_{s1})}{C_{gs1}}}, \end{aligned} \quad (5)$$

where f_{gn} , f_{dn} , and f_{rfbn} are gate, drain, and feedback resistor noise factors, respectively and α , δ , and γ are constants equal to 0.85, 4.1, and 2.21, respectively.

It is clear from (4) that, to reduce the noise figure, high quality factors of L_{s1} and L_{g1} are desired. It can also be noted that the noise factor is inversely proportional to feedback resistor R_f . In other words, weak feedback topology decreases the noise factor value while strong feedback implementation degrades the noise performance of the suggested UWB LNA.

In addition, the noise factor formula given by (4) states that the noise figure is also inversely proportional to the transconductance of the input stage (g_{m1}). This goes along with the known fact that noise performance trades off with power consumption.

For output matching, the series resonance of the shunt peaking technique is used to match the proposed UWB LNA to the load impedance R_L while the series drain resistance R_{d2} is used to extend the output matching bandwidth.

This proposed UWB LNA (LNA1) has an operating bandwidth of 3.1–10.6 GHz. The proposed LNA2 whose schematic

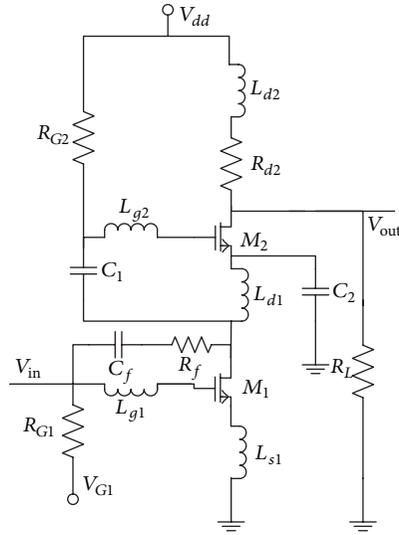


FIGURE 1: Current reuse UWB LNA (LNA1).

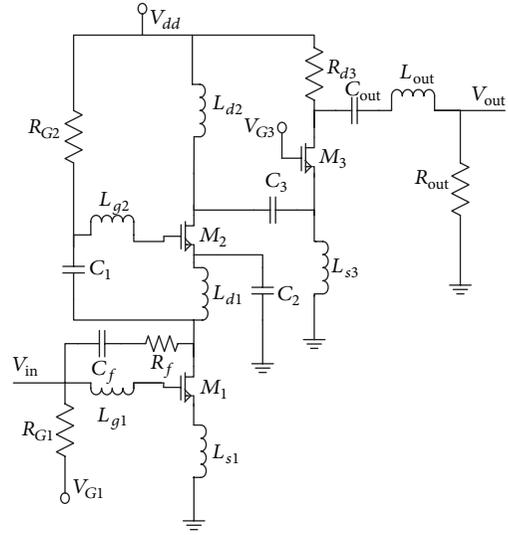


FIGURE 4: Schematic circuit of LNA2.

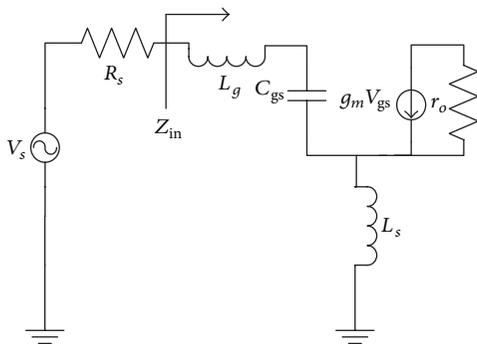


FIGURE 2: Input stage small signal equivalent circuit.

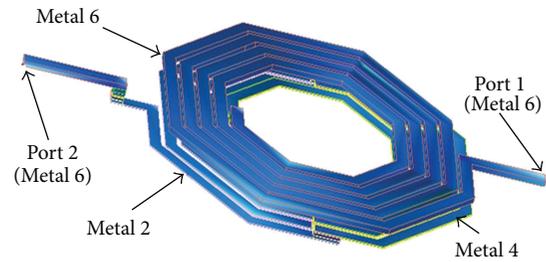


FIGURE 5: 3D view of the symmetric 3D proposed structure.

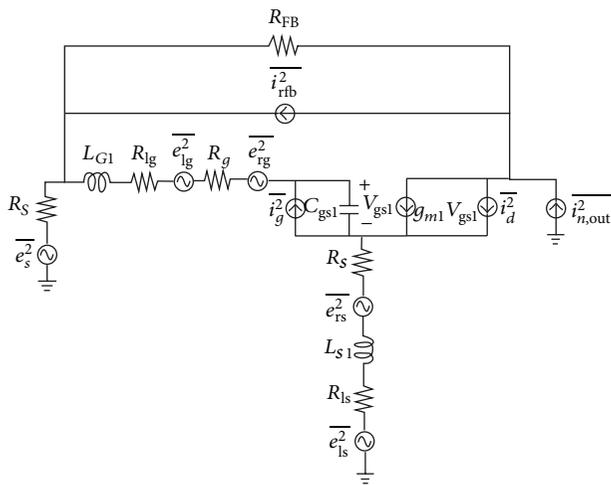


FIGURE 3: Equivalent circuit of the first stage for noise calculation [1].

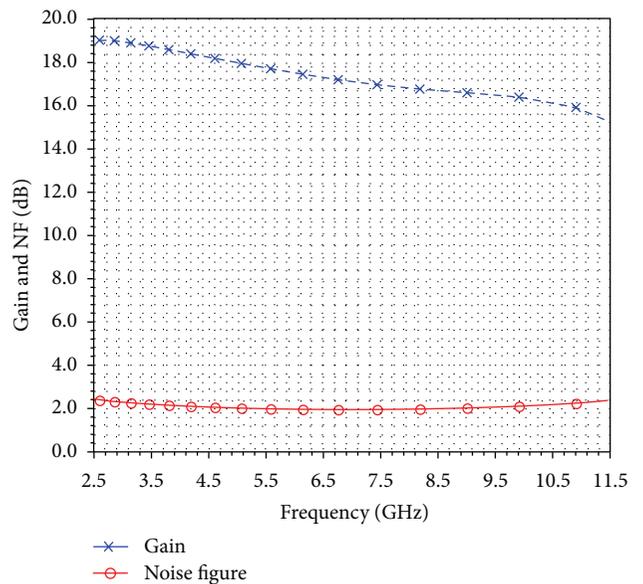


FIGURE 6: S_{21} (dB) and NF (dB) of LNA1.

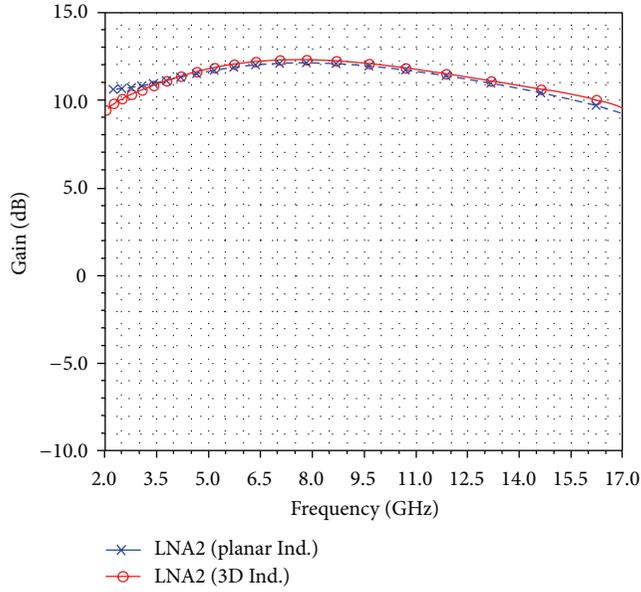
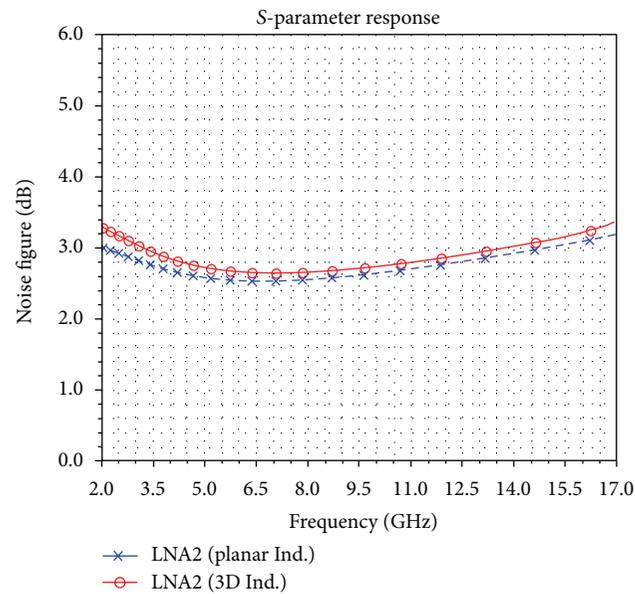
FIGURE 7: S_{21} (dB) of LNA2.

FIGURE 8: NF (dB) of LNA2.

circuit is shown in Figure 4 is an extended version of LNA1. It has a wider operating band of frequency which extends from 2.5 GHz to 16 GHz.

Input impedance match has a special importance and consideration especially in wideband sensitive circuits design. Input impedance matching bandwidth is broadened by the use of a weaker shunt capacitive-resistive feedback loop which mainly leads to quality factor reduction of the input matching circuit. Weakness of shunt feedback strength not only reduces the input reflection coefficient over this wide bandwidth but it also reduces the input side injected thermal noise which decreases the proposed LNA2 noise

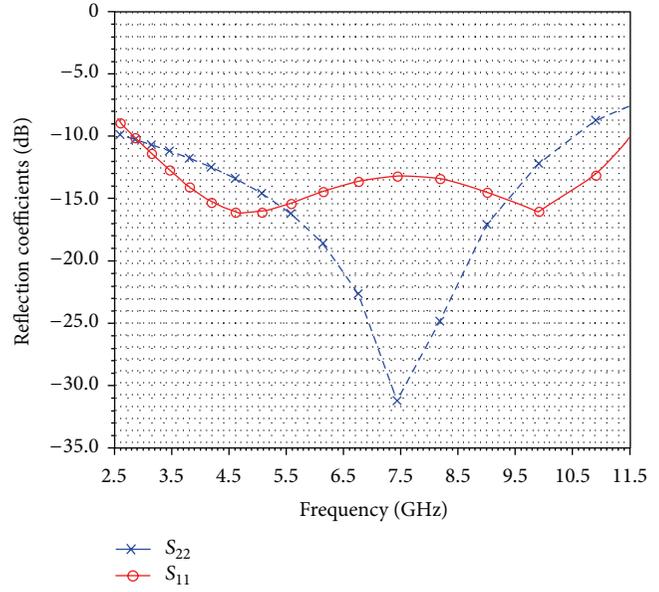
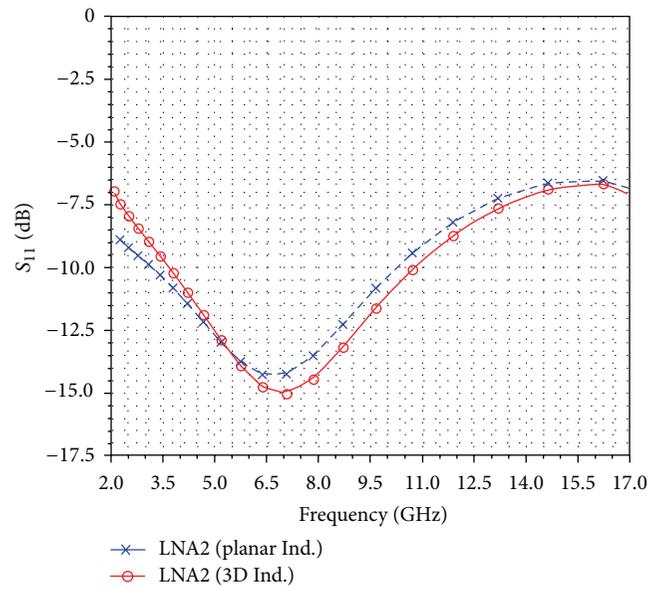
FIGURE 9: S_{11} (dB) and S_{22} (dB) of LNA1.FIGURE 10: S_{11} (dB) of LNA2.

figure indicating the enhanced noise performance of the suggested design.

Shunt-peaking technique increases the low frequency gain and hence decreases the gain flatness while having a wide operating bandwidth. In spite of shunt-peaking drawbacks, it mainly facilitates LNA output impedance to load matching. LNA2 bandwidth extension and gain flatness over its operating band of frequency are achieved through the removal of shunt peaking. Moreover the control of gate peaking is used to enhance the current reuse amplifier core gain.

For wideband output impedance matching, a unity common gate (CG) matching topology in addition to series

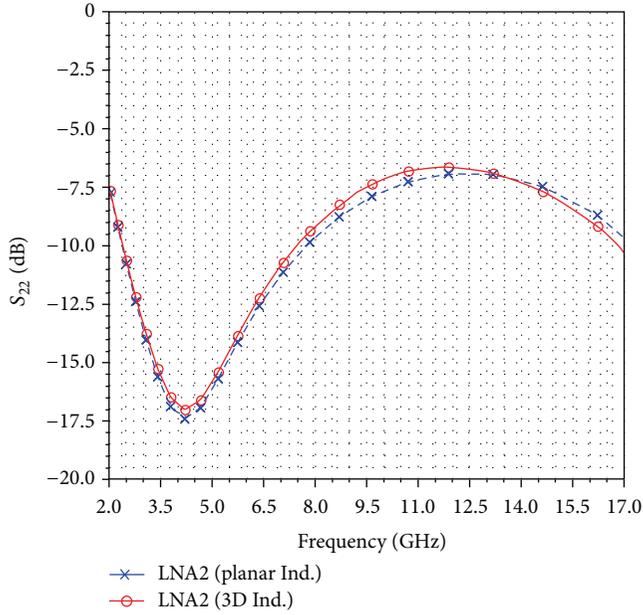


FIGURE 11: S_{22} (dB) of LNA2.

resonance circuit consisting of capacitor C_{out} and inductor L_{out} is used to match the LNA2 output impedance to its load (succeeding RF stage). The resistive termination R_{out} is used to control the load-output impedance match bandwidth.

A planar RF on-chip spiral inductor (L_{d1}) having an inductance of 14.5 nH and a maximum quality factor of 8.0 is needed as a load of the input CS stage to improve the current reuse stages matching. This RF integrated inductor occupies an area of $428 \mu\text{m} \times 425 \mu\text{m}$ which represents a considerable part of the UWB LNA total die area.

One of the well-known difficulties facing the development of RFICs is inductors large area relative to other passive and active components. This area problem becomes more severe with the recent intensive shrinking of active devices and competitive reduction of fabrication cost [10].

Inductors quality factor (Q) reduction is another limiting factor of RFICs performance enhancement. The reduction of inductor Q factor is due to ohmic and substrate losses. Ohmic losses can be decreased by using a high conductive metal for inductor implementation. On the other hand placing a high resistive layer underneath the inductor can minimize the substrate losses. Lately optimized 3D structures and implementations of RF integrated inductors are suggested to overcome all of these limitations and improve the RF integrated inductors performance [4, 5].

For LNA2 circuit area reduction and RF inductor characteristics improvement, a symmetric 3D structure for RF integrated inductor implementation is suggested to replace the planar RF integrated inductor (L_{d1}). Similar to the design of planar RF inductor, 3D metallic structure layout should be drawn on a substrate to design and test a 3D integrated inductor [11]. 3D RF inductors structures are mainly consisting of serially connected different metal layers spirals having the same current flow direction. This 3D structure inductance

is dependent on these different spirals inductances and the positive mutual coupling they have [11].

For 1P6M CMOS technology which has six different metal layers, the proposed symmetric 3D RF integrated inductor has a complete spiral inductor on the highest metal layer ($M6$). Half of the lower spiral is implemented using fourth metal layer ($M4$) to increase its inductance value due to the increased mutual coupling. The second metal layer ($M2$) which is distant from the top metal layer is employed to implement the lower spiral other half to reduce the parasitic components of that 3D metal structure and increase its quality factor. The suggested symmetric 3D inductor has an inductance of 14.5 nH, a quality factor of 8.5, and an area of $185 \mu\text{m} \times 165 \mu\text{m}$. 80% of planar inductor area is saved through this symmetric 3D structure while achieving the same inductance value and higher quality factor. Figure 5 shows a 3D view of the proposed symmetric RF integrated inductor.

3. Simulation Results and Discussion

The proposed UWB LNA (LNA1 and LNA2) circuits are designed in TSMC CMOS 0.18 μm technology process using Agilent Advanced Design System (ADS). Electromagnetic simulation is verified by the post-layout simulation results which are obtained using the Cadence design environment. The suggested symmetric 3D structure is designed and tested using Momentum simulation software and verified using Cadence design environment. The LNAs simulation results are given below.

3.1. Power Gain and Noise Figure. LNA1 has a gain of 17 ± 1.5 dB as shown in Figure 6. It also has a noise figure less than 2.3 dB over its operating band of frequency (3.1–10.6 GHz).

S_{21} (dB) of LNA2 is higher than 10 dB with a maximum value of 12 dB over the desired band of frequency (2.5–16 GHz). This high and flat gain is due to the use of inductive gain-peaking technique in addition to the control of the unity gain current cut-off frequencies of LNA2. Figure 7 shows that the proposed LNA2 employing the symmetric 3D RF integrated inductor achieves a gain of 11 ± 1.0 dB.

The proposed UWB LNA2 has an enhanced LNA noise performance. LNA2 NF ranges from 2.5 dB to 3.3 dB over the operating bandwidth (2.5–16 GHz). This NF reduction is accomplished due to the optimization of the LNA noise factor given by (4) and the use of weak shunt capacitive-resistive feedback implemented over the input stage. LNA2 achieves a NF less than 3.3 dB over the operating band of frequency as shown in Figure 8.

3.2. Input and Output Impedance Matching. LNA1 input and output ports have good matching conditions to its source and load, respectively. Simulation results of input and output reflection coefficients of LNA1 are shown in Figure 9. LNA1 has S_{11} and S_{22} less than -11 dB and -10 dB, respectively, over the UWB range of frequencies.

The proposed UWB LNA2 achieves good input impedance matching as shown in Figure 10. Good impedance

TABLE 1: Proposed UWB LNA performance summary in comparison to recently published UWB LNAs.

Reference	BW (GHz)	Gain (dB)	NF (dB)	S_{11} (dB)	S_{22} (dB)
This work (LNA2)*	2.5~16	11 ± 1.0	<3.3	<-7	<-7.25
This work (LNA1)*	3.1~10.6	17 ± 1.5	<2.3	<-11	<-10
LNA-1 [1]	1.7~5.9	11.2 ± 2.3	<4.7	<-11.8	<-12.7
LNA-2 [1]	1.5~11.7	12.2 ± 0.6	<4.8	<-8.6	<-10
[2]	3~10.6	15	<4.4	<-7	NA
[12]	3.1~10.6	10.8 ± 1.7	<6	<-10	<-9.3
[13]	1~5	12.7 ± 0.2	<3.5	<-8	NA

* Post-layout simulation results.

match between LNA2 and its source is obtained using the series-resonant input matching technique. The input return loss (S_{11}) is less than -7.0 dB over this wide range of frequency (2.5–16 GHz).

Figure 11 shows that better output impedance matching is obtained using the planar integrated inductor while simulating LNA2. Good output impedance matching of LNA2 over its operating band of frequency (2.5–16 GHz) is accomplished due to the optimization of the CG output matching stage with the aid of the output LC resonant circuit. R_{out} termination is used to widen the matching bandwidth. The output return loss (S_{22}) shown in Figure 11 is less than -7.25 dB for LNA2 using the planar inductor while it is less than -6.0 dB for LNA2 employing the proposed 3D inductor over the desired frequency band (2.5–16 GHz).

3.3. DC Power, Reverse Isolation, and Stability. LNA1 and LNA2 consume DC power of 12.8 mW and 20 mW, respectively, from a 1.8 V power source. The increased DC consumption of LNA2 is due to having enough driving bias for the CG output match stage.

Both of the proposed UWB LNA1 and LNA2 have a reverse isolation factor (S_{12}) less than -28 dB over each design bandwidth. The proposed UWB LNAs (LNA1 and LNA2) are unconditionally stable over their bandwidths.

Table 1 shows a summary of the proposed UWB LNAs performance in comparison to other recently published UWB LNAs implemented in 0.18 μ m CMOS technology.

4. Conclusion

In this paper, two different UWB LNAs were presented. LNA1 has high gain, minimized noise figure, and good impedance match over the UWB range of frequencies. LNA2 has a wide range of operating frequency (2.5 GHz–16 GHz). UWB LNA2 consists of a current reuse cascaded amplifier with shunt resistive feedback followed by a CG output stage with resistive termination. LNA2 input stage use series-resonant impedance matching technique and employs a symmetric 3D RF integrated inductor as a load. The post-layout simulation results of LNA1 and LNA2 demonstrate the performance improvement achieved through these designs. The next step

is to implement these UWB LNAs to have a comparison between post-layout simulation results and measured results.

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Review Article

Performance and Trends in Millimetre-Wave CMOS Oscillators for Emerging Wireless Applications

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This paper reports the latest advances on millimeter-wave CMOS voltage-controlled oscillators (VCOs). Current state-of-the-art implementations are reviewed, and their performances are compared in terms of phase noise and figure of merit. Low power and low phase noise LC-VCO and ring oscillator designs are analyzed and discussed. Design and performance trends over the last decade are provided and discussed. The paper shows how for the higher range of millimeter-waves (>60 GHz) the performances of ring oscillators become comparable with those of LC-VCOs.

1. Introduction

In the last few years several standards have been, or have been planned to soon be, released, regarding millimetre-waves (mm-waves, i.e., 30–300 GHz) systems for emerging wireless applications. Some of the most attractive applications are 60 GHz unlicensed wireless data communication [1], 77-GHz automotive radars [2], and 94 GHz passive imaging [3]. Key enabler for high-volume and low-cost mass market implementation of these systems is the significant improvement of device performance in the latest CMOS technology nodes (i.e., 130 nm and smaller), which offer a great potential for the realization of millimeter-waves wireless transceivers on a single chip.

One of the most important building blocks in a wireless transceiver is the frequency synthesizer. Performance of the voltage controlled oscillator (VCO) dictates the performance of the frequency synthesizer and thus of the whole communication system.

The aim of the present paper is to provide a review of the state-of-the-art (SoA) of millimeter-wave (mm-wave, 30–300 GHz) VCOs in CMOS technology in order to identify the trends over the last decade and derive some useful observations regarding the past and possible future evolution of design and performance. In particular, the paper reports

a comparison of performances among SoA design solutions and highlights the achievements and trends in terms of phase noise (PN) and figure of merit (FOM).

The present paper is organized as follows. Section 2 provides an overview of two of the most widespread VCO topologies, LC-tank, and ring oscillators and recalls briefly their main causes responsible for the phase noise. In Section 3, SoA millimeter-wave CMOS LC-VCO and ring oscillator design solutions are reported, and their performances are discussed and compared. In Section 4, the conclusions are drawn.

2. CMOS VCOs

The most widespread CMOS VCO topologies at mm-wave frequencies are LC-tank and ring oscillators. Section 2.1 provides a brief overview of LC-VCOs and their PN contributions. Section 3.1 provides a brief review of ring oscillators and their PN contributions.

2.1. LC-Tank VCOs. LC-VCOs consist of a resonant circuit (LC-tank) and an amplifier that provides adequate gain to compensate the losses of the resonant circuit. The amplifier can be a single transistor in one of the known configurations (common-source, common-gate, or source follower) or the widespread cross-coupled differential pair (see Figure 1(a)).

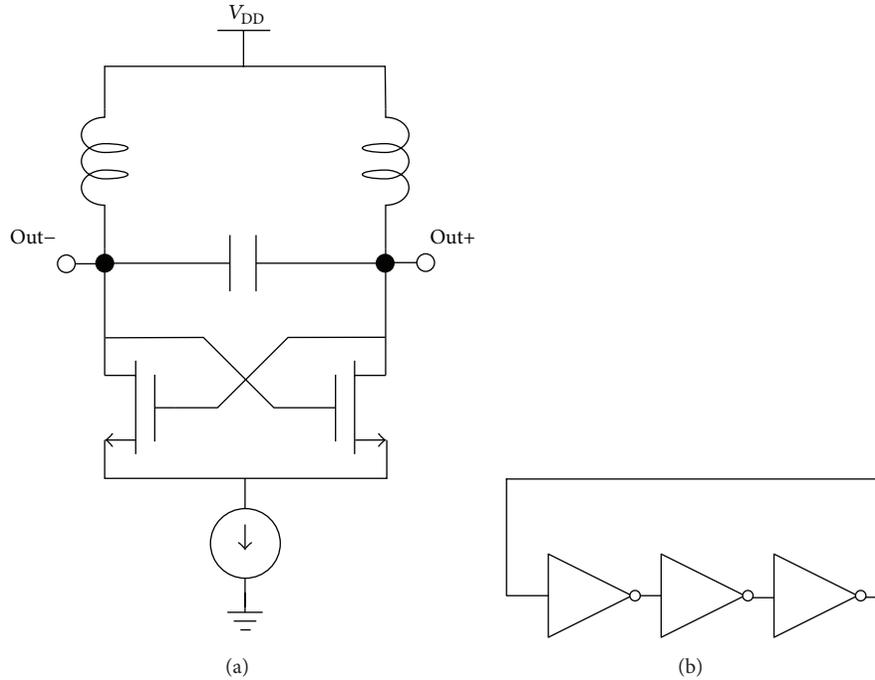


FIGURE 1: (a) LC-VCO; (b) ring oscillator.

The main causes of PN in LC-VCO are due to the losses in the resonator and the amplifier noise. For instance, in the case of cross-coupled differential pair LC-VCOs, they are (i) resonator thermal noise (due to the loss conductance in the resonator), (ii) tail current noise (the switching action of the differential pair translates noise up and down in frequency, and so the noise enters the resonator), and (iii) differential pair noise (due to the finite switching time of the pair) [4].

2.2. Ring Oscillators. Ring oscillators (ROs) are composed of a cascade of inverting amplifiers, and the output of the last element is fed back to the input of the first (see Figure 1(b)). These inverter stages can be implemented by differential amplifiers, CMOS inverters, or even LC-VCOs.

The main causes of PN in ring oscillators are (i) the thermal noise (due to MOSFET drain-source channel resistance and load resistors) and (ii) flicker noise (in CMOS inverter-based ROs, the pull-up and pull-down currents contain flicker noise which varies slowly over many transitions, while, in differential ROs, the flicker noise in the tail current modulates the propagation delay of the stages) [5].

3. State-of-the-Art of mm-Wave CMOS VCOs

In this Section, a review of SoA mm-wave CMOS LC-VCO and RO design solutions is provided, and their performances are discussed and compared. In Section 3.1, three SoA mm-waves CMOS LC-VCO implementations, operating at 30, 60, and 140 GHz, respectively, are reported. In Section 3.2, two SoA mm-wave RO designs (the first implemented at 50 and 60 GHz, the second at 104 and 121 GHz) are reported. In Section 3.3, performance trends over the last decade of

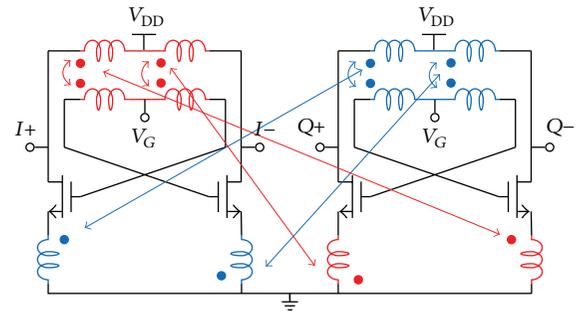


FIGURE 2: Schematic of the VCO presented in [6]. The two trifilar transformers of I and Q VCOs are highlighted in red and blue. Spirals couplings are represented by the thin arrowed lines. I and Q are VCO outputs.

mm-wave CMOS LC-VCOs and ROs are provided and discussed. The performances of the SoA VCOs are summarized in Tables 1 and 2, and their figure of merit (FOM) see (1) are evaluated:

$$\text{FOM} = PN - 20\text{Log}\left(\frac{f_0}{\Delta f}\right) + 10\text{Log}\left(\frac{P_{\text{DC}}}{1 \text{ mW}}\right), \quad (1)$$

where f_0 is the oscillation frequency, Δf is the offset at which the PN is evaluated, and P_C is the power consumption.

3.1. SoA mm-Wave CMOS LC-VCOs. In [6] a 30 GHz quadrature VCO (QVCO) implemented in 0.13 μm CMOS technology is presented. The circuit schematic is shown in Figure 2. It exploits the use of a trifilar (1:1:1) transformer with a high quality factor (i.e., with respect to spiral inductors)

TABLE 1: SoA mm-wave CMOS LC-VCOs: summary of performance.

Reference	Tech. (nm)	f_0 (GHz)	V_{DD} (V)	P_C (mW)	Phase noise (dBc/Hz)	FOM (dBc/Hz)
[6]	130	30.3	0.6	7.8	-114 @ 1 MHz	-196
[7]	90	57.6	0.6	7.2	-102 @ 1 MHz	-188
[9]	90	139.8	1.2	9.6	-75 @ 1 MHz	-178

TABLE 2: SoA mm-wave CMOS ROs: summary of performance.

Reference	Tech. (nm)	f_0 (GHz)	V_{DD} (V)	P_C (mW)	Phase noise (dBc/Hz)	FOM (dBc/Hz)
[10]	130	50.3	0.8	35	-104 @ 1 MHz	-186.4
[10]	130	58.5	0.8	34	-95 @ 1 MHz	-180.6
[11]	130	104	1.5	28	-93.3 @ 1 MHz	-180
[11]	130	121	1.3	21	-88 @ 1 MHz	-176.5

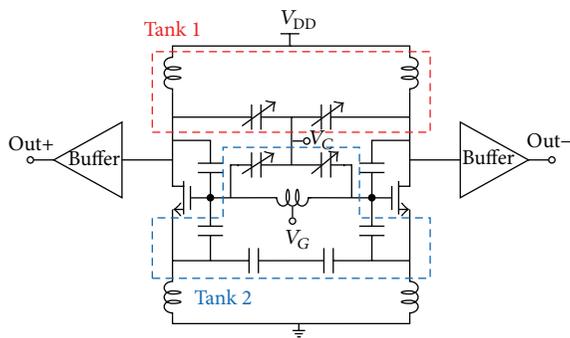


FIGURE 3: Schematic of the 60 GHz Colpitts LC-VCO presented in [7].

in order to improve the PN performance. In fact, with respect to inductors, transformers can provide higher quality factors due to the mutual coupling between the spirals. The trifilar transformer couples two series cascaded cross-coupled VCO structures. The transformer couples in-phase and in-quadrature drain and source spirals, allowing for a reduction of device noise, parasitic capacitances, and power consumption. The PN is -114 dBc/Hz @ 1 MHz from the carrier frequency of 30.3 GHz. The power consumption amounts to 7.8 mW from a 0.6 V supply voltage.

In [7], a 60 GHz Colpitts LC-VCO implemented in 90 nm CMOS technology is presented. The circuit schematic is shown in Figure 3. Although Colpitts oscillators have good PN performances, they suffer from the Miller capacitance effects, which cause an increase in the parasitic gate-drain capacitance of the MOSFET transistors. This issue is solved by combining a conventional Colpitts oscillator and a tuned-input tuned-output (TITO) oscillator [8]. In this way, start-up issues of the Colpitts oscillator have been solved, and phase noise performance improved (thanks to an extra LC-tank for noise filtering). The circuit consumes 7.2 mW from a 0.6 V supply voltage. The PN is -102 dBc/Hz @ 1 MHz offset from the carrier (57.6 GHz). The tuning range is 5.3 GHz (from 55.8 to 61.1 GHz).

In [9] a 140 GHz cross-coupled LC-VCO implemented in 90 nm CMOS technology by UMC is presented. The

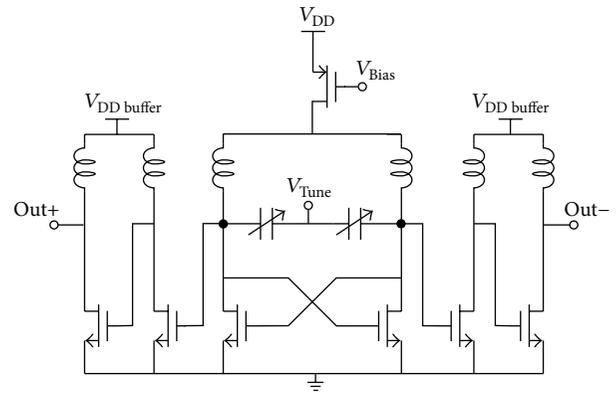


FIGURE 4: Schematic of the 140-GHz LC-VCO presented in [9].

circuit schematic is shown in Figure 4. A low parasitic cross-coupled transistor layout is developed in order to achieve a high fundamental frequency. The VCO core has been biased through a p-MOSFET in order to reduce the flicker noise contribution to the overall close-in PN. Moreover, to minimize the load capacitance connected to the LC-tank, a two-stage tapered buffer has been used to drive the 50 Ω load. The VCO core consumes 9.6 mW from a 1.2 V voltage supply. The buffers consume 7.2 mW. The PN amounts to -75 dBc/Hz @ 1 MHz offset from the carrier frequency of 139.8 GHz.

Table 1 summarizes the main characteristics and performances of the aforementioned LC-VCOs.

3.2. SoA mm-Wave CMOS Ring Oscillators. In [10], 50 GHz and 60 GHz ring oscillators implemented in 0.13 μ m CMOS are presented. The block diagram is shown in Figure 5(a). An interpolative-phase-tuning (IPT) technique is used to tune frequency of multiphase mm-wave LC-based ROs without using varactors (see Figure 5(b)). In order to vary the output frequency, the delay of each stage of the ROs is varied by means of tunable phase shifters. A fixed phase shift is used to introduce a delayed current i_1 via M_3 and M_4 ; i_1 is interpolated with the undelayed current provided by M_1 and M_2 . The phase shift can be tuned from 0 to β by controlling the biasing dc current I_0 and I_1 . Two output

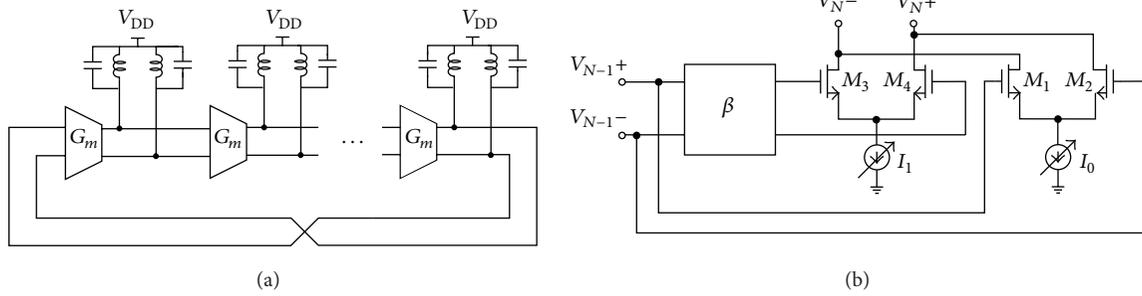


FIGURE 5: (a) Block diagram of the 50 and 60 GHz ring oscillators presented in [10]. (b) Schematic of G_m block of Figure 4(a): β is a fixed phase shifter implemented by a LC-based differential stage.

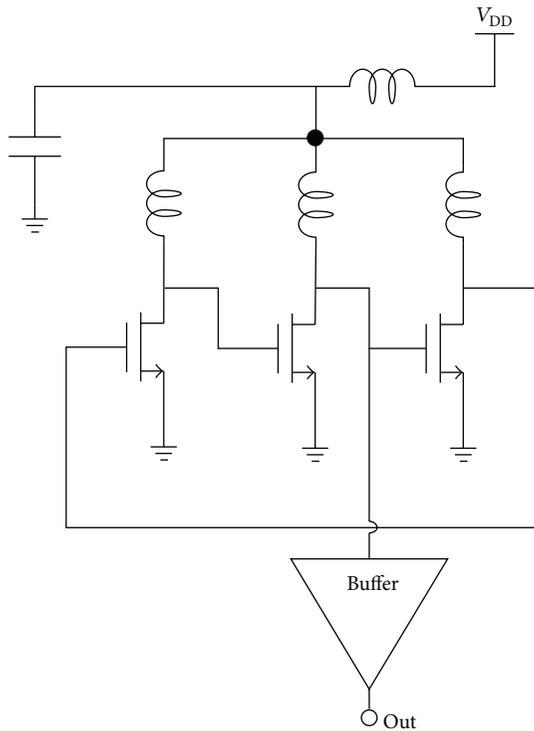


FIGURE 6: Schematic of the 104 and 121 GHz ring oscillators presented in [11].

current-controlled oscillators (CCOs), with 4 and 8 phases, are implemented using this technique. The 8-phase CCO can be tuned from 48.6 to 52 GHz, and it consumes from 32 to 48 mW from a 0.8 V voltage supply. The 4-phase CCO can be tuned from 56 to 61.3 GHz and consumes from 30 to 37 mW. The PN of the 8-phase CCO amounts to -104 dBc/Hz at 1 MHz offset from the carrier (50.3). The PN of the 4-phase CCO is -95 dBc/Hz @ 1 MHz offset from the carrier (58.5 GHz).

In [11] two fundamental three-stage ROs implemented in a $0.13 \mu\text{m}$ CMOS process and oscillating at 104 GHz and 121 GHz, respectively, are presented. The circuit schematic is shown in Figure 6. A new design methodology for designing high-frequency oscillators has been developed. This method finds the best topology to achieve frequencies close to the

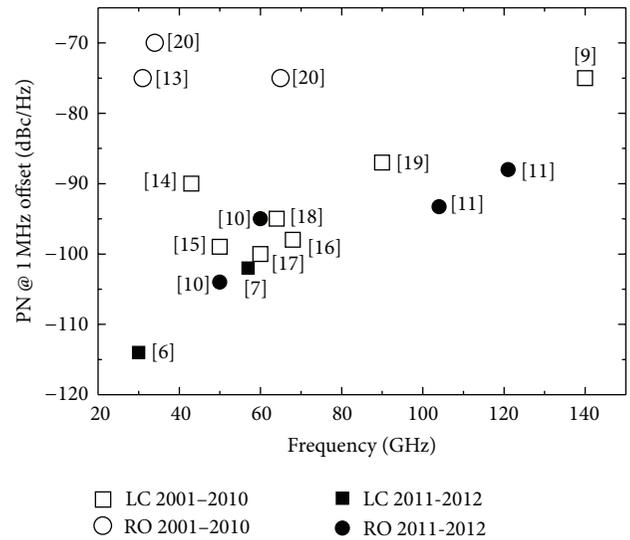


FIGURE 7: Oscillator phase noise performances versus oscillation frequency [6, 7, 9–11, 13–20].

maximum frequency of oscillation of the transistors. It is based on the activity condition of the transistors. A device is called active at a certain frequency, if it can generate power in the form of a single sinusoidal signal at that frequency [12]. This method determines also the maximum frequency of oscillation for a fixed circuit topology. Each stage of the implemented ROs is implemented using a double gate transistor with a substrate contact ring around the transistor and an inductive load. The measured peak output powers of the two oscillators are -3.5 dBm and -2.7 dBm at 121 GHz and 104 GHz, respectively. The DC power consumptions, including the output buffer, is 21 mW from a 1.28 V supply and 28 mW from a 1.48 V supply for the 121 GHz and 104 GHz oscillators, respectively. The PN at 1 MHz offset frequency is -88 dBc/Hz and -93.3 dBc/Hz for the 121 GHz and 104 GHz oscillators, respectively.

The main figures of merit and performances of the aforementioned ring oscillators are presented in Table 2.

3.3. *Performance Trends in mm-Wave CMOS VCOs.* PN versus oscillation frequency of SoA mm-wave CMOS LC-VCOs and ROs published in the last 11 years are shown in

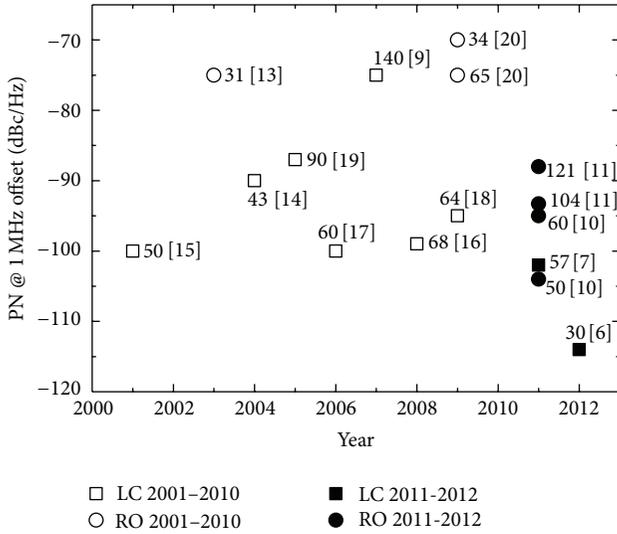


FIGURE 8: Oscillator phase noise performances versus publication year [6, 7, 9–11, 13–20].

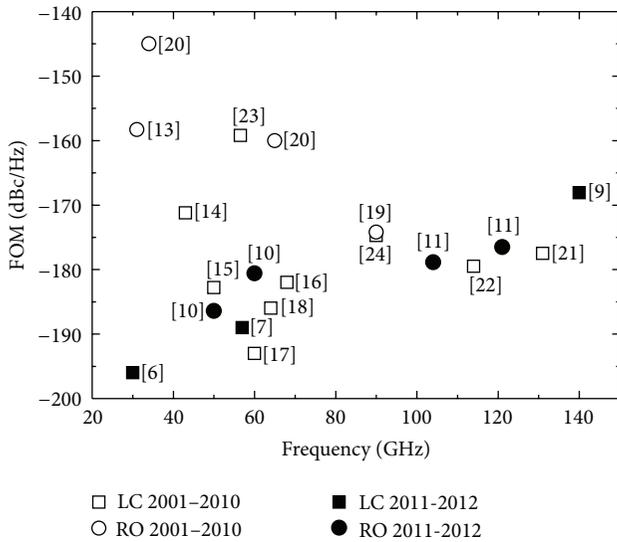


FIGURE 9: Oscillator FOM versus oscillation frequency [6, 7, 9–11, 13–24].

Figure 7. It can be observed that PN performances of ring oscillators are becoming closer to those of LC-VCOs while moving towards very high frequencies.

Figure 8 shows PN versus publication year. It can be noted that in the last couple of years, while in the low mm-wave range (30 GHz) the PN of LC-VCOs is still better (-114 dBc/Hz @ 1 MHz offset from 30 GHz [6]), at very high frequencies PN of RO becomes comparable to that of LC-VCOs, achieving a PN of -88 dBc/Hz @ 1 MHz at 121 GHz [11].

The FOM achieved by the state-of-the-art mm-wave CMOS LC-VCOs and ROs published in the last 11 years are shown in Figure 9. Also in this case, as in Figure 7 relative to PN, it can be noted that in the lower part of the mm-wave range (below 60 GHz) LC-VCOs attain overall better FOM

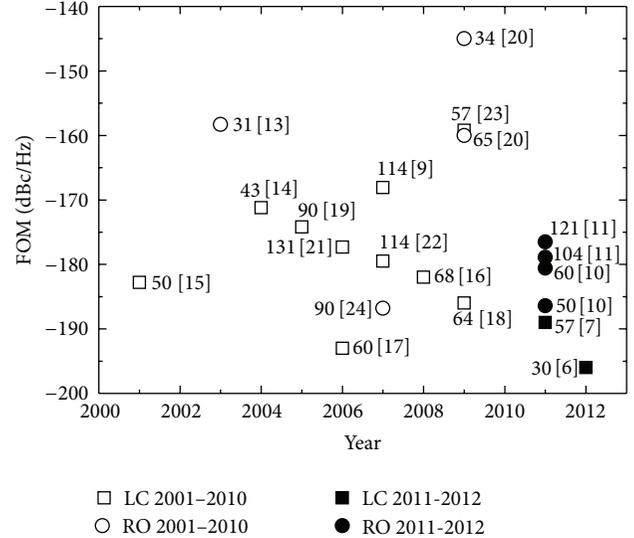


FIGURE 10: Oscillator FOM versus publication year [6, 7, 9–11, 13–24].

than ROs, but for very high frequencies FOM of ROs became comparable to that of LC-VCOs.

Figure 10 shows FOM versus publication year. It can be noted that the trend in the last couple of years is that the FOM of LC-VCOs is still superior, but it is achieved for lower frequencies [6, 7] than the ROs in [10, 11]. In fact, the solutions in [10, 11] achieve FOM comparable to those of previous implementations of LC-VCOs at lower frequencies.

4. Conclusions

A review of the state-of-the-art of millimeter-wave CMOS VCOs has been presented. State-of-the-art LC-VCOs and ring oscillators have been presented and discussed, and their performances have been compared. The trends for VCO design and performance over the last decade have been traced and discussed.

From these evaluations it appears that while moving in the higher part of the mm-wave spectrum (>60 GHz) phase noise and FOM performance of ring oscillators tend to become closer, and even comparable, to those of LC-VCOs, which are dominant at lower frequencies. Thus, ring oscillators appear to be a strong candidate for the implementation of CMOS VCOs operating at the higher region of the mm-wave frequency spectrum.

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Research Article

A Novel Reconfigurable MB-OFDM UWB LNA Using Programmable Current Reuse

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This paper presents a design of a reconfigurable low noise amplifier (LNA) for multiband orthogonal frequency division multiplexing (MB-OFDM) ultra wideband (UWB) receivers. The proposed design is divided into three stages; the first one is a common gate (CG) topology to provide the input matching over a wideband. The second stage is a programmable circuit to control the mode of operation. The third stage is a current reuse topology to improve the gain, flatness and consume lower power. The proposed LNA is designed using $0.18\ \mu\text{m}$ CMOS technology. This LNA has been designed to operate in two subbands of MB-OFDM UWB, UWB mode-1 and mode-3, as a single or concurrent mode. The simulation results exhibit the power gain up to 17.35, 18, and 11 dB for mode-1, mode-3, and concurrent mode, respectively. The NF is 3.5, 3.9, and 6.5 and the input return loss is better than -12 , -13.57 , and -11 dB over mode-1, mode-3, and concurrent mode, respectively. This design consumes 4 mW supplied from 1.2 V.

1. Introduction

Ultra wideband (UWB) has many advantages over narrowband technology such as high data rate, low power, low complexity, and low cost technology. When The US Federal Communication Commission (FCC) recognized the potential advantages of UWB, it issued a report that allows UWB use for commercial communication systems in 2002, and its applications can operate in the unlicensed spectrum of 3.1–10.6 GHz [1]. UWB supports carrierless baseband signals such as impulse-radio IR-UWB, and it supports wideband with carrier such as multiband orthogonal frequency division multiplexing MB-OFDM UWB [2]. In MB-OFDM UWB systems, the spectrum from 3.1 to 10.6 GHz is divided into 14 subbands of 528 MHz as shown in Figure 1, which supports data rates from 53 to 480 Mbps [3, 4].

In order to roam across different subbands, devices that support multinet applications are required. There is a strong motivation on using single chip supports multiband and multiapplications, due to it provides wireless access for users anywhere and anytime. In such reconfigurable devices, the design of low noise amplifier (LNA) is a critical issue

because its has effects in the overall system and requirements as high gain, low noise figure (NF), and lower power consumption, with good input and output matching over each band of interest.

Recently, there are some schemes proposed to the multistandard LNAs like parallel, concurrent, wideband, and reconfigurable LNA. The first approach is the parallel architecture that employs multiple architectures for each band of interest [5]. However, this approach requires large area, different design for each band, and more time. The concurrent and wideband approaches provide multiband simultaneously [6] by providing the input matching, but this approaches pass the large interference the matching network; therefore, increasing the linearity is required [7, 8]. Recently, the reconfigurable approach presents to discrete band and/or concurrent bands [7] to solve the tradeoff between area, power, and cost. Many approaches present a continuous tuning like [8, 9]; it is good for narrowband applications, but it is not applicable for widebands.

This paper proposed a new reconfigurable MB-OFDM LNA for UWB systems. The proposed LNA reconfigured over dual widebands and it works as a discrete band or concurrent

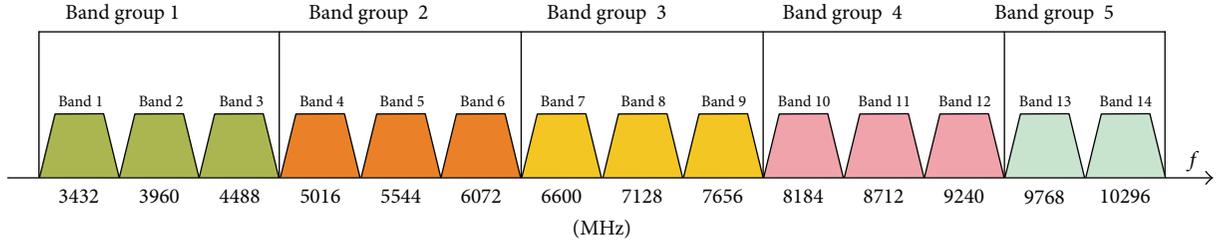


FIGURE 1: Frequency spectrum of MB-OFDM UWB system.

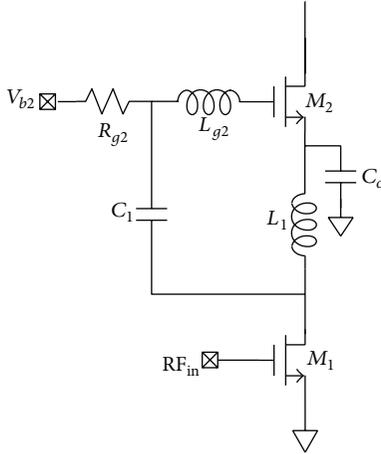


FIGURE 2: Current reuse architecture.

based on the programmable part. This design based on CG topology to provide the input matching over wideband [10, 11], current reuse technique shown in Figure 2 used to provide high and flat gain, and low power consumption [12–14], and programmable circuit to select the band of operation. This paper is organized as follows, the demonstration of the proposed circuit, defect and solution of current reuse technique will be presented in Section 2. Section 3 discusses the simulation results of the proposed LNA. Finally, the conclusion is presented in Section 4.

2. Circuit Design of the Proposed Reconfigurable MB-OFDM UWB LNA

The proposed LNA was designed by a standard $0.18\ \mu\text{m}$ CMOS process. Figure 3(a) shows the schematic of the LNA. This circuit consists of three stages distinguished by three different blocks in Figure 3(a). The first one, input matching stage in block-1 in Figure 3(a), the CG topology used to control the input matching over wideband [11, 15] where the input impedance at L_S resonated with the gate-to-source parasitic capacitance of C_{gs1} of M_1 is $Z_{in} = 1/g_{m1}$, where g_{m1} is the transconductance of transistor M_1 . Therefore, the matching bandwidth can be calculated by

$$f_{BW} = \frac{1}{2\pi C_{gs1} (1/g_{m1})} = \frac{g_{m1}}{2\pi C_{gs1}} \quad (1)$$

TABLE 1: Look-up table of programmable circuit.

M_{S1}	M_{S2}	BW (GHz)	f_0 (GHz)	Mode
0	0	—	—	—
0	1	0.528	3.432	Single
1	0	0.528	4.488	Single
1	1	≈ 1.4	3.96	Concurrent

hence, by controlling g_{m1} the input impedance can be matched to $50\ \Omega$ at resonance.

Second stage is the programmable switches in block-2 in Figure 3(a), actually this stage is proposed to achieve two main tasks. The first task is used to select the branch that will provide the desired band, consequently, the selected band depends on Table 1, where f_0 is the center frequency of the selected mode. The other task is used to solve current reuse defect, without using this stage the control of this circuit can be made by transistor M_{2a} and M_{2b} , but when one of them is OFF, n_1 and n_2 nodes will be shorted, thereby the overall circuit performance will be effected.

To solve this problem the programmable circuit is proposed, when transistor M_{S2} is OFF as shown in Figure 3(b) n_1 and n_2 nodes will be disconnected.

Finally, the current reuse stage in block-3 in Figure 3(a), is used to achieve high and flat gain, and lower power consumption. This architecture was simplified in Figure 2 and it consists of series inductor L_1 and shunt capacitor C_1 connected to DC cascode transistors M_1 and M_2 . C_1 is used to resonate with gate-to-source parasitic capacitance of M_2 , C_{gs2} , while L_1 is selected large in the desired bandwidth to provide high impedance path to block RF signal. Furthermore, when the capacitance C_o is selected large, the transistors M_1 and M_2 act as two common source (CS) cascaded stage at high frequency [12–14].

3. Simulation Results

Design of the proposed reconfigurable MB-OFDM UWB LNA was carried out using Spectre simulator from Cadence Design Suite. The proposed circuit consumes 3.32 mA from 1.2 V supply when it works in single mode, but when it works in concurrent mode it consumes 3.39 mA. The simulation results for S-parameters and NF are illustrated in Figure 4 and Figure 5.

Figure 4(a) shows the simulated input return loss S_{11} for different frequency bands based on Table 1. As noticed,

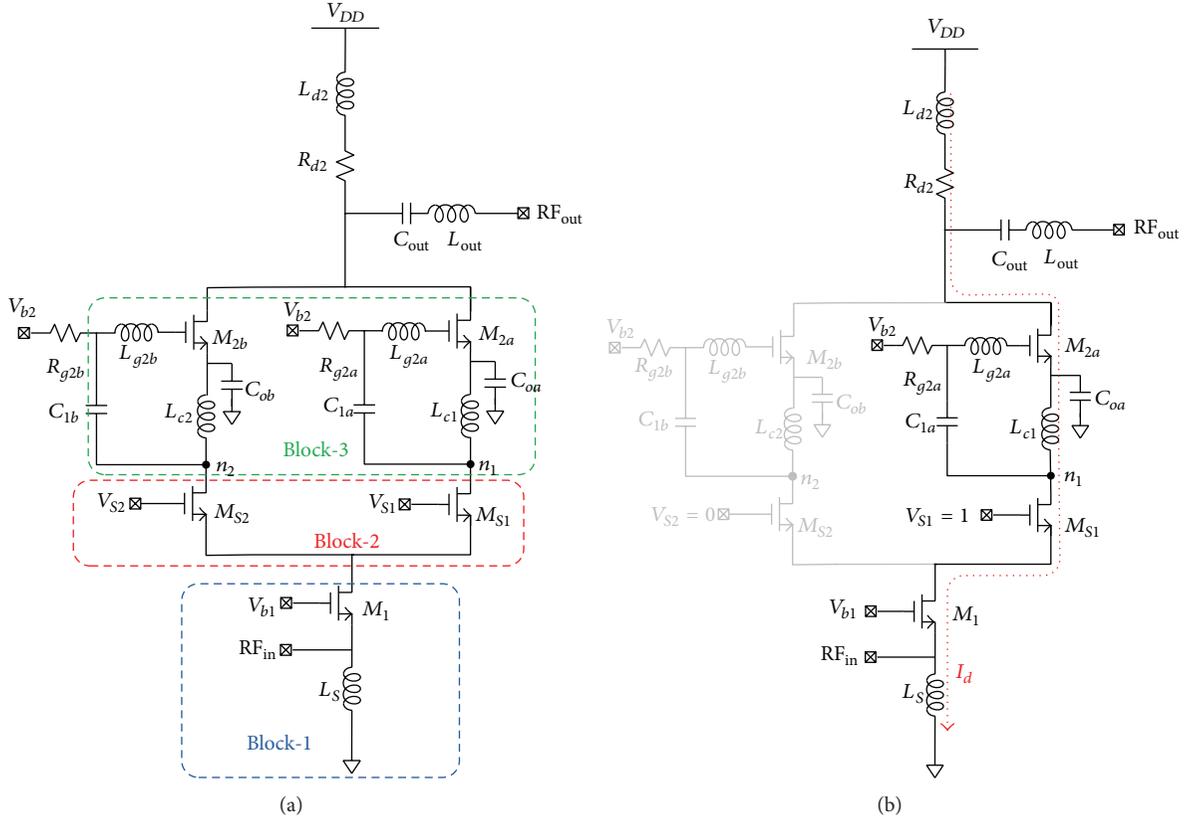


FIGURE 3: Circuit design of the proposed reconfigurable MB-OFDM UWB LNA: (a) schematic of proposed reconfigurable MB-OFDM UWB LNA and (b) operation of the proposed LNA when M_{S1} ON and M_{S2} OFF.

S_{11} is less than -12 , -13.57 , and -11 dB for UWB mode-1 with center frequency 3.432 GHz, UWB mode-3 with center frequency 4.488 GHz, and concurrent mode with center frequency 3.96 GHz, respectively. These results depict the input matching network of the proposed LNA under -10 dB, the reason behind this due to CG topology and selection of appropriate value of L_s to resonate with C_{gs1} , so the proposed design has a good input matching.

Figure 4(b) presents the reverse isolation S_{12} between output and input ports over bands of interest, where it is less than -50.5 , -44.2 , and -52 dB for mode-1, mode-3, and concurrent mode, respectively. Also the better isolation comes from CG topology, where the input is isolated from the output of this topology.

Figure 4(c) illustrates the voltage gain S_{21} of the proposed LNA. As depicted, the proposed LNA achieves 17.35, 18, and 11 dB for mode-1, mode-3, and concurrent mode, respectively. The high gain of this LNA is due to current reuse, where the overall transconductance of this design is $g_m = g_{m1}g_{m2}$. However, the gain of concurrent mode is lower than single mode, due to the parallel resistance of branches (output resistance of M_{2a} , r_{o2a} series with output resistance of M_{S1} , and r_{oS1} are parallel with output resistance of M_{2b} , r_{o2b} series with output resistance of M_{S2} , and r_{oS2}). Figure 4(d) shows the output return loss S_{22} of the reconfigurable LNA where it is under -14.9 , -9.6 , and -14.2 dB for all modes.

The good output matching was achieved due to the selection of appropriate values for output matching network (M_2 , L_{g2} , L_{d2} , L_{out} , C_{out} , and C_o). The simulated NF versus bands of interest is shown in Figure 5. As noticed, NF of the proposed LNA achieves 3.49–3.53, 3.9–3.93, and 6.29–6.8 dB for mode-1, mode-3, and concurrent mode, respectively. The high NF of concurrent mode is due to the number of transistors that are used in this mode.

The performance of the proposed LNA and a comparison with existing architectures are summarized in Table 2. As shown in this table, the proposed LNA provides discrete tuning and concurrent, while the existing techniques either provide discrete, concurrent, or continuous tuning. The voltage gain S_{21} for the proposed architecture is lower than [8, 9, 16], because they use the cascode and cascade topologies for that they consume higher power when compared with the proposed reconfigurable LNA.

4. Conclusion

A reconfigurable LNA for MB-OFDM UWB receivers is proposed. This LNA works in three modes of operation based on programmable current reuse technique. The detailed operation of the proposed reconfigurable LNA including input matching topology (CG), programmable switches circuit, high gain and low power technique (current reuse),

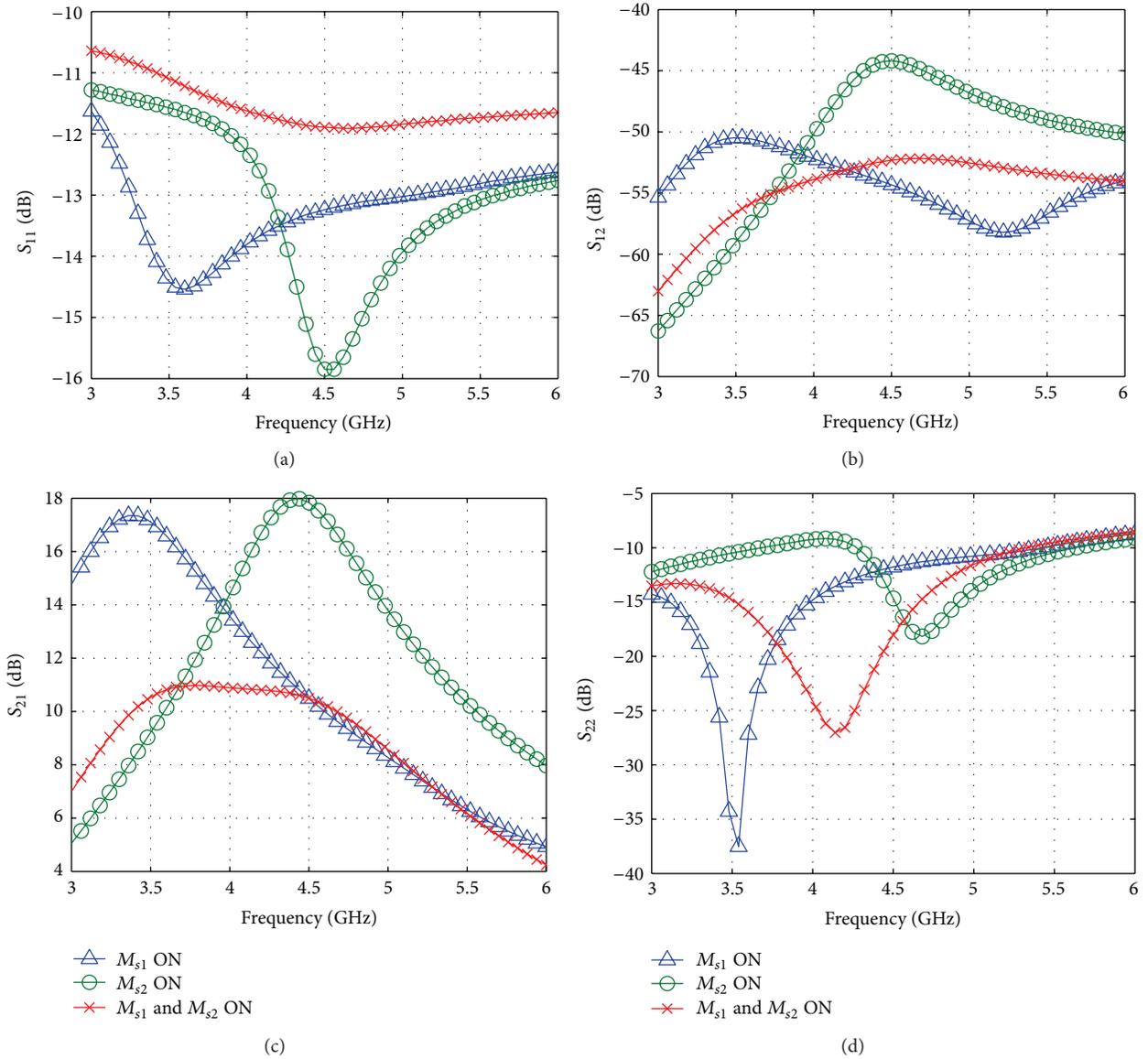


FIGURE 4: S-Parameter results of reconfigurable LNA over multibands: (a) input reflection coefficient S_{11} , (b) reverse isolation S_{12} , (c) voltage gain S_{21} , and (d) output reflection coefficient S_{22} .

TABLE 2: The performance of the proposed LNA and comparison with existing architecture.

	Tech. CMOS	BW (GHz)	V_{dd} (V)	S_{11} (dB)	S_{22} (dB)	S_{21} (dB)	NF (dB)	Power (mW)	Topology
[7]	0.13	2.8, 3.3, 4.6	1.2	< -18	—	14.2–16	1.7–3.7	6.4	S*
		2.05, 5.65		< -8.6	—	14.9	4–4.8		C**
		4.3–10.8		—	—	3–15.6	4–5.3		UWB
[8]	0.13	1.9–2.4	1.2	< -13	—	14–10	3.2–3.7	17	Con***
[9]	0.13	3.4–3.6	1.2	< -18	< -15.3	20.9–21.3	< 1.8	16	S
		4.2–4.8	1.2	< -15	< -14.5	19.2–20.7	< 2.3		
[15]	0.18	0.9, 1.5, 2.4	1.8	< -10	—	15–19	1.9–4.5	30	C
[16]	0.13	1.8–2.4	1.2	< -12	—	26–28	3.2–3.4	9.6	
This work	0.18	3.168–3.696	1.2	< -12.04	< -14.9	15.8–17.35	3.49–3.53	4	S
		4.224–4.752		< -13.57	< -9.6	16–18	3.9–3.93		S
		3.432–4.488		< -11	< -14.2	10.25–11	6.28–6.8		C

*S: Single mode; **C: Concurrent mode; ***Con: continuous.

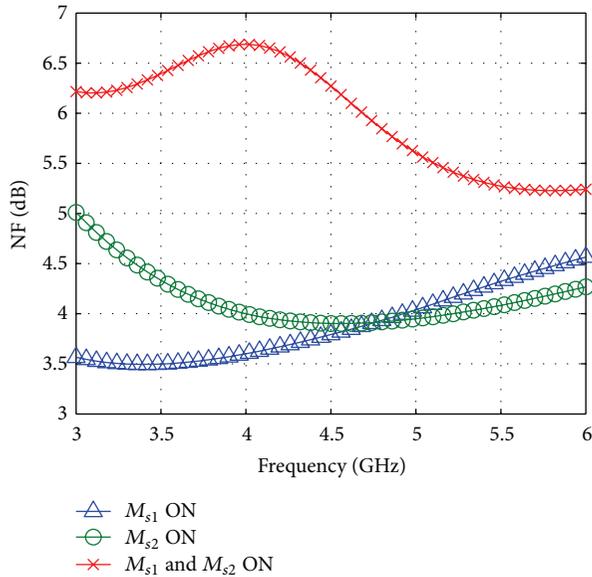


FIGURE 5: Noise figure NF.

and the noise performance of this circuit was presented. The proposed LNA operates by 1.2 V supply and consumes 3.32 mA for single mode (UWB mode-1 or mode-3) and 3.39 mA for concurrent mode. Finally, it has been designed by 0.18 μm CMOS process.

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Research Article

Systematic Design Methodology of a Wideband Multibit Continuous-Time Delta-Sigma Modulator

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Systematic design of a low power, wideband and multi-bit continuous-time delta-sigma modulator (CTDSM) is presented. The design methodology is illustrated with a 640 MS/s, 20 MHz signal bandwidth 4th order 2-bit CTDMS implemented in 0.18 μm CMOS technology. The implemented design achieves a peak SNDR of 65.7 dB and a high dynamic range of 70 dB while consuming only 19.7 mW from 1.8 V supply. The design achieves a FoM of 0.31 pJ/conv. Direct path compensation is employed for one clock excess loop delay compensation. In the feedforward topology, capacitive summation using the last opamp eliminates extra summation opamp.

1. Introduction

Delta-sigma modulators embed low-resolution analog-to-digital converter in a feedback loop. The use of feedback and high oversampling pushes the quantization noise out of the band of interest and thereby provides a high in-band resolution. Delta-sigma modulator is well suitable for a high-resolution data conversion because a moderate accuracy of passive components is required. Recently, continuous-time delta-sigma modulator has brought tremendous attention because of its exceptional features such as inherent antialiasing filter (AAF), relaxed gain-bandwidth requirement on active elements resulting in a low-power consumption compared to its counterpart discrete-time delta-sigma modulator [1, 2]. Low-power consumption is the key for a CTDSM.

In [3], the design methodology for a multibit modulator with two-step quantizer is presented. However, the optimization of the peak SNR and the maximum stable amplitude is not taken into consideration. Also, excess loop delay compensation is for more than one clock, where, to achieve higher resolution, higher bit quantizer should be used. These

all increase the design methodology complexity and are not simple to adopt for designers. To keep the design simple and the insight intact, we implement one-step quantizer with excess loop delay compensation for one clock. In [4], the optimal design methodology of a higher-order continuous-time wideband delta-sigma modulator is presented. However, this methodology requires summation amplifier and hence consumes higher power. In our approach, the summation amplifier is eliminated by using capacitive summation with last integrator's amplifier and this makes design simpler and saves significant power. Also, in [4] SNR and phase margin are optimized which could be replaced to simpler way to optimize the peak SNR and the maximum stable amplitude which are more obvious parameters.

Recent development in wireless communication standard demands a wideband and high-resolution data converters. To achieve a high SNR over a wideband, a higher clock rate, that is, a higher oversampling ratio (OSR), is desired. However, OSR is limited by the clock rate due to technology limitations and power consumption. Fortunately, the SNR

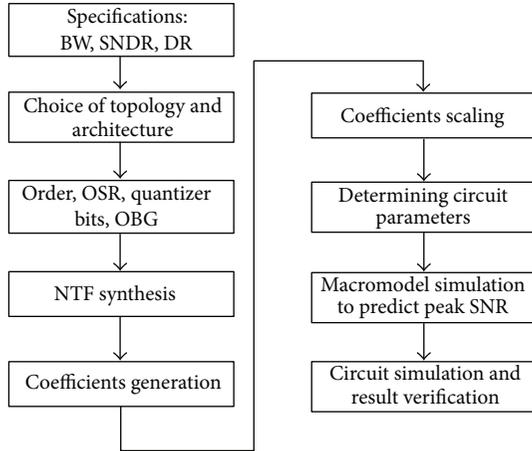


FIGURE 1: Flow chart of the design methodology.

degradation due to lower OSR can be compensated by a multi-bit quantizer.

We present a systematic methodology to design a wide-band and high-resolution modulator at low power cost. To illustrate the methodology, we aim to design a continuous-time delta-sigma modulator which has signal bandwidth of 20 MHz and requires 10-11-bit resolution suitable for WLAN. Section 2 discusses the high-level synthesis. In Section 3, we present simple circuit implementation of the modulator. Section 4 presents the results and discussion and finally Section 5 concludes the paper.

2. High-Level Synthesis

In this section, we describe the design methodology in accordance with the flow chart in Figure 1 to synthesize a high-level wideband multi-bit continuous-time delta-sigma modulator in MATLAB to meet the specification for WLAN.

2.1. Choice of Topology and Architecture. A single-loop topology is preferred to a MASH topology to reduce the circuit complexity. To implement the loop filter, a feedforward (FF) topology is preferred to a feedback (FB). A FF topology has several advantages over a FB topology. Firstly, FF uses only one feedback DAC (without any compensation for excess loop delay (ELD)) in the main loop which results in smaller silicon area and better matching of coefficients. However, in the case of FB, multiple DACs equal to the order of the modulator are needed which increase the chip area and mismatch is a major concern [5]. Secondly, the integrating resistor in both the FF and the FB topologies is determined by the noise and distortion requirement. However, in a FF topology, the second and further resistors can be made larger. In a FF topology the first opamp is the fastest while in a FB topology, the first opamp is the slowest. Thus the capacitor size can be reduced in the second and higher integrators with increased resistor value which significantly reduces the silicon area [6]. Also, the necessity for scaling and also the requirements on integrator dynamics are much more relaxed which results in increase in power efficiency of FF topology

compared to that of FB topology [1]. However, in general FF topology requires extra summation amplifier which could be eliminated by implementing capacitive as shown in Figure 4 and explained in Section 2.3 [7]. Thus a single-loop FF DSM is the most suitable choice for a high dynamic range and a low-power design.

2.2. Noise Transfer Function (NTF) Synthesis. Noise transfer function synthesis is critical for delta-sigma modulator design as it guides the overall performance and the stability of modulator. Before NTF can be synthesized, order of the modulator, oversampling ratio, quantizer's bit and out-of-band gain must be determined.

2.2.1. Oversampling Ratio (OSR). Among all these, oversampling is the most important driving factor as it is directed by the technology node and power consumption. In principle, increasing OSR by 2 times results in a 15 dB improvement in SNR. However, OSR or clock rate is limited by CMOS technology and the power consumption. To design a wide-band modulator with 20 MHz signal bandwidth, an OSR of 16 results in a clock rate (f_s) of 640 MS/s which is high enough to design analog circuits in 0.18 μm CMOS technology. Thus we need to design a comparator which can perform comparison at 640 MS/s and opamp which can have GBW higher than 640 MHz for integration to support sampling at 640 MS/s. Since these are pretty high-performance components, we limit the oversampling ratio to 16.

2.2.2. Modulator's Order. Higher-order modulator improves the SNR; however, it increases the circuit complexity and deteriorates the stability. Since we target a wide-signal band of 20 MHz, a higher-order modulator is essential and therefore we simulate the modulator for third, fourth, and fifth order. From simulation we find that a good choice of the modulator order is 4 for a wide bandwidth (20 MHz) and ideally produces a SNDR of 70 dB which is approximately 8 dB higher than the required 62 dB for 10-bit resolution. This 8 dB margin is kept to counter the loss due to circuit nonidealities. This is why 4th-order modulator is chosen for implementation.

2.2.3. Quantizer's Bit. A multi-bit quantizer has several advantages over a single-bit quantizer [1, 2] and compensates well the SNR limitation due to lower OSR. Firstly, a multibit quantizer reduces in-band quantization noise by 6 dB and allows more aggressive NTF with higher out-of-band gain (OBG) resulting in further significant drop in in-band quantization noise. Secondly, the amplitude of the noise in a multi-bit quantizer is much lower compared to that in a single-bit quantizer. Hence the slew rate requirement on the loop filter opamp is greatly relaxed to allow low-power opamp design. Thirdly, a multi-bit feedback DAC is less sensitive to clock jitter [8]. For low power, reduced circuit complexity, and to keep peak SNR well above 60 dB, a 2-bit quantizer is chosen.

2.2.4. Out-of-Band Gain (OBG). As a rule of thumb, the OBG for a single bit quantizer is 1.5 to ensure the stability

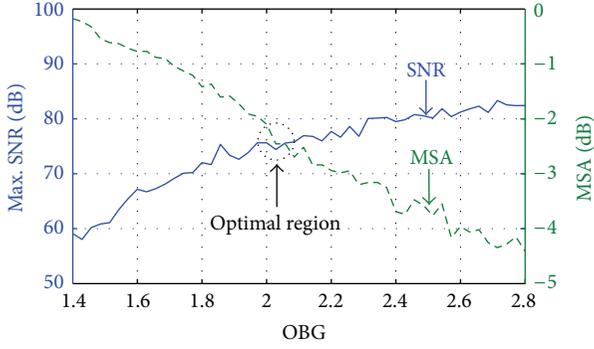


FIGURE 2: SNR and MSA versus the out-of-band gain (OBG) of the NTF for 4th-order 2-bit DSM.

[9]. However, in case of a multi-bit quantizer, the OBG can be increased to reduce the in-band noise and thereby improve the SNR. A 4th-order, 2-bit modulator is extensively simulated for various OBG to determine the maximum SNR and the maximum stable amplitude (MSA). Considering the tradeoff between the SNDR and the maximum stable amplitude (MSA), as depicted in Figure 2, the optimum OBG is chosen to be 2.

Now with all parameters in hand, the NTF is determined using the function *synthesizeNTF* from [10]. A 4th-order, 2-bit modulator with OSR of 16 results in a peak SNDR of 70 dB over a signal bandwidth of 20 MHz.

2.2.5. Excess Loop Delay (ELD) Compensation. The finite regenerative time of a flash converter and the digital logic delay time in the feedback add extra delay, called excess loop delay (ELD), in the loop and effectively increase the order of the modulator. For a modulator of order 2 or above, it needs to be compensated to ensure the stability and maintain a high SNR. One of the efficient methods to compensate ELD is coefficient tuning by adding a direct path between the DAC output and the flash input [1]. Though the compensation time could be any, from the circuit design and operation point of view, it is better to compensate for half a clock or integral multiple of half a clock. To use a single clock, one clock delay compensation is used which helps to relax the requirement on analog building blocks, opamp and comparator.

2.3. Coefficients Generation and RC Parameters. The function *synthesizeNTF* returns discrete-time (DT) coefficients of a modulator which must be translated into continuous-time (CT) coefficients. To reduce the clock jitter sensitivity, NRZ DAC pulse is preferred to other DAC pulse shapes. With NRZ DAC and one clock compensation for excess loop delay, the discrete-time coefficients are converted into the continuous time using the function *realizeNTF_ct* available in [10]. The obtained coefficients result in integrator's output which have much higher swing for modern low supply voltage like 1.8 V and direct implementation would result in large clipping and hence large distortion. Also, the output of one integrator is input to the next integrator and therefore large swing will demand high-input swing for opamp which costs high power.

TABLE 1: Scaled coefficients.

a_0	1.34
a_1	4.25
a_2	4.92
a_3	3.39
a_4	2.76
b_1	0.4
c_1	0.4
c_2	0.4
c_3	0.4
c_4	0.1
g_1	0.11
g_2	0.29

Therefore, the scaling is done to ensure that the output swings of all integrators are well below the maximum allowed voltage (in our case 1.8 V) such that they accommodate the saturation voltage of the output stages of opamps and they do not distort the signals. The resulting coefficients are tabulated in Table 1 for the modulator block diagram in Figure 3.

Figure 4 shows the block diagram of the loop filter. For simplicity, the diagram is shown single-ended; however, the actual circuit implementation is done fully differential. The fourth integrator is used to integrate with R_4C_4 and opamp and the same opamp is used to sum all the feedforward voltages with a_0C_4 , a_1C_4 , a_2C_4 , and a_3C_4 along with C_4 [7]. The coefficients a_1 , a_2 , and a_3 are realized with the capacitive sum while the coefficient a_4 is embedded in the integration with R_4C_4 . This helps to completely eliminate the summation opamp and thereby saves a significant amount of power. Delta-sigma

$$R_1 = \frac{V_{in}^2/2}{32kTf_B * 3 * 2^{2B-1}} \quad (1)$$

modulator is a thermal-noise-limited system and the resistor at the input of an active RC integrator contributes the majority of noise. So in a thermal-noise-limited modulator, the resistance value is calculated using (1) [1]. Here R_1 is the resistance at the input of the first integrator, V_{in} is the input signal voltage, k is Boltzmann constant, T is the temperature, f_B is the frequency bandwidth, and B is the effective number of bits. The determined coefficients are translated into "R" and "C" values with the thermal noise constraint as per (1) and keeping the capacitor values such that the feedforward capacitors values are not too large as it loads the last integrating opamp. The determined first resistance value is only 10.93 k Ω and the capacitance is 1.78 pF. The stability and performance of a continuous-time delta-sigma modulator are strongly dependent on process variation as it changes the coefficients drastically. To mitigate the effect, coefficient tuning is desirable. Since resistors are connected either between input and input to the first opamp or between output of one opamp and input of next opamp, it is imperative that tuning using capacitance will be much easier

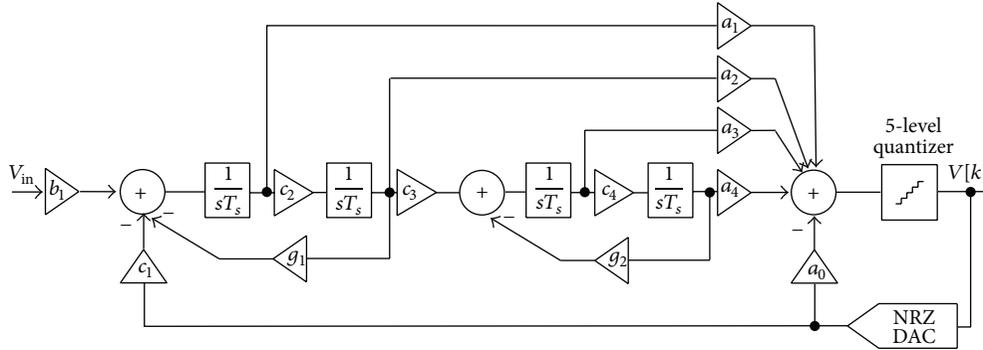


FIGURE 3: The block diagram of a 4th-order FF modulator with direct path for excess loop delay compensation.

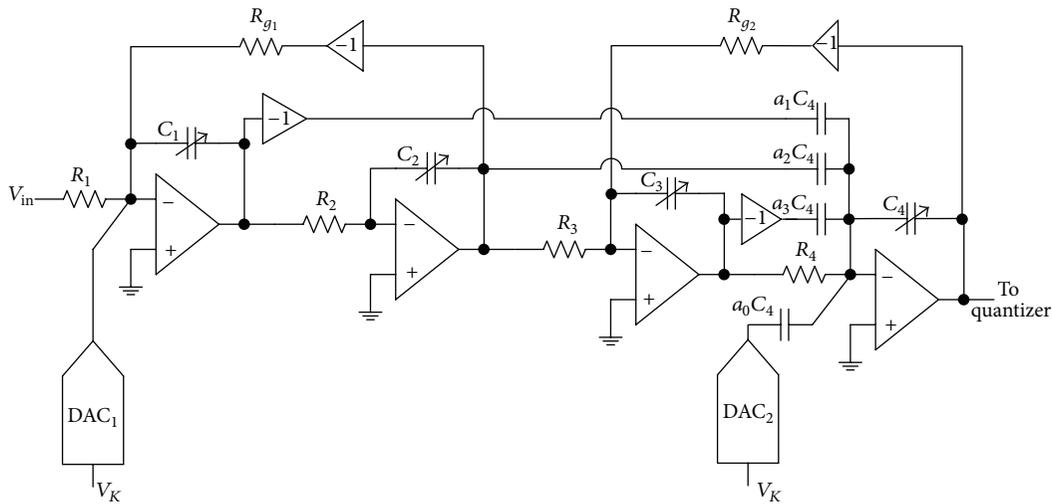


FIGURE 4: The block diagram of a 4th-order CIFF with direct path for excess loop delay compensation.

and effective to implement. Therefore, to combat process variation, capacitive tuning (C_1 to C_4) is implemented.

To predict the SNR, the behavioral simulation of the modulator is done with macro model of building blocks using the components from *analogLib* and *ahdlLib* of cadence. To include all the noises, thermal and circuit, transient noise is enabled while simulating the design. A 16384-point Hann window PSD predicts a SNDR of 69.7 dB for a tone at 1.0547 MHz.

3. Circuit Implementation

In this section, we describe the transistor level circuit designs of the building blocks used in the modulator.

3.1. Opamp. A generic two-stage miller-compensated opamp is used for a high-speed and a wide output swing. To mitigate input-referred flicker noise, long length input transistors are used. To keep the design simple and, power consumption low only one common mode feedback (CMFB) loop is used to maintain the output at V_{cm} . The opamp draws a total current

of 2.2 mA, including the CMFB and biasing, from a supply of 1.8 V. The designed opamp has GBW of $1.56 f_s$.

3.2. Comparator. A preamp stage with a gain of 10 is used as input stage. A regenerative circuit follows the preamp stage and finally SR-latch is used to output the decision. Separate references for differential input are used to avoid the coupling between the two differential inputs. The comparator settles its output within 120 ps.

3.3. Feedback DAC. Feedback DAC is designed in two parts. First part is a d-flip-flop [11] which is used to retime the output of the quantizer. In the second part, a current steering DAC is used for fast response. This DFF and the quantizer effectively introduce a delay of one clock between the input of the flash converter and the output of the feedback DAC. The cascade current source in the DAC cell is used to achieve a high-output resistance. The output impedance of the current DAC is 70 k Ω .

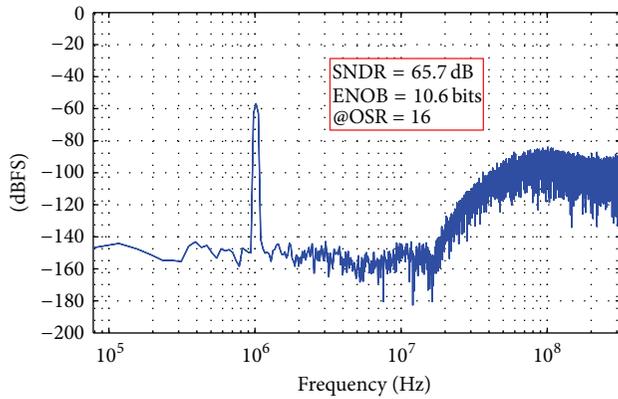


FIGURE 5: Output Spectrum of the modulator.

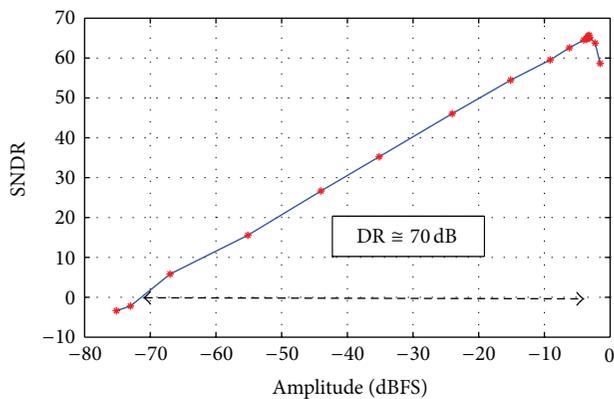


FIGURE 6: Amplitude versus SNDR of the modulator.

4. Results and Discussion

To illustrate the design methodology, a 4th-order 2-bit continuous-time delta-sigma modulator is designed in $0.18 \mu\text{m}$ CMOS technology. The implemented modulator is tested with a single tone at 1.0547 MHz. A 16384-point Hann window PSD is produced to ensure the sufficient accuracy. The resulted spectrum is shown in Figure 5. From Figure 5, it is determined that the peak SNDR is 65.7 dB over a bandwidth of 20 MHz. Figure 6 has the plot of SNR versus amplitude which gives a high dynamic range of 70 dB. The design consumes overall power of 19.7 mW to achieve a figure of merit (FoM) of 0.31 pJ/conv.

5. Conclusion

A systematic design methodology of a continuous-time delta-sigma modulator is described. A 640 MS/s, 20 MHz signal bandwidth 4th-order 2-bit continuous-time delta-sigma modulator is implemented in $0.18 \mu\text{m}$ CMOS technology to illustrate the design methodology. The CT coefficients are systematically computed compensating for excess loop delay. The designed modulator has a high SNDR of 65.7 dB and a high dynamic range of 70 dB for a signal band of 20 MHz. This modulator is well suited for WLAN applications. The

modulator consumes 19.7 mW power from a 1.8 V supply to achieve FoM of 0.31 pJ/conv.

Acknowledgments

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Research Article

An Inductorless Cascaded Phase-Locked Loop with Pulse Injection Locking Technique in 90 nm CMOS

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An inductorless phase-locked loop with subharmonic pulse injection locking was realized (PLL area: 0.11 mm^2) by adopting 90 nm Si CMOS technology. The proposed circuit is configured with two cascaded PLLs; one of them is a reference PLL that generates reference signals to the other one from low-frequency external reference signals. The other is a main PLL that generates high-frequency output signals. A high-frequency half-integral subharmonic locking technique was used to decrease the phase noise characteristics. For a 50 MHz input reference signal, without injection locking, the 1 MHz offset phase noise was -88 dBc/Hz at a PLL output frequency of 7.2 GHz ($= 144 \times 50 \text{ MHz}$); with injection locking, the noise was -101 dBc/Hz (spur level: -31 dBc ; power consumption from a 1.0 V power supply: 25 mW).

1. Introduction

Conventional multistandard wireless mobile terminals contain multiple RFICs. To reduce production costs, one-chip wideband RF LSI systems are desired. A great effort is being made to develop wideband and/or multiband RF solutions using highly scaled advanced CMOS processes. The use of such processes is beneficial to *A/D* and *D/A* converters and digital baseband circuits. However, it is very difficult to reduce the scale of RF/analog circuit blocks, especially power amplifiers and oscillator circuits, including voltage-controlled oscillators (VCOs) and phase-locked loops (PLLs), because of the presence of inductors that do not scale with advancements in technology.

In designing VCOs which generate signals in RF systems, ring-type VCOs (ring VCOs) are more attractive than LC-resonant-type VCOs (LC VCOs) in terms of their small area and wide frequency tuning range since they do not use large passive devices. However, they have poor phase noise with relatively high power consumption. Nevertheless, low-phase-noise ring VCO is still a possibility if some noise-suppression mechanism is applied. One of available options would be injection locking.

In the early days, Adler [1] and many other authors studied the behavior of VCOs with injection locking. Also,

there are numerous papers published in reference to VCOs with injection locking in order to achieve phase locking and high performances. Moreover, recently, PLLs with an injection-locked frequency divider and frequency multiplier, and a clock and data recovery circuit (CDR) were presented.

This paper describes a study on a ring-VCO-based PLL with pulse injection locking as a potential solution to realize a scalable inductorless PLL, which can generate wideband frequency signal with low supply voltage. Usually, the frequency range utilized consumer RF applications, such as wireless LAN *a/b/g/n*, Bluetooth, and digital TV (DTV), is very wide and spreading from 400 MHz to 6 GHz. Table 1 shows target performance of the proposed PLL. Generally, in RF systems using high transmitting power, a frequency synthesizer should generate higher-frequency signals up to 12 GHz to avoid injection pulling from a power amplifier. Then, some methods, such as using frequency dividers and mixers, are applied to widen frequency range [2, 3].

In addition, the proposed PLL is augmented with high-frequency half-integral subharmonic locking in order to improve its phase-noise performance. In Section 2, brief features of the proposed PLL are explained. In Section 2.1, high-frequency half-integral subharmonic locking is shown as a method of reducing phase noise. Also, the proposed

TABLE 1: Target performance.

VCO	Ring
Frequency range	6–12 GHz
Phase noise at 1 MHz offset	−100 dBc/Hz
CMOS process	90 nm
Supply voltage	1.0 V

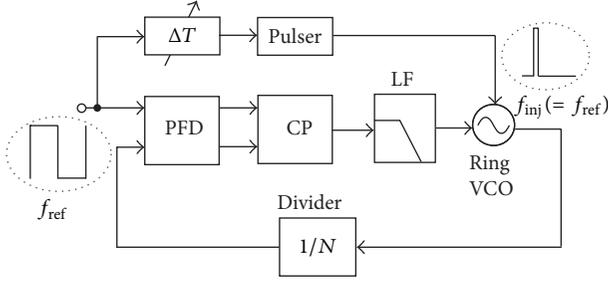


FIGURE 1: Injection-locked PLL with pulse injection.

cascaded PLL (CPLL) that can achieve injection locking at high frequencies from low-frequency reference is presented. Detailed circuit designs, such as a VCO and a charge pump which are able to realize wide-band operation, and the measurement results obtained from an implementation in 90 nm CMOS process are presented in Sections 3 and 4, respectively. Finally, we conclude this work in Section 5.

2. Injection Locking in Frequency Synthesizers

Figure 1 shows an injection-locked PLL (ILPLL). The PLL is based on a ring VCO that is able to generate high-frequency outputs across wide frequency range, as well as I/Q outputs. The PLL also consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a variable delay unit (ΔT), and a pulser.

PLLs that use ring type VCOs are required to have a wide loop bandwidth of the phase-locked loop for lowering their poor phase noise characteristics. However, there is a trade-off between the loop bandwidth and the stability of PLLs. In general, the loop bandwidth ($\omega_{-3\text{dB}}$) must be narrower than $\omega_{\text{ref}}/20 \sim \omega_{\text{ref}}/10$, where ω_{ref} is the reference-signal frequency [4]. Consequently, there is a limitation on lowering the phase noise in ring-VCO-based charge-pump PLLs (CP PLLs). Figure 2 shows phase noise characteristics of the PLL. In this case, the charge-pump noise of the PLL is assumed to be small enough and can be neglected. In Figure 2, phase noise is suppressed up to the loop bandwidth ($\omega_{-3\text{dB}}$) by the noise filtering of the loop. On the other hand, pulse injection locking is effective to reduce phase noise of ring VCOs since ring VCOs have a wider lock range with injection locking than that of LC VCOs because of their low quality factors. In designing subharmonically injection-locked oscillators (ILOs), N times frequency-multiplied signals as to the reference frequency

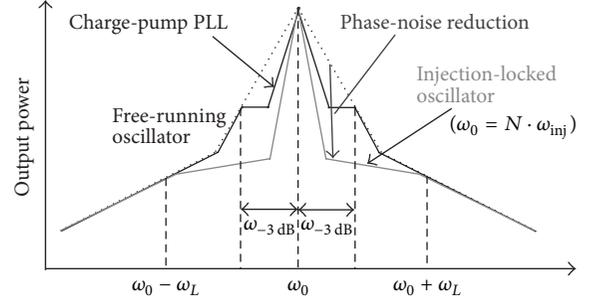


FIGURE 2: Phase-noise reduction with a charge-pump PLL and injection locking.

can be achieved. The lock range is decided by the power of N th superharmonics of the reference signal as follows [1, 5]:

$$\omega_L = \frac{\omega_{\text{out}}}{2Q} \cdot \sqrt{\frac{P_{\text{inj}N}}{P_0}}, \quad (1)$$

where Q represents the open-loop quality factor of an oscillator (calculated by using the open-loop transfer function of the oscillator [6]), ω_{out} is the output frequency of the oscillator under injection locked condition, $P_{\text{inj}N}$ is the N th harmonic power of the reference signal, and P_0 is the free-running output power of the oscillator. $P_{\text{inj}N}$ is approximately given by

$$P_{\text{inj}N} \propto \left\{ A \cdot D \frac{\sin(\pi D \cdot N)}{\pi D \cdot N} \right\}^2, \quad (2)$$

where A is the pulse amplitude, D is the duty cycle of pulses ($D = \Delta T/T$, ΔT : pulse width, T : period of pulses). From (1) and (2), the lock range ω_L can be rewritten as follows:

$$\omega_L \propto \frac{\omega_{\text{inj}}}{2Q} \cdot \frac{|\sin(\pi D \cdot N)|}{\sqrt{P_0}}, \quad (3)$$

where $\omega_{\text{inj}} (= \omega_0/N)$ is the injection-signal frequency [7].

The overall ILO output phase noise is obtained by adding the noise contributions in an ILO. Assuming that $S_{\text{ILO}}(\omega)$, $S_{\text{REF}}(\omega)$, and $S_{\text{VCO}}(\omega)$ are phase noise power functions of an injection-locked VCO, a reference signal, and a free-running VCO, respectively, the phase noise of an ILO, $S_{\text{ILO}}(\omega)$, simply can be expressed as

$$\begin{aligned} S_{\text{ILO}}(\omega) &= S_{\text{REF},M}(\omega) \cdot |H_{\text{LPF}}(j\omega)|^2 + S_{\text{VCO}}(\omega) \cdot |H_{\text{HPF}}(j\omega)|^2 \\ &= M^2 \cdot S_{\text{REF}}(\omega) \cdot \frac{1}{1+(\omega/\omega_L)^2} + S_{\text{VCO}}(\omega) \cdot \frac{(\omega/\omega_L)^2}{1+(\omega/\omega_L)^2}, \end{aligned} \quad (4)$$

where $S_{\text{REF},M}$ is the normalized phase noise power function with respect to the output frequency of f_{out} , and M means the ratio between the output frequency (f_{out}) and the input frequency (f_{inj}). $H_{\text{LPF}}(j\omega)$ and $H_{\text{HPF}}(j\omega)$ are low-pass and

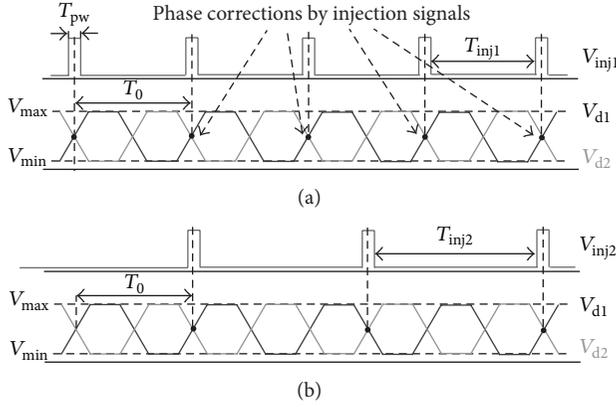


FIGURE 3: Voltage and current waveforms at differential output nodes of a VCO; (a) integral subharmonic locking ($f_0 = f_{inj}$), (b) half-integral subharmonic locking ($f_0 = 1.5f_{inj}$).

high-pass transfer functions, respectively [8]. Supposed that $H_{HPF}(j\omega)$ and $H_{LPF}(j\omega)$ have the first-order transfer functions and they have the same cutoff frequency of ω_L , the simple equation of (4) would be achieved [5, 9, 10].

In the proposed PLL, there are two kinds of phase locking mechanism: one is a phase-locked loop, and the other is pulse injection locking. In general, either of them is enough for phase locking. However, those two mechanisms are combined to get a wide frequency range operation with a low-phase-noise performance. The phase-locked loop, which uses a charge pump for controlling the oscillation frequency, is implemented to ensure correct frequency locking over the entire VCO tuning range. The final phase locking is done by injection locking to reference signal [11–13].

2.1. High-Frequency Half-Integral Subharmonic Locking Topology for Noise Reduction. A paper on half-integral subharmonic injection locking based on the use of a ring VCO has been presented [8]. A differential VCO can be easily designed to lock to half-integral subharmonics by giving its necessary symmetry properties. Suppose that a VCO consists of differential circuits and has a certain symmetry. As a method to achieve injection locking, a direct injection technique is applied, which uses nMOS switches that short the differential outputs for phase corrections. Figure 3 shows differential waveforms (V_{d1} , V_{d2}) of the VCO in the case of both integral ($f_0 = f_{inj}$) and half-integral subharmonic locking ($f_0 = 1.5f_{inj}$). The two output nodes are shorted when the injection signal (V_{inj1} , V_{inj2}) is input into the nMOS switches. Phase corrections may occur at the time and the jitter is reduced. Generally, there are two points of time during the period of the output signal when two output nodes can be shorted because of topological symmetry as shown in Figure 3. Consequently, the differential VCO is capable of both integral and also half-integral subharmonic locking.

One advantage of using half-integral subharmonic locking is to be able to use high-frequency reference signal and can make the locking range of injection locking, ω_L wide as shown in (1). Figure 2 and Equation (4) also show that

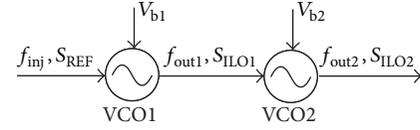


FIGURE 4: Concept of the cascaded ILOs.

the phase noise of the reference signal mainly affects the output phase noise at low offset frequencies and that the phase noise of the PLL becomes dominant as the offset frequency approaches the edge of the locking range [11]. Therefore, it will improve phase noise characteristics to the edge of the locking range to use high-frequency reference signals.

2.2. High-Frequency Signal Generation with Cascaded ILOs.

As shown in (3), the lock range is proportional to the input frequency of ω_{inj} . However, narrower pulses are required to achieve smaller D with increasing the multiplication ratio (N). Unfortunately, it is difficult to achieve sufficiently narrow pulses even with the use of nm-scale CMOS processes since the reference inputs also have certain jitter and parasitic components of the pulser limit the pulse width. In other words, there is limitation to generate high-frequency (over 5 GHz) injection-locked signals with low-frequency reference such as XTALs.

One solution is to employ cascaded oscillators [11], which make each multiplication ratio (N) smaller by using two multiplication processes. Figure 4 shows the concept of the cascaded ILOs. Firstly, the input signal, which has sufficiently high-power superharmonics, is injected into VCO1. Then, M_1 multiplied frequency signal ($f_{out1} = M_1 \cdot f_{inj}$) of the reference frequency can be achieved by tuning the VCO1 oscillation frequency properly. In this case, the output phase noise of VCO1 with injection locking can be expressed as follows:

$$S_{ILO1}(\omega) = M_1^2 \cdot S_{REF}(\omega) \cdot \frac{1}{1 + (\omega/\omega_{L1})^2} + S_{VCO1}(\omega) \cdot \frac{(\omega/\omega_{L1})^2}{1 + (\omega/\omega_{L1})^2}, \quad (5)$$

where ω_{L1} is the lock range that is proportional to the input frequency (f_{inj}) and can be calculated from (3).

The output signal of VCO1 is injected into VCO2 and locked to the output of VCO2 with the same process occurred in VCO1. Also, the output phase noise of VCO2 with injection locking can be expressed as follows:

$$S_{ILO2}(\omega) = M_2^2 \cdot S_{ILO1}(\omega) \cdot \frac{1}{1 + (\omega/\omega_{L2})^2} + S_{VCO2}(\omega) \cdot \frac{(\omega/\omega_{L2})^2}{1 + (\omega/\omega_{L2})^2} \approx M_2^2 \cdot \frac{1}{1 + (\omega/\omega_{L2})^2} \cdot S_{ILO1}(\omega), \quad (7)$$

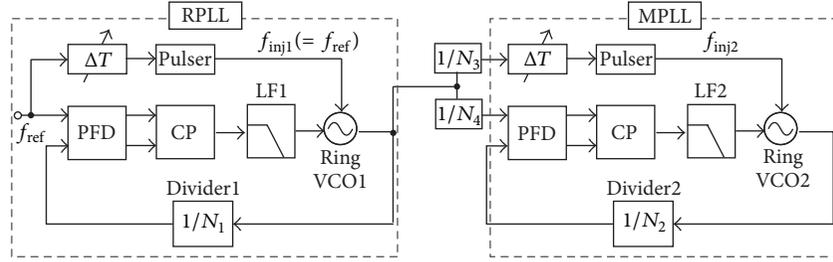


FIGURE 5: Proposed cascaded injection-locked PLL (CPLL) with pulse injection.

TABLE 2: Dividers ratio in Figure 5.

N_1	N_2	N_3	N_4
32	24, 36	1, 8	4, 8

where M_2 is the ratio between the output frequency of VCO2 (f_{out2}) and input frequency (f_{out1}) and ω_{L2} is the lock range of VCO2. When the offset frequency of ω is sufficiently lower than ω_{L2} (i.e., $\omega \ll \omega_{L2}$), (7) is held. In other words, sufficiently wide lock range makes it possible to neglect the secondary VCO phase noise up to the lock range in cascaded ILOs.

3. Proposed Injection-Locked PLL Topology

Figure 5 shows the configuration of the proposed PLL that enables the use of half-integral subharmonic locking, which was proposed in our previous work [13]. The proposed PLL consists of two injection-locked PLLs. A reference PLL, namely, RPLL generates reference signals to a main PLL, namely, MPLL from low-frequency external reference signals. In this topology, when we choose divider ratios (Table 2), respectively as, $N_2 = 36$, $N_3 = 1$, and $N_4 = 8$, the ratio between the reference signal to MPLL and the output frequency of MPLL may be 4.5 and high-frequency half-integral subharmonic locking can be applied. Variable time delay cells ΔT s are implemented to control the time when injection signals are input because phase corrections can occur easily when differential output nodes are shorted in the direct injection locking scheme (Figure 3).

3.1. Main PLL. Figure 6(a) shows the topology of the proposed delay cell that composes a ring VCO [13]. The delay cell contains an inverter latch as a negative conductance circuit that generates delay by positive feedback in order to satisfy the oscillation condition [14]. To tune the VCO output frequency widely, variable pMOS resistive loads are used. However, in the commonly used delay cells with pMOS resistive loads, the range of control voltage is limited from 0 V to the pMOS threshold voltage. In the proposed delay cell, a pMOS transistor is added into which the subcontrol voltage (V_{bn}) is input in order to make the range of sensitive voltages identical to the rail-to-rail voltage range (0 V to V_{DD}). For this purpose, the bias level shifted by about $V_{DD}/2$, V_{bn} , is input to the added pMOS transistor. As a result,

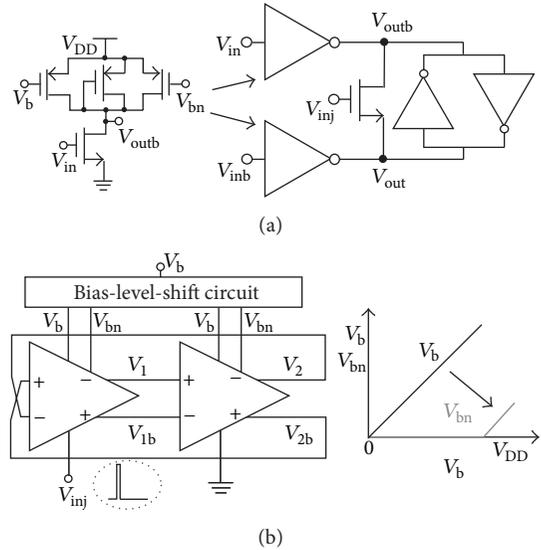


FIGURE 6: (a) Proposed differential delay cell, (b) two-stage differential VCO of MPLL with a bias-level-shift circuit.

the total equivalent resistance of the two pMOS transistors in parallel changes almost linearly versus the main control voltage, V_b . Consequently, the VCO output frequency can be tuned linearly across the wide tuning range [12, 13]. An nMOS switches are connected at the nodes between the differential nodes to achieve injection locking [15].

The proposed ring VCO is shown in Figure 6(b). It is based on a two-stage pseudo differential ring oscillator. Pulses which are generated by the on-chip pulser are injected into the left delay cell in the form of rail-to-rail pulses for injection locking. To maintain topological symmetry, an nMOS switch biased to 0 V is also applied in the right-side delay cell. We achieved the VCO tuning range of 6.02 GHz to 11.1 GHz across the rail-to-rail control voltage from the postlayout simulation of the VCO core with output buffers (90 nm CMOS process, $V_{DD} = 1.0$ V).

A tristate phase/frequency detector (PFD) is implemented, which consists of two D-flip flops, delay-path inverters, and an AND logic. The PFD detects phase and frequency difference between the reference signal and the divided VCO output and generates output pulses of V_{UP} and V_{DN} which are input into the charge pump to reduce the difference.

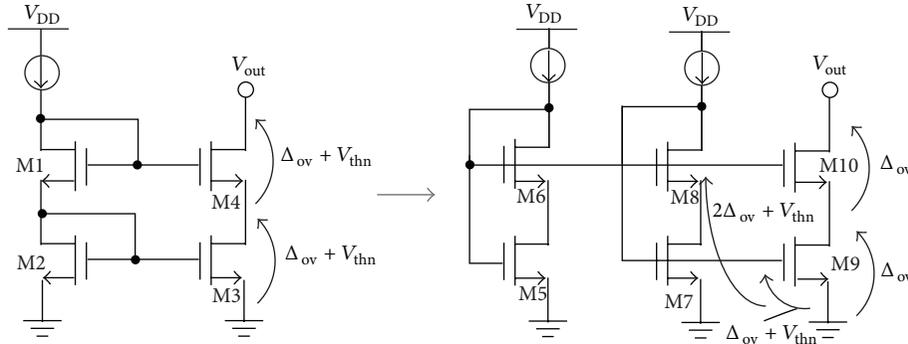


FIGURE 7: Sooch cascode current mirror circuit.

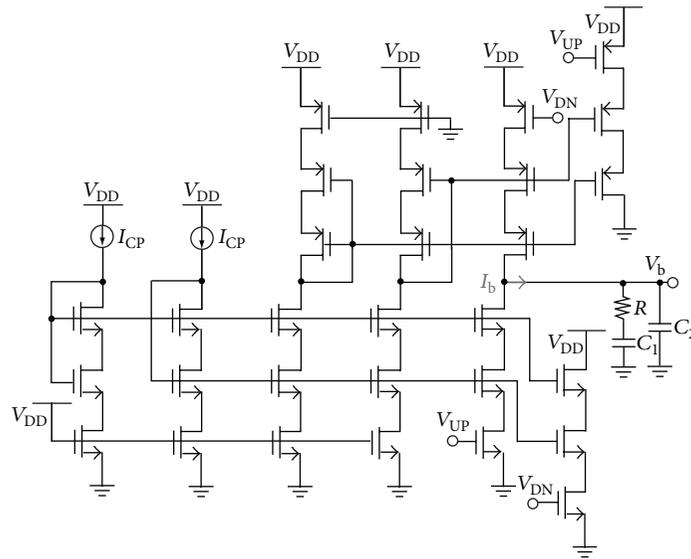


FIGURE 8: Proposed charge-pump (CP) circuit and loop filter (LF).

Figure 7 shows an implemented current mirror circuit to generate stable constant current from the charge pump. Usually, stacked current mirrors design can obtain better DC headroom and linearity with longer channel lengths as shown in the left side of Figure 7. In this case, DC headroom of the output voltage (V_{out}) is expressed as $2(\Delta_{ov} + V_{thn})$, where Δ_{ov} is the overdrive voltage of MOS transistors (M3, M4), and V_{thn} is an nMOS threshold voltage. In the case of Sooch cascode current mirror as shown in the right side of Figure 7, the MOS transistor, M5, is forced to operate in the triode region. The DC headroom can be reduced as $2\Delta_{ov}$ since MOS transistors operate in the saturation region except for M5 [16]. Consequently, low voltage operation can be achieved.

Proposed current switching charge pump (CP) that employs Sooch cascode current mirror is shown in Figure 8. Dummy switches are also implemented to maintain the balance between PFD outputs. Two external current sources ranged from $10 \mu A$ to $150 \mu A$ are used.

Figure 9 shows postlayout simulation results of the proposed charge pump, when $I_{CP} = 20 \mu A$ (90 nm CMOS process, 1.0 V supply). It shows that the charge pump can generate quite constant output current across the wide range

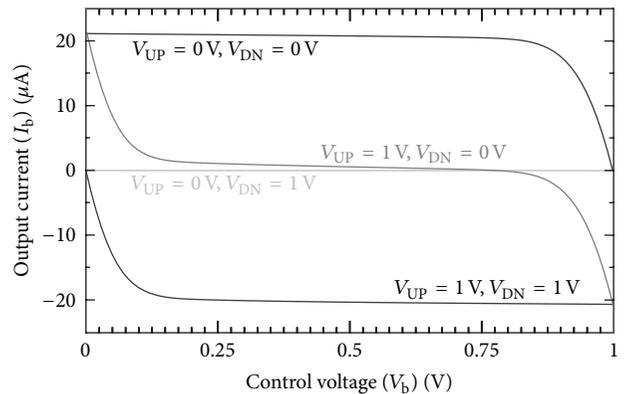


FIGURE 9: Charge-pump output current versus the control voltage (V_b), when $I_{CP} = 20 \mu A$.

of the output voltage (V_b). When $V_{UP} = 1 V$ and $V_{DN} = 0 V$, the result shows current mismatch between the up and down output currents as a function of the output voltage (V_b). The percentage mismatch error for $0.48 V \leq V_b \leq 0.81 V$ is less

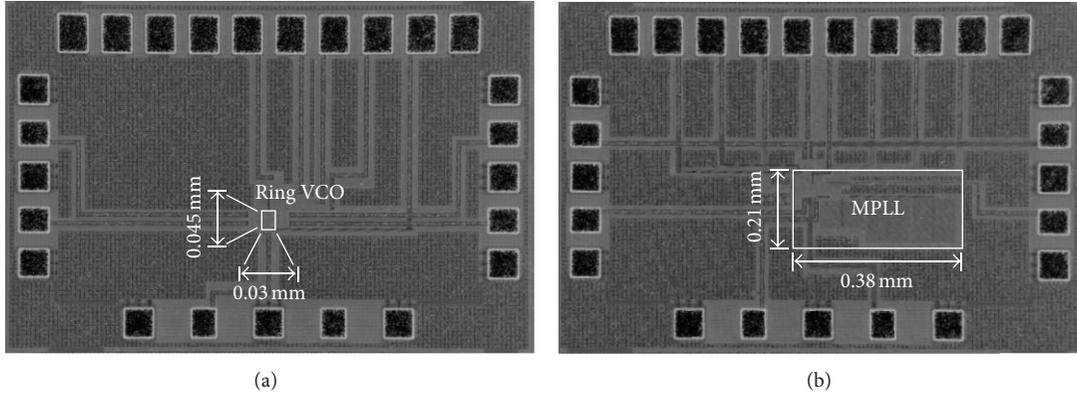


FIGURE 10: Chip micrographs; (a) proposed VCO and (b) proposed PLL.

than 2% and increases to less than 5% for $0.21\text{ V} \leq V_b \leq 0.85\text{ V}$.

A second-order lag-lead filter that consists of a register and two capacitors is implemented as a loop filter (LF) of the loop to suppress the charge-pump ripple. ($R = 16\text{ k}\Omega$, $C_1 = 41\text{ pF}$, $C_2 = 12\text{ pF}$). In this case, on-chip MIM capacitors were used.

The frequency divider consists of differential pseudo-nMOS latches to minimize chip area and achieve low power consumption [17]. The frequency divider chain consists of three divide-by-2 circuits and one divide-by-2/3 circuit. As a result, it can divide by 24 and 36 in the loop (i.e., divider ratio $N_1 = 24, 36$).

The loop dynamic characteristics are designed to have the unity-gain bandwidth of 2.8 MHz and phase margin of 16° (VCO gain: 5 GHz/V , $I_{CP} = 20\text{ }\mu\text{A}$, divider ratio $N_1 = 24$). When the divider ratio N_1 equals to 36, the unity-gain bandwidth of 2.2 MHz and phase margin of 19° are achieved. The PLL has poor phase margin that is related to the low damping factor and the slow settling time, because final phase locking is done not only by the phase-locked loop but also by injection locking. Injection locking that is applied into a phase-locked loop helps the phase margin to be improved [21]. In this case, large capacitance of C_2 is required to suppress the reference spur level due to the control voltage ripple. A loop bandwidth of the PLL is designed to be small enough compared to the lock range of injection locking to avoid the interference between two phase locking but can still achieve frequency locking.

To achieve subharmonic locking, an AND-based pulser is used, which is able to tune the pulse width below 40 ps by the analog control. Also, a variable time-delay unit (ΔT) which consists of inverters and tristate inverters was applied to match the zero-crossing points of differential VCO outputs to the pulses for effective injection locking.

3.2. Reference PLL. The proposed ring VCO used in RPLL is based on a four-stage pseudo differential ring oscillator. The same delay cell shown in MPLL (Figure 6(a)) is applied to widen frequency tuning range linearly. Also, long-gate channel MOS transistors are equipped in the delay cell to decrease VCO oscillation frequencies and reduce flicker noise

characteristics as a reference signal into MPLL. Pulses which are generated by the on-chip pulser are injected into the left delay cell in the form of rail-to-rail pulses for injection locking. To maintain topological symmetry, an nMOS switch biased to 0 V is also applied in the other delay cells. We achieved the VCO tuning range of 0.805 GHz to 2.85 GHz across the rail-to-rail control voltage from the postlayout simulation of the VCO core with output buffers (90 nm CMOS process, $V_{DD} = 1.0\text{ V}$).

The tristate PFD and CP presented in Figure 8 are implemented in RPLL. With postlayout simulation results of the charge pump (90 nm CMOS process, 1.0 V supply), the percentage mismatch error ($I_{CP} = 100\text{ }\mu\text{A}$) for $0.32\text{ V} \leq V_b \leq 0.70\text{ V}$ is less than 2% and increases to less than 5% for $0.24\text{ V} \leq V_b \leq 0.76\text{ V}$ ($V_{UP} = 1\text{ V}$, $V_{DN} = 0\text{ V}$).

As a loop filter (LF), a second-order lag-lead filter is implemented. The filter consists of a register ($R = 16\text{ k}\Omega$), and two on-chip capacitors ($C_1 = 41\text{ pF}$, $C_2 = 1\text{ pF}$). The frequency divider chain in RPLL consists of five divide-by-2 circuits. As a result, it can divide by 32 (i.e., divider ratio $N_2 = 32$). Finally, the AND-based pulser and the variable time-delay unit (ΔT) were implemented for effective injection locking. In RPLL, an injection frequency of f_{inj1} is same to a reference frequency of f_{ref} .

4. Measurement Results

4.1. Main PLL (MPLL). Figures 10(a) and 10(b) show chip micrograph of the differential ring VCO and a PLL, respectively. To clear the effectiveness of the proposed PLL, the VCO cell used in the PLL was also fabricated. They were fabricated by a 90 nm Si CMOS process. The area of the ring VCO core is $0.030 \times 0.045\text{ mm}^2$ including the bias-level-shift circuit and the pulser. The PLL circuit occupies an area of $0.38 \times 0.21\text{ mm}^2$. They were measured in 1.0 V supply condition. Also, the PLL circuit was measured using $20\text{ }\mu\text{A}$ -current-sources (I_{CP}) into the charge pump.

During free-running operation, the frequency tuning range of the VCO was from 6.35 GHz to 11.5 GHz as shown in Figure 11. It was measured by using an Agilent Technologies E5052B signal source analyzer. It also shows that the VCO

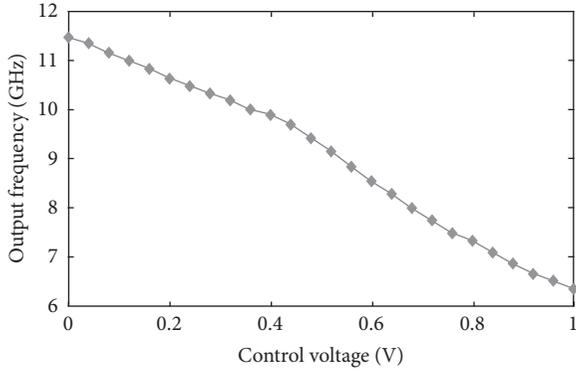


FIGURE 11: Measured frequency tuning range of the VCO.

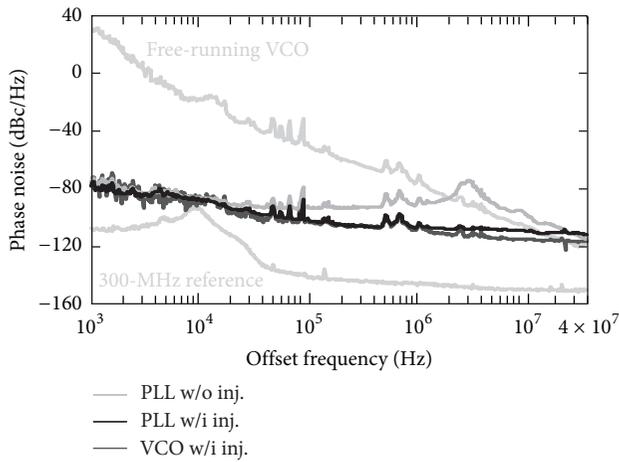


FIGURE 12: Measured phase noise characteristics at 7.2 GHz from the VCO and PLL output without and with injection locking.

output frequency could be tuned quite linearly versus the rail-to-rail control voltage (V_b) due to the bias-level-shift circuit. When the VCO output frequency (f_0) is 7.18 GHz, the total power consumption of the VCO (with the bias-level-shift circuit and pulser) was 8.4 mW.

Phase noise characteristics of the VCO and PLL at $f_0 \approx f_{out} = 7.2$ GHz without and with injection locking are shown in Figure 12 as measured by the signal source analyzer. In addition to them, phase noise characteristics of the 300 MHz reference signal are shown in Figures 12 and 14. A 1 MHz-offset phase noise of -75.8 dBc/Hz was generated in the free-running VCO. With injection locking, a 1 MHz offset phase noise of -108 dBc/Hz was generated, which was improved by 32 dB compared to the former. On the other hand, a 1 MHz-offset phase noise of -91.3 dBc/Hz was generated in the PLL when the PLL was only locked by the phase-locked loop. Due to the poor phase margin, gain peaking at the offset frequency of about 3 MHz was observed. With injection locking, a 1 MHz offset phase noise of -107 dBc/Hz was generated, which was improved by 16 dB compared to the former.

Figure 13 shows calculated phase noise characteristics by using (4) and the measurement phase noise of the free-running VCO and the reference signal as shown in Figure 12.

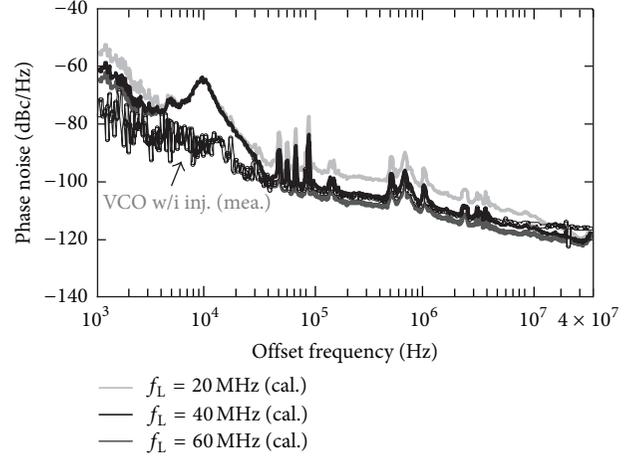


FIGURE 13: Calculated phase noise by using (4) and measure phase noise characteristics as shown in Figure 12.

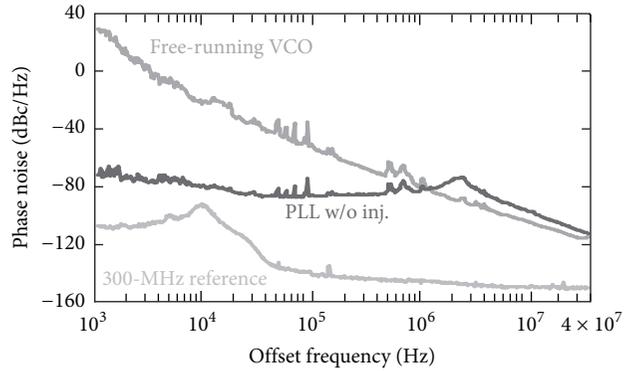


FIGURE 14: Measured phase noise characteristics at 10.8 GHz from the VCO and PLL output without injection locking.

The results show that wider lock range makes lower phase noise characteristics within the lock range. From the calculated result of $f_L = \omega_L/2\pi = 40$ MHz, (4) is well matched to the measurement results except the offset-frequency region up to about 30 kHz. It is because that flicker noise model as expressed in [5] is not included for simplicity and certain spurs occurred at the offset frequency of about 10 KHz were measured.

Phase noise characteristics of the VCO and PLL at $f_0 \approx f_{out} = 10.8$ GHz are shown in Figure 14. A 1 MHz offset phase noise of -79.5 dBc/Hz and -83.7 dBc/Hz were generated in the free-running VCO and the PLL, respectively. Phase noise reduction with injection locking could not be achieved since it was difficult to generate effective injection pulses with sufficient power for achieving the injection-locked condition at that high output frequency.

4.2. Cascaded PLL. Figure 15 shows a chip micrograph of the proposed CPLL. It was fabricated by a 90 nm Si CMOS process. It includes both RPLL and MPLL that occupy an area of 0.11 mm^2 . It was measured in 1.0 V supply condition. Also, the PLL circuit was measured using $100 \mu\text{A}$ current

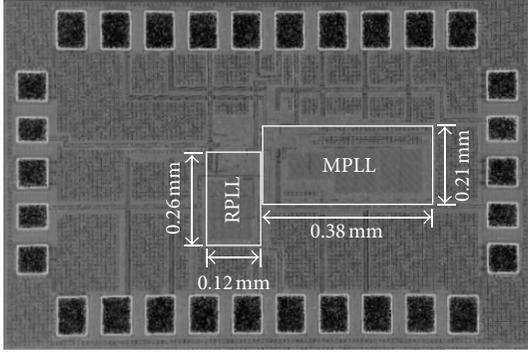


FIGURE 15: A chip micrograph of the proposed cascaded PLL.

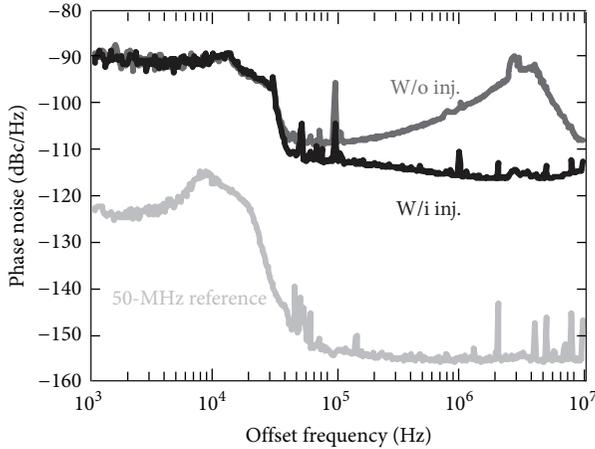


FIGURE 16: Measured phase noise characteristics of RPLL output at 1.6 GHz.

sources into RPLL charge pump and $20 \mu\text{A}$ current-sources into MPLL charge pump. RPLL was locked to reference signals of 50 MHz which were generated by the pulse pattern generator.

Figure 16 shows the phase noise characteristics at $f_{\text{rout}} = 1.6 \text{ GHz}$ ($= 32 \times 50 \text{ MHz}$) as measured by an Agilent Technologies E5052A signal source analyzer. Without injection locking, a 1 MHz-offset phase noise of -100 dBc/Hz was generated in RPLL. Due to the poor phase margin, gain peaking at the offset frequency of about 4 MHz was observed. With injection locking, the measured phase noise was -116 dBc/Hz at an offset of 1 MHz. It shows a 16-dB phase-noise reduction with injection locking. Also, phase noise characteristics of the external reference signal are shown in Figure 16. At 10 KHz and 1 MHz offset, the phase noise of the reference signal were -117 and -155 dBc/Hz , respectively.

Figure 17 shows the phase noise characteristics at $f_{\text{mout}} = 7.2 \text{ GHz}$ ($= 144 \times 50 \text{ MHz}$). 0.2 GHz injection signals were injected when N_2 , N_3 , and N_4 are corresponding to 36, 8, and 8, respectively. Also, 1.6 GHz injection signals were injected when N_2 , N_3 , and N_4 are corresponding to 36, 1, and 8, respectively. Without injection into MPLL, a 1 MHz offset phase noise of -88 dBc/Hz was generated in the PLL. With integral subharmonic injection locking ($f_{\text{mout}} = 36 \times$

TABLE 3: Performance summary at $f_{\text{out}} = 7.2 \text{ GHz}$.

This work	MPLL VCO	MPLL	CPLL	
f_{out} [GHz]		7.2		
f_{ref} [MHz]	—	300	50	
f_{inj} [MHz]	300	300	200	1600
$f_{\text{out}}/f_{\text{inj}}$	24	24	36	4.5
$L(\Delta f) _{\Delta f=1 \text{ MHz}}$ [dBc/Hz]	-108	-107	-99	-101
Power consumption [mW]	8.4	14	25	
Area [mm^2]	0.0014	0.080	0.11	

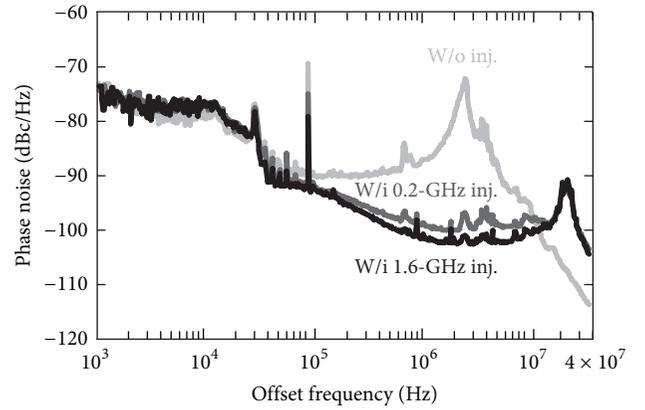


FIGURE 17: Measured phase noise characteristics of CPLL output at 7.2 GHz.

$f_{\text{inj}2}$, $f_{\text{inj}2} = 0.2 \text{ GHz}$), the measured phase noise was -99 dBc/Hz at an offset of 1 MHz. With high-frequency half-integral subharmonic locking ($f_{\text{mout}} = 4.5 \times f_{\text{inj}2}$, $f_{\text{inj}2} = 1.6 \text{ GHz}$), we successfully achieved 2 dB lower phase noise at 1 MHz offset than the former. A 4 MHz offset phase noise was improved by 4 dB in the latter case, compared with the former. The results show that high-frequency reference injections can widen the injection lock range. However, there was a spur around the offset frequency of 25 MHz owing to the RPLL spur level, and the spur limited the lock range widening with high-frequency signal injections.

Usually, spurs are induced by periodic phase shift due to injection locking. The spur level can be expressed as follows:

$$\sqrt{\frac{P_{\text{spur}, \omega_{\text{inj}}}}{P_0}} \approx \frac{\omega_0}{2Q\omega_{\text{inj}}} \cdot \sqrt{\frac{P_{\text{inj}N}}{P_{\text{osc}}}} = \frac{\omega_L}{\omega_{\text{inj}}}, \quad (8)$$

where $P_{\text{spur}, \omega_{\text{inj}}}$ represents the spur levels occurred by the reference signal at $f_0 \pm f_{\text{inj}}$, and P_0 is the injection-locked output power of the oscillator [22]. As shown in this equation, the spur level would be reduced lowering the lock range with the same reference frequency, however, which is undesirable to reduce phase noise characteristics.

Calculated phase noise characteristics by using (6) and measure phase noise characteristics, as shown in Figures 12 and 16, are shown in Figure 18. In this case, the lock range was supposed to be proportional to the input frequency and the coefficient was 0.14, which was expected in Figure 13. In

TABLE 4: Performance comparison of PLLs.

Reference	CMOS Technology	f_0 [GHz]	$N = f_0/f_{ref}$	$L_{in-band}$ [dBc/Hz]	$L_{normalized}^*$ [dBc/Hz ²]	Power [mW]	Area [mm ²]	VCO
This work	90 nm	1.6	32	-116	-223	11 (sim.)	0.031	Ring
		7.2	144	-101	-221	25	0.11	
		9.6	192	-93	-216	27		
[11]	90 nm	20	20	-113	-229	38	0.46	LC
[18]	90 nm	9.24	35	-97	-212	56	0.09	Ring
[19]	0.18 μ m	8.98	17	-110	-222	58	0.77	LC
[20]	0.18 μ m	8.45	32	-98	-212	117	5.5	LC

*Normalized in-band phase noise = $L_{in-band} - 20\log N - 10\log f_{ref}$.

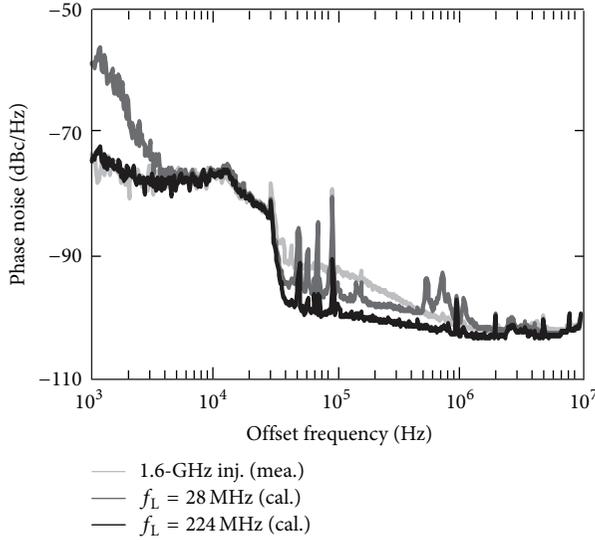


FIGURE 18: Calculated phase noise by using (6) and measuring phase noise characteristics as shown in Figures 12 and 16.

the results, phase noise characteristics especially at the offset frequency of 500 kHz, 700 kHz, and lower than 5 kHz due to the secondary VCO (VCO2) would be reduced by using high-frequency injection signals ($f_{inj} = 1.6$ GHz, $f_L = 224$ MHz). In Figure 18, measured phase noise characteristics from the offset frequency of 30 kHz to 1 MHz were degraded compared with calculated results due to induced noise from the MPLL loop.

Figure 19 shows the phase noise characteristics at $f_{mout} = 9.6$ GHz ($= 192 \times 50$ MHz). In these cases, N_2 , N_3 , and N_4 are corresponding to 24, 8, and 8, respectively. Without injection into MPLL, a 1 MHz offset phase noise of -85 dBc/Hz was generated in the PLL. With integral subharmonic injection locking ($f_{mout} = 48 \times f_{inj2}$, $f_{inj2} = 0.2$ GHz), the measured phase noise was -93 dBc/Hz at an offset of 1 MHz. In Figure 19, spur levels around the offset frequency of 25 MHz were decreased, because the phase-locking effect of injection locking was decreased.

The PLL generated reference spurs of lower than -31 dBc at the output frequency of 7.2 GHz with 1.6 GHz injections, as shown in Figure 20(a). At the output frequency of 9.6 GHz with 0.2 GHz injections, reference spurs of lower than -27 dBc were measured as shown in Figure 20(b).

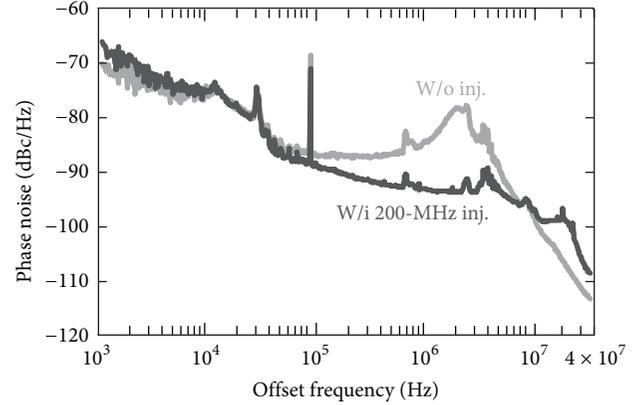


FIGURE 19: Measured phase noise characteristics of CPLL output at 9.6 GHz.

A performance summary at the output frequency of 7.2 GHz of the fabricated chips are given in Table 3, when injection locking was established. It shows that high-frequency injections are effective to reduce the phase noise because a wide injection lock range can be achieved.

A performance comparison of the PLL with other PLLs that were designed using various kinds of phase-locking methods is given in Table 4. Unfortunately, the proposed PLL cannot cover wide frequency range from 6 GHz to 12 GHz as shown in Table 1, due to the VCO tuning range and limitation of tunable divider ratio. To make a fair in-band phase noise comparison between various kinds of PLL designs, the dependency of in-band phase noise on f_{ref} and N should be normalized out [23]. Therefore, normalized in-band phase noise $L_{normalized}$ was applied for comparison. The proposed PLL shows a relatively good $L_{normalized}$ value. Also its area and power consumption are small and comparable to that of other circuits.

5. Conclusion

An inductorless PLL architecture, using the combination of a phase-locked loop, and injection locking with a ring VCO was proposed. The proposed CPLL that consists of two PLLs was designed in order to generate high-frequency output signals with low-frequency external reference signals. High-frequency half-integral subharmonic injection locking

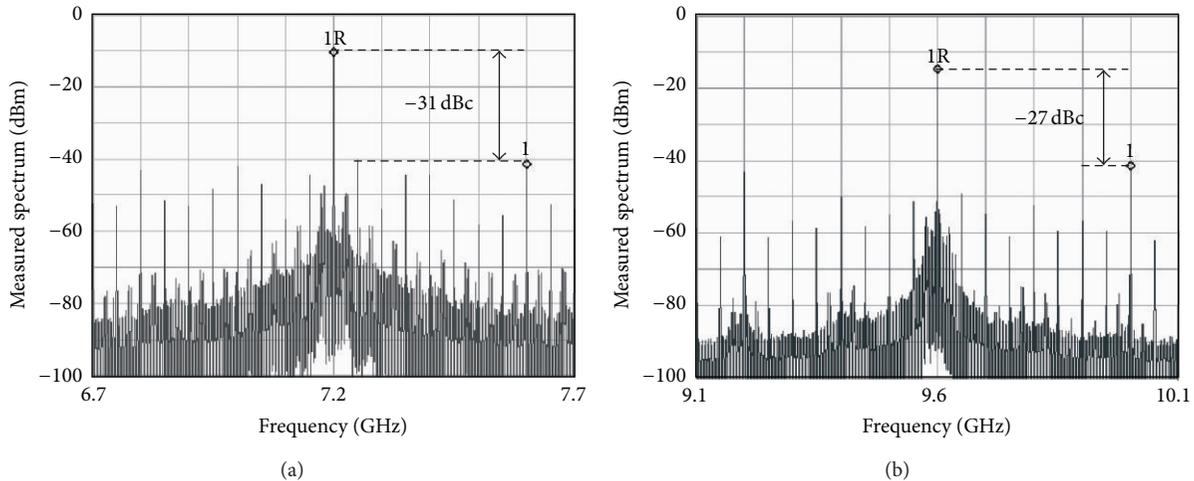


FIGURE 20: Measured frequency spectra of CPLL output (a) at 7.2 GHz and (b) at 9.6 GHz.

to improve the phase noise characteristics of the inductorless PLL was implemented.

The injection-locked PLL was fabricated by adopting 90 nm Si CMOS technology. A 1 MHz-offset phase noise of -101 dBc/Hz was achieved at an output frequency of 7.2 GHz, which was improved by 25 dB compared with that of the free-running VCO. The area of this inductorless PLL was as small as 0.11 mm^2 with low power consumption of 25 mW.

Acknowledgments

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