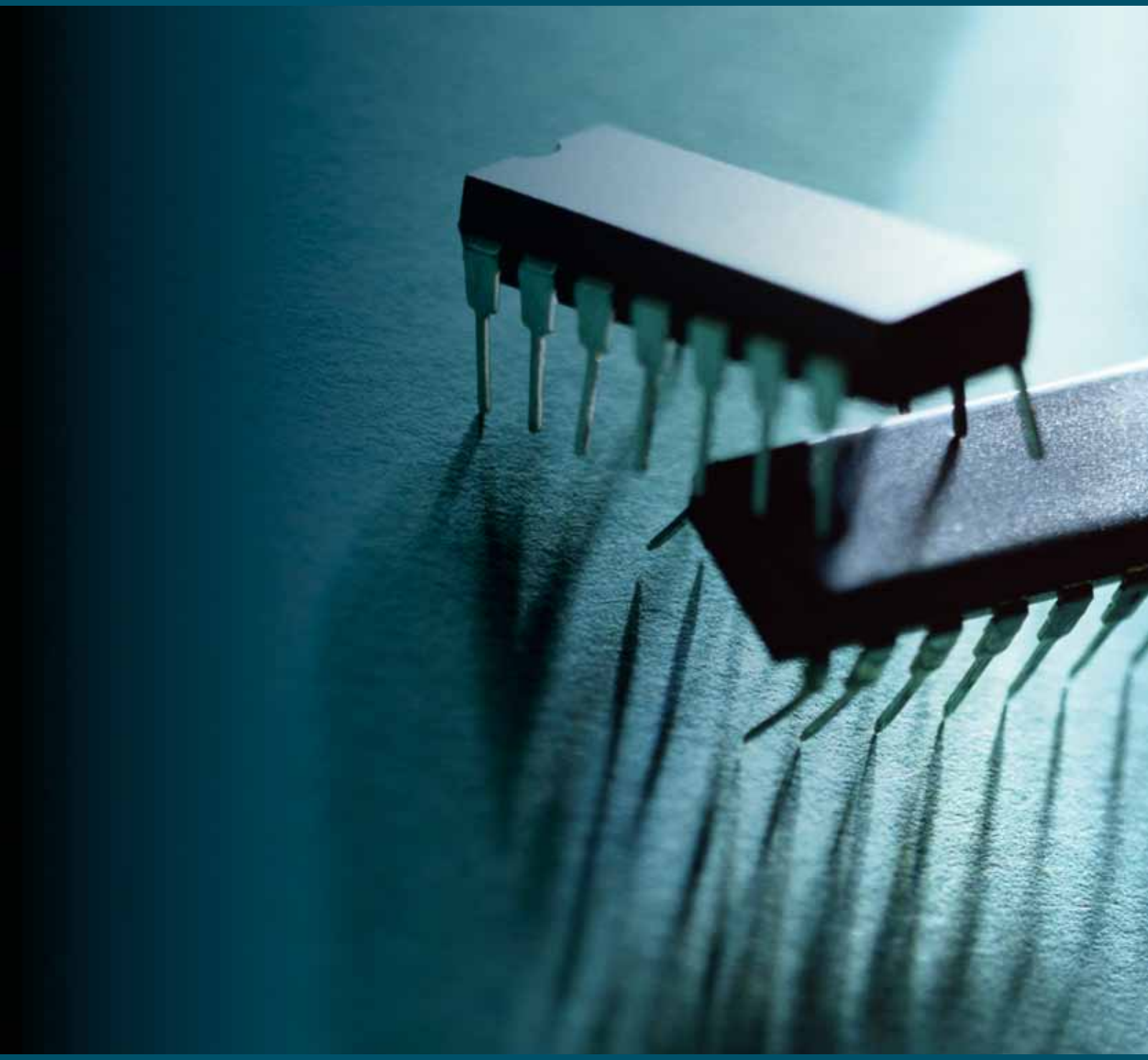
Active and Passive Electronic Components

Metal-Insulator-Semiconductor Field-Effect Transistors

Guest Editors: Kuan-Wei Lee, Edward Yi Chang, Yeong-Her Wang, Pei Wen Li, and Yasuyuki Miyamoto



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Editorial Board

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Editorial
Metal-Insulator-Semiconductor Field-Effect Transistors

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In the last few decades, there has been a tremendous progress in metal-insulator-semiconductor field-effect transistors (MISFETs) and their applications. Among many possible semiconductor material choices for MISFETs, Ge, III-V, and III-N semiconductors have attracted considerable attentions as the channel for MISFETs. These devices are used in a large number of different circuits such as power amplifiers, low-noise amplifiers, mixers, frequency converters, and phase shifters. Also, high-k dielectric materials are now playing an important role in the high-mobility-channel devices for improving speed and drive current performance. We invite authors to contribute original research as well as review articles on the recent progress in all kinds of MISFETs and their applications.

One paper in this issue entitled "*The improvement of reliability of high-k/metal gate pMOSFET device with various PMA conditions*" discusses the improvement of reliability of high-k/metal gate pMOSFET with various postmetallization annealing conditions.

In another paper entitled "*Gate stack engineering and thermal treatment on electrical and interfacial properties of Ti/Pt/HfO_2/InAs pMOS capacitors*," the authors explore effects of gate stack engineering and postmetallization annealing on electrical and interfacial properties of Ti/Pt/HfO_2/InAs pMOS capacitors. An As-rich InAs interfacial layer further suppresses the surface states, evidenced by the reduction of gate leakage, and depletion/inversion capacitances.

The paper "*Comparative study of SiO_2, Al_2O_3, and BeO ultrathin interfacial barrier layers in Si metal-oxide-semiconductor devices*" investigates effects of SiO_2, Al_2O_3, and BeO ultrathin interfacial barrier layers on Si MOS devices. Inserting an ALD BeO interfacial layer between the Si channel and high-k gate dielectric enhances high-field carrier mobility and improves MOSFET parameters and reliability characteristics while maintaining a similar EOT.

The paper "*GaN-based high-k praseodymium oxide gate MISFETs with $P_2S_5/(NH_4)_2S_x$ + UV interface treatment technology*" presents the AlGaN/GaN MISFETs with high-k Pr_2O_3 in which the AlGaN Schottky layers are treated with $P_2S_5/(NH_4)_2S_x$ + UV illumination. This novel pretreatment is therefore proven to be suitable for low-noise GaN MISFET applications.

The paper entitled "*Comprehension of postmetallization annealed MOCVD-TiO_2 on $(NH_4)_2S$ treated III-V semiconductors*" deals with the electrical characteristics of MOCVD-TiO_2 grown on p-type InP and GaAs. With $(NH_4)_2S$ treatment, the electrical characteristics of MOS capacitors are improved due to the reduction of native oxides. The electrical characteristics can be further improved by the postmetallization annealing, which causes hydrogen atomic ion to passivate defects and the grain boundary of polycrystalline TiO_2.

The paper entitled "*A novel nanoscale FDSOI MOSFET with block-oxide*" proposes a novel planar fully-depleted

silicon-on-insulator nMOSFET with block-oxide-enclosed Si body by applying oxide sidewall spacer technology. The presence of block-oxide along the sidewalls of the Si body significantly reduces the influence of drain bias over the channel. The novel FDSOI structure shows improved performance over conventional FDSOI.

These papers show the research topics representative of some of the active and original areas of MISFETs. It is hoped that these articles included here aid the reader in gaining a better understanding of some new and important research field.

The guest editors are pleased to submit this special issue to Hindawi Publishing Corporation and hope that this issue accomplishes the goal of highlighting outstanding advances in the MISFETs. Many thanks are expressed to all the reviewers who contribute their most valuable comments.

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Research Article

A Novel Nanoscale FDSOI MOSFET with Block-Oxide

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We demonstrate improved device performance by applying oxide sidewall spacer technology to a block-oxide-enclosed Si body to create a fully depleted silicon-on-insulator (FDSOI) nMOSFET, which overcomes the need for a uniform ultrathin silicon film. The presence of block-oxide along the sidewalls of the Si body significantly reduces the influence of drain bias over the channel. The proposed FDSOI structure therefore outperforms conventional FDSOI with regard to its drain-induced barrier lowering (DIBL), on/off current ratio, subthreshold swing, and threshold voltage rolloff. The new FDSOI structure is in fact shown to behave similarly to an ultrathin body (UTB) SOI but without the associated disadvantages and technological challenges of the ultrathin film, because a thick Si body allows for reduced sensitivity to self-heating, thereby improving thermal stability.

1. Introduction

Semiconductor science, triggered by the impetus of a growing market for faster, more reliable, and less costly chips, has been undergoing a rapid technological development [1]. Many of these new technologies, however, suffer from undesirable side effects. For example, as the gate length of CMOS—the bulk complementary metal-oxide semiconductor—is decreased, short-channel effects (SCEs), such as drain-induced barrier lowering (DIBL) and threshold voltage (V_{TH}) rolloff, become a significant problem because S/D encroachment begins to limit the gate's ability to control the channel. Also, due to the existence of the PN junction between the Si substrate and the S/D regions, a large junction leakage current prevents the use of scaled-down transistors in low standby power (LSTP) applications. Moreover, the parasitic capacitance of the transistor may strongly affect the characteristics of CMOS devices [2–4]. Therefore, the use of planar technology for ultralarge-scale integrated (ULSI) circuits becomes more challenging.

Recently, silicon-on-insulator (SOI) technology has demonstrated promise for nano-CMOS scaling. Compared to its bulk Si counterparts, SOI offers reduced capacitance and lower OFF-state leakage current (I_{OFF}), mainly due to the presence of a buried oxide (BOX) layer under the Si active layer [5]. This can be attributed to the fact that the BOX can be seen as a "blocking layer" to reduce the drain electric field. Also, because the active region is fully isolated, it avoids the latch-up problem of classical CMOS devices.

The benefits of SOI technology, however, are not without associated problems. A partially depleted (PD) SOI transistor cannot achieve an improved performance in future sub-45 nm semiconductor devices, due to the electrical properties of PDSOI MOSFET relative to the thickness of the Si layer. It has been proved that a thick Si film makes reducing DIBL very difficult [6]. The fully depleted (FD) ultrathin body (UTB) SOI MOSFET is able to improve the short-channel characteristics but suffers from high S/D series resistance, because the semiconducting Si layer is, by definition, ultrathin. Also, when the gate-to-source overdrive voltage (V_{GT}) is high enough, the self-heating effect causes a negative incremental conductance in the UTBSOI MOSFET associated with thermal instability. Consequently, the reliability of SOI devices will be degraded by these issues [7–11].

Our previous studies revealed that some of the unique features of the FDSOI MOSFET with block-oxide (bFDSOI) could allow it to replace the UTBSOI structure for CMOS scaling [12–14]. The device parameters of bFDSOI and UTBSOI were not optimized; however, neither bFDSOI nor UTBSOI showed high drain ON-state current (I_{ON}). Now, equipped with a block-oxide-enclosed Si body using oxide sidewall spacer technology, this paper presents a fully

depleted silicon-on-insulator (FDSOI) nMOSFET to improve device performance, without using ultrathin silicon film. Also, the authors have optimized the device parameters to enhance current drive without losing the desired electrical characteristics.

This paper is organized as follows: the device structures and their corresponding simulations are described in Section 2. In Section 3, the electrical characteristics are compared between the bFDSOI-FETs and their counterparts in the FDSOI-FET, UTBSOI-FET, and elevated S/D (E-S/D) UTBSOI-FET before a brief summary is carried out in Section 4.

2. Device Structures and Simulations

ISE-TCAD was used to design and simulate the thin S/D and the recessed S/D bFDSOI-FETs. The key steps for processing the bFDSOI are shown in Figure 1. First, the Si body was patterned with e-beam (see Figure 1(a)), and for thin S/D bFDSOI-FET, 60 nm thick oxide was deposited using chemical vapor deposition (CVD) as a blocking layer. The deposited oxide layer was then etched back to form the sidewall spacers of the Si body (see Figure 1(b-1)). A layer of poly-Si (5 nm thick) was then deposited to act as an active layer (see Figure 1(c-1)). For the recessed S/D bFDSOI-FET, a 15 nm thick oxide was deposited and etched back to form the sidewall spacers of the Si body (see Figure 1(b-2)). Next, poly-Si was deposited and planarized with chemical mechanical polishing (CMP). Poly-Si (5 nm thick) was then redeposited to form the active region (see Figure 1(c-2)). For both bFDSOI-FETs, a 2.3 KeV boron difluoride (BF_2) channel implantation at a dosage of 1.15×10^{12} cm^{-2} was performed, followed by rapid thermal annealing. Hence, the values of V_{TH} for both devices were determined. Then, 1.4 nm thick oxide was grown and a 50 nm thick poly-Si layer was deposited, followed by gate patterning. After gate patterning, a layer of nitride was deposited and etched back by dry etching. Next, 10 nm oxide was deposited as an implantation screen layer. In order to form S/D regions for bFDSOI-FETs, arsenic ions were implanted at a dosage of 2.1×10^{14} cm^{-2} and an ion implantation energy of 14 KeV, followed by thermal annealing. As a result, the source/drain resistance for both devices was determined playing an important role in drain currents. The second sidewall spacers were then formed by dry etching. After contact formation, bFDSOI-FETs were achieved.

In this paper, some technical "tricks", such as S/D extension (SDE) implants [15], asymmetric halo [16], and retrograde channel profiles [17], were not used for our bFDSOI-FETs because the purpose of this work is to emphasize the importance of the block-oxide in reducing the SCEs. The device parameters used are listed as follows. For thin S/D and recessed S/D bFDSOI-FETs, typical values of Si body thickness (T_{Si}) and poly-Si channel thickness (T_{CH}) were 30 nm and 5 nm, respectively. Additionally, three types of SOI MOSFETs (FDSOI, UTBSOI, and E-S/D UTBSOI) were designed; the parameters were based on the same conditions for the simulation. For the FDSOI-FET, the typical value of T_{Si} is 30 nm. For the UTBSOI-FET, the typical value of T_{Si} (= T_{CH}) is 5 nm. For the E-S/D UTBSOI-FET, the typical value of T_{Si} (= T_{CH}) is 5 nm, and the raised S/D thickness is 35 nm. The other parameters, BOX thickness (T_{BOX}) and front-gate oxide thickness (T_{GOX}) are 50 nm and 1.4 nm, respectively.

3. Results and Discussion

The physics models in this paper, including the generation and recombination model, the effective intrinsic density model, and the basic mobility models, were specified for the I_{DS}-V_{GS} characteristics of bFDSOI-FETs and its counterparts. Among them, the mobility models include a doping-dependence model and a high-field-saturation model (velocity saturation for electrons), based on the hydrodynamic Canali model. Besides the models used in I_{DS}-V_{GS} simulation, a local-carrier temperature-dependent impact-ionization model is attached to the generation and recombination models, a transverse-field dependence model is attached to the basic mobility models, and a hydrodynamic model is used to simulate numerically the I_{DS}-V_{DS} characteristics of bFDSOI-FETs and its counterparts [18].

For bFDSOI-FETs, owing to the presence of single crystal Si body, the poly-Si active layer can be recrystallized after annealing. In the simulation study, the crystalline Si values used for bFDSOI-FETs were the same as those used for FDSOI and UTBSOI devices. The major parameters for the comparison are listed as follows. V_{DS} is the voltage bias applied between drain and source, $V_{TH,lin}$ is the linear threshold voltage at V_{DS} = 0.05 V, and $V_{TH,sat}$ is the saturation threshold voltage at V_{DS} = 1.0 V. The threshold voltage is extracted using the constant current method at I_{DS} = 1 μA/μm. The saturation current (I_{ON}) is the drain current at V_{GS} = V_{DS} = 1.0 V. The leakage current (I_{OFF}) is the drain current at V_{GS} = 0.0 V and V_{DS} = 1.0 V. DIBL is the difference between the $V_{TH,lin}$ and the $V_{TH,sat}$. In order to adjust the V_{TH} and optimize the I_{ON}/I_{OFF}, the barrier of doped poly-Si (gate electrode) is chosen as 0.45 eV because this is the difference between the poly-Si extrinsic Fermi level and the Si intrinsic Fermi level [18].

Figure 2 shows the surface potential plots for both the bFDSOI and SOI MOSFETs with gate length of L_G = 30 nm. As shown in Figure 2, there is no significant change in the potential for bFDSOI-FETs as V_{DS} increases, although a slight change in the potential is observed. However, the FDSOI MOSFET (green line) still shows an increase due to the SCEs. This means that the thick FD scheme cannot effectively handle the issue of DIBL. These results confirm that the influence of drain bias upon the channel current has been reduced. As a consequence, the block-oxide-enclosed Si body helps suppress the SCEs, leading to an improved subthreshold swing and a decrease in I_{OFF}. Unfortunately, the V_{DS} appears to drop across the S/D regions rather than the channel regions, which leads to smaller effective V_{DS} which then drops across the channel region. This is not the ideal condition for a comparison of the properties of the intrinsic devices designed. The reason for this is that we have

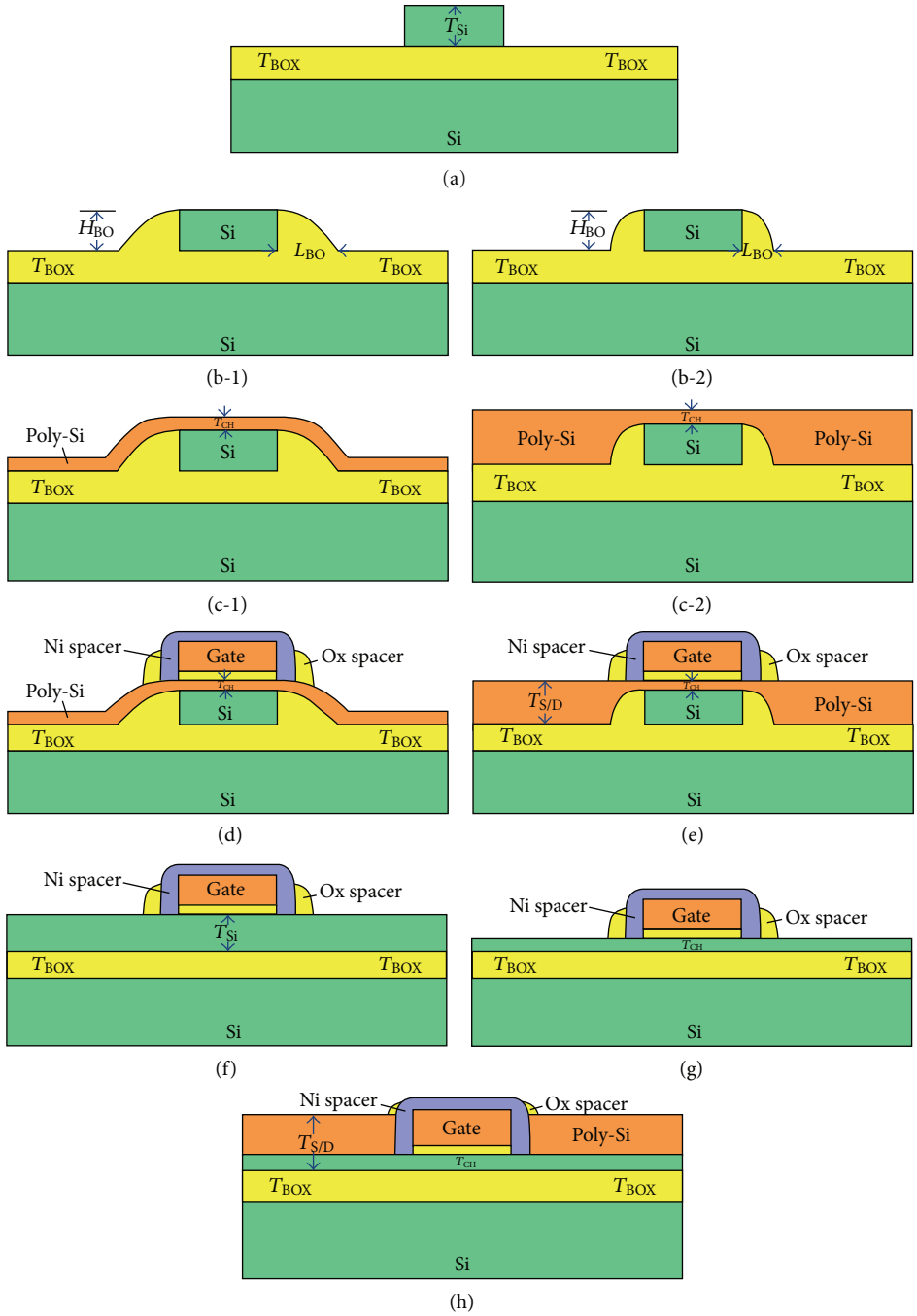

FIGURE 1: Schematic of the process flow of bFDSOI-FETs. (a) Si body patterning. (b-1) Block-oxide formation, where the height of the block-oxide (H_{BO}) is equal to the Si body thickness (T_{Si}) and the length of the block-oxide (L_{BO}) is 60 nm for thin S/D bFDSOI-FET. (b-2) Block-oxide formation, where the H_{BO} is equal to the T_{Si} and the L_{BO} is 15 nm for recessed S/D bFDSOI-FET. (c-1) Poly-Si deposition. (c-2) Poly-Si deposition, planarization, and deposition again. (d) A thin S/D bFDSOI-FET. (e) A recessed bFDSOI-FET. (f) An FDSOI-FET. (g) A UTBSOI-FET. (h) An E-S/D UTBSOI-FET. For thin S/D and recessed S/D bFDSOI-FETs, typical values of T_{Si} and poly-Si channel thickness (T_{CH}) are 30 nm and 5 nm, respectively. For FDSOI-FET, the typical value of T_{Si} is 30 nm. For UTBSOI-FET, the typical value of T_{Si} (= T_{CH}) is 5 nm. For E-S/D UTBSOI-FET, typical values of T_{Si} (= T_{CH}) and poly-Si raised S/D thickness are 5 nm and 30 nm, respectively. For other parameters, BOX thickness (T_{BOX}) and front-gate oxide thickness (T_{GOX}) are 50 nm and 1.4 nm, respectively.

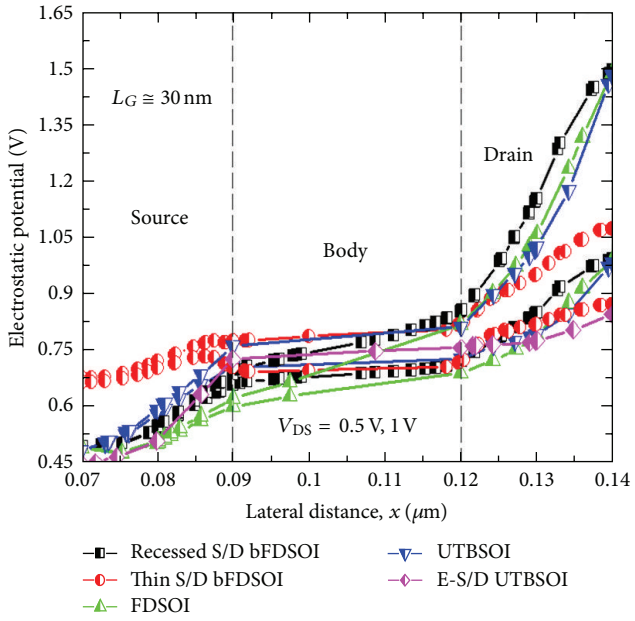

FIGURE 2: Simulated electrostatic potential (V) as a function of lateral distance along the FETs interface with gate length $L_G = 30$ nm.

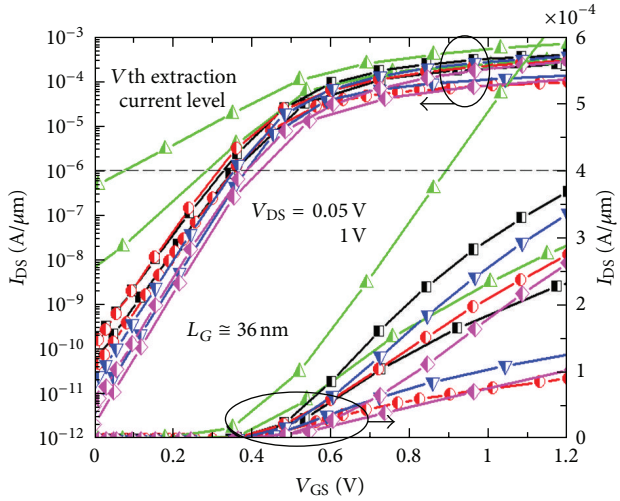

FIGURE 3: Comparison of bFDSOI and SOI MOSFETs I_{DS}-V_{GS} characteristics with gate length $L_G = 36$ nm. The symbols are the same as in Figure 2.

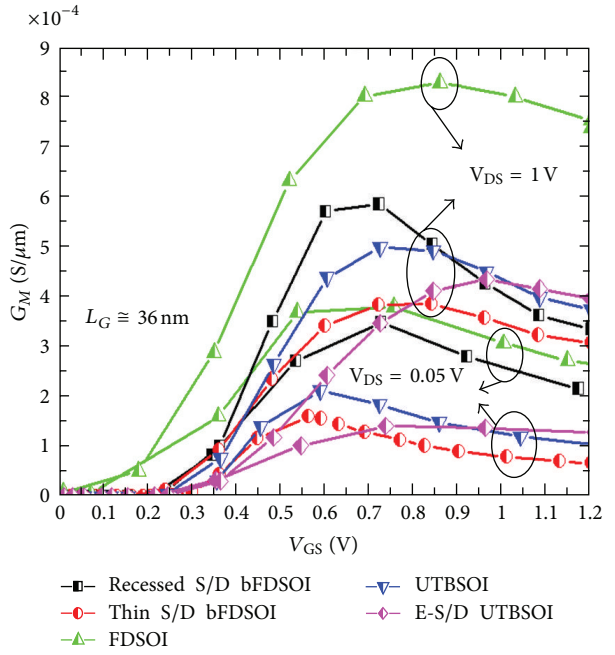

FIGURE 4: Comparison of bFDSOI and SOI MOSFETs G_M-V_{GS} characteristics with gate length $L_G = 36$ nm.

not optimized the S/D engineering in this study so that the characteristics are strongly dependent on the source/drain parasitic resistances. However, this study does predict the general trends for device scaling. Figure 3 shows the transfer characteristics of FETs with gate length $L_G = 36$ nm. Because of the block-oxide-enclosed Si body, bFDSOI-FETs show that DIBL is suppressed and subthreshold swing is improved. Furthermore, both thin S/D and recessed S/D bFDSOI-FETs show similar results compared to the UTBSOI-FET as well as the E-S/D UTBSOI-FET—additionally, those results are all better than those for the FDSOI-FET. In the UTBSOI-FET or E-S/D UTBSOI-FET, the subthreshold leakage current is the lowest among the transistors. Although FDSOI-FET shows the highest I_{ON} and transconductance ($G_{M,\,MAX}$ in Figure 4), it is very difficult to alleviate the SCEs in a thick body structure. For a given MOS device, transconductance is proportional to the square root of the drain-to-source current I_{DS} [19]. This suggests that thick S/D regions need to be introduced for an SOI to reduce series resistance. Yet a thick S/D structure alone cannot effectively reduce SCEs. Note that in Figure 5, the DIBL of bFDSOI-FETs is much smaller than that of the FDSOI-FET because the influence of drain bias on the channel current is reduced, as discussed earlier. Also, Figure 5 shows that as the gate length is reduced, the DIBL characteristics of the thin S/D bFDSOI-FET become slightly better than the recessed S/D bFDSOI-FET because the thin S/D structure possesses an effective method of suppressing SCEs. Nevertheless, either of the bFDSOI-FETs can alleviate the requirement of using an ultrathin channel to control SCEs in future nanodevices.

Figure 6 shows the I_{OFF} versus I_{ON} for the MOSFETs at different gate lengths. Thanks to its improved subthreshold swing, the bFDSOI-FETs show a lower I_{OFF} when compared with the FDSOI-FET. It should be noted that the FDSOI-FET shows the highest I_{ON} among transistors. As discussed earlier, thick S/D structure alone was unable to effectively reduce source and drain punch-through leakage, leading to the increase in I_{OFF}. On the one hand, UTBSOI-FET achieves the lowest I_{OFF}, mainly owing to the ultrathin S/D structure that suppresses punch-through and reduces the leakage current. This ultrathin S/D structure also allows the UTBSOI-FET to better control SCEs (see Figure 3), by reducing the effects of charge sharing. But the UTBSOI-FET has a poor I_{ON} because of the high series resistance caused by its ultrathin

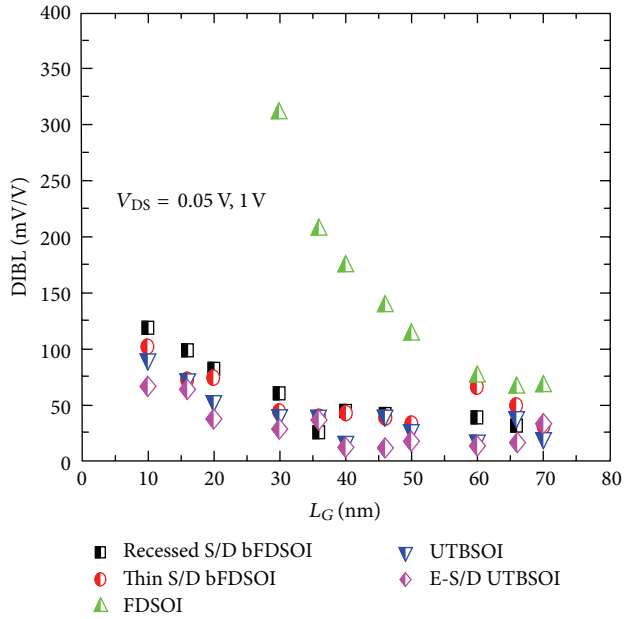

FIGURE 5: Simulated DIBL as a function of the gate length L_G for a low drain bias (V_{DS} = 0.05 V) and high drain bias (V_{DS} = 1.0 V). It is shown that the DIBL characteristics of the bFDSOI-FETs are better than those of the FDSOI-FET and similar to those of the UTBSOI-FET.

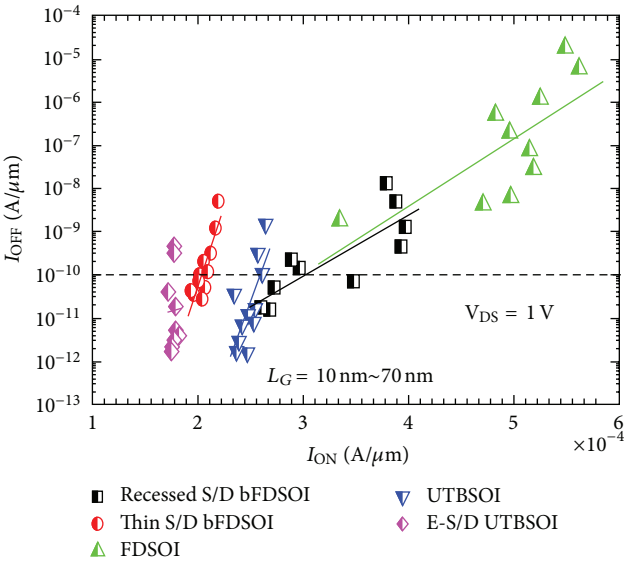

FIGURE 6: Simulated I_{OFF} versus I_{ON} for the MOSFETs at V_{DS} = 1.0 V. Mainly due to improved subthreshold swing, bFDSOI-FETs produce higher on/off current ratio than FDSOI-FET.

S/D regions. In the case of the E-S/D UTBSOI-FET, due to the nonoptimized S/D doping (because we use the same process conditions and parameters to fabricate all devices except those unique respective structures), this results in the longest channel length among all five transistors, and a poor I_{ON} is obtained. That is why the E-S/D UTBSOI-FET shows a better subthreshold swing and lower leakage current compared to

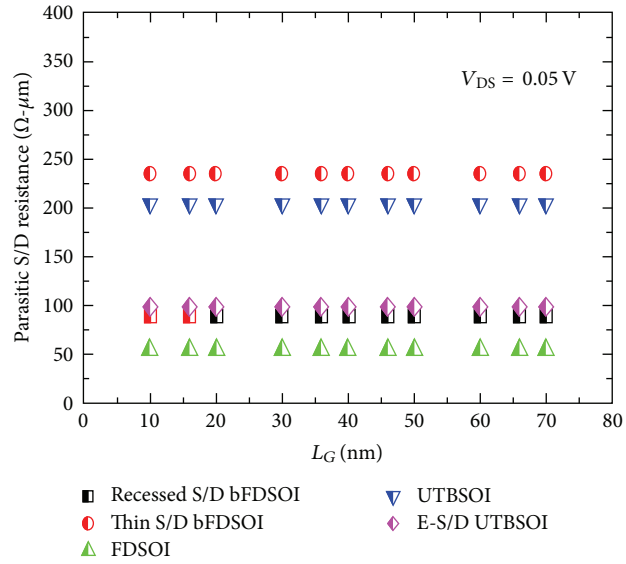

FIGURE 7: Simulated $R_{S/D}$ in different transistors for a low drain bias (V_{DS} = 0.05 V) and high gate bias (V_{GS} = 5.0 V). As shown in the figure, other than the thin S/D bFDSOI and UTSOI devices, devices show lower $R_{S/D}$ because of thick S/D regions.

the UTBSOI-FET as also shown in Figure 3 and smaller DIBL with decreasing gate length as shown in Figure 5. Therefore, the long channel leads to the small channel current and transconductance as shown in Figure 4. Both of the bFDSOI-FETs have similar results to the UTBSOI-FET. This is because the combined applications of a thick Si body and a block-oxide in a FDSOI MOSFET are used to minimize the effects of charge sharing.

Figure 7 shows the S/D series resistance ($R_{S/D}$) for the different transistors, which was extracted at V_{DS} = 0.05 V and V_{GS} = 5.0 V [20]. Compared with the thin S/D bFDSOI-FET and the UTBSOI-FET, both of the recessed S/D bFDSOI-FET and the FDSOI-FET have a very low $R_{S/D}$ because of their thick S/D regions. Furthermore, owing to the raised S/D scheme, the E-S/D UTBSOI-FET reveals a similar $R_{S/D}$ when compared to the recessed S/D bFDSOI-FET. We also consider that due to the recessed S/D scheme, the bFDSOI-FET can get a relatively lower $R_{S/D}$ than that of the E-S/D UTBSOI-FET. In other words, the junction depth that is different for both devices may be a reason why the $R_{S/D}$ of the recessed S/D bFDSOI-FET is relatively smaller. The low $R_{S/D}$ is desirable for SOI devices in high-performance applications, but ultrathin S/D regions have difficulty achieving a low $R_{S/D}$. Although the FDSOI-FET shows the lowest $R_{S/D}$ among the transistors, it is difficult to reduce DIBL and other SCEs. For the recessed S/D bFDSOI-FET, the combined applications of a thick S/D and a block-oxide are an effective way of reducing $R_{S/D}$ as well as DIBL. For the thin S/D bFDSOI-FET, it is difficult to reduce $R_{S/D}$ because of its thin S/D regions, but the thinness of these regions makes it easy to reduce DIBL. On the other hand, the E-S/D UTBSOI-FET also exhibits a smaller $R_{S/D}$ compared to the UTBSOI-FET; however, the Miller capacitance is one of the most important issues for high-frequency applications.

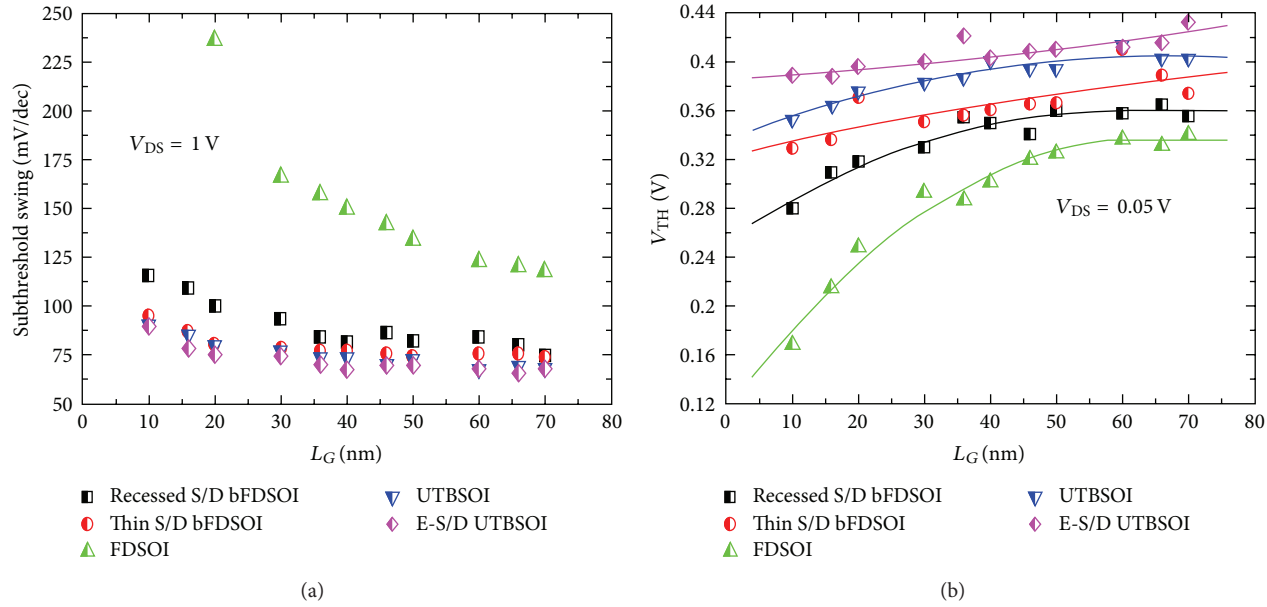

FIGURE 8: Simulated (a) subthreshold swing and (b) V_{TH} dependence on the gate length L_G. The bFDSOI-FETs show improved subthreshold swing and better V_{TH} rolloff than FDSOI-FET, similar to the UTBSOI-FET.

The subthreshold swing and V_{TH} of MOSFETs, as a function of the gate length, are presented in Figure 8. Because of the good gate controllability over the active channel, the bFDSOI-FET has an improved subthreshold swing and a better V_{TH} rolloff when compared with the FDSOI-FET. According to recent trends, SOI FETs limit the device performance itself since a uniform film thickness below 10 nm is needed for improving the subthreshold swing [21, 22]. In brief, SOI devices need to conform to the rule that $T_{Si} \leq L_G/4$ [23]. The use of a block-oxide in FDSOI design can alleviate the requirement for a uniform ultrathin Si film, thereby making the characteristics of the bFDSOI-FETs like those of the UTBSOI-FET with or without an E-S/D scheme, even though the total body thickness (including the single crystal Si body and the poly-Si film deposited afterward) is 35 nm in the bFDSOI-FETs.

One of the key issues associated with SOI-based transistors is self-heating effects (SHEs), because the reliability of SOI devices is severely affected by thermal instability. To investigate the influence of SHEs on the device structures, various gate-to-source overdrive voltages (V_{GT}) are applied to the devices. With V_{GT} = 1.0 V, thin S/D bFDSOI-FET still shows good behavior in suppressing SHEs. However, FDSOI, UTBSOI, and E-S/D UTBSOI devices, in contrast, suffer from serious thermal effects because the self-heating-induced negative differential conductance (NDC) is observed in the output curves, as shown in Figure 9. The authors also found that the 35 nm thick body bFDSOI structures can help transistors to endure more heat generated in the channel. Although the body of the FDSOI is thicker than that of the UTBSOI, a higher drain current also results in more heat energy and eventually leads to a reduction of the drain current I_{DS} when the FDSOI enters into the saturation region. For the recessed bFDSOI-FET, due to the higher drain

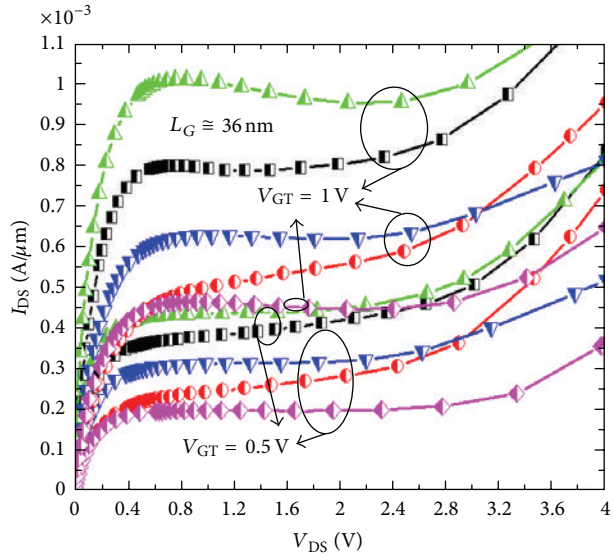

FIGURE 9: Comparison of bFDSOI and SOI MOSFETs I_{DS}-V_{DS} characteristics with gate length L_G = 36 nm. The symbols are the same as in Figure 2.

current compared to that of the thin S/D bFDSOI-FET, the self-heating-induced NDC is also observed in the output curves. However, the recessed S/D bFDSOI-FET still provides better self-heating immunity than SOI devices owing to its thick body scheme. Additionally, due to the lower current in the bFDSOI device than in the UTBSOI, self-heating is not dominant. If the drain current is high enough, self-heating is still a significant problem for the bFDSOI-FETs, as it is in UTBSOI devices. Nevertheless, owing to the thick body and the block-oxide schemes, requiring a uniform UTB

structure for suppression of SCEs can be excluded. This relaxes the technology requirement in a UTB application. In addition, the power supply voltage will eventually decrease in order to reduce the power consumption in the IC circuits. Therefore, the thermal instability in the bFDSOI-FETs can be diminished via a choice of low power supply (i.e., $V_{cc} < 1.0$ V).

In the case of low drain bias, self-heating is not significant; hence the NDC is not obviously observed in the output characteristics. The better control of SCEs the transistor has, the higher output resistance (r_o) the transistor possesses. That is why the UTBSOI with or without an E-S/D structure can produce a higher r_o compared to the FDSOI, with or without a block-oxide scheme. In addition, because large drain current results in large G_M, both FDSOI and recessed bFDSOI devices show a larger G_M than those of other transistors. In order to compare the incremental voltage gain ($A_V = G_M/G_D = G_M r_o$), it is believed that the UTSOI with or without E-S/D devices can produce a higher voltage gain as compared to the FDSOI with or without block-oxide scheme, despite the fact that their G_M is lower. It is because the poor short-channel behavior leads to a small r_o observed in output curves for the FDSOI with or without the block-oxide scheme. If the self-heating is dominant, it is not a fair comparison chiefly owing to the NDC phenomenon that results in negative r_o.

Figure 10 shows the electron temperature along the MOSFETs' channel surface with gate length $L_G = 36$ nm. For bFDSOI-FETs, the thermal stability can be improved with the addition of a thick body, which results in a lower electron temperature in the channel. Although an ultrathin S/D structure alone shows excellent subthreshold characteristics, SHEs will become a severe problem for SOI-based transistors in particular, as SHEs would likely block the use of SOI MOSFETs in high-performance CMOS applications. It is worthwhile noting that a high-temperature electron possessing high transportation, rotation, and vibration energy will result in the increased probability of phonon scattering and surface scattering, thereby increasing thermal resistance and aggravating self-heating. In contrast to both of these SOI-based transistors, bFDSOI-FETs can alleviate the requirement of uniform ultrathin films to control SCEs, thereby leading to high device reliability. As a result, the thermally induced vibrations of the atoms in the bFDSOI-FETs are ameliorated by its thick body. The body thickness of the FDSOI is thicker than that of the UTBSOI, but a higher I_{DS} also results in more heat energy and eventually leads to a serious reduction of the carrier mobility.

The simulation results in this paper suggest that a metal-gate material and a high-k dielectric should be introduced into the bFDSOI-FET devices. The use of a metal gate would allow the V_{TH} to be optimized even for a lightly doped ultrathin body. In addition, the metal gate, when used with a high-k dielectric, would allow the I_{ON}/I_{OFF} ratio to be improved [24, 25]. This is because the work function of the metal gate can help transistors to adjust the V_{TH} while the high-k dielectric can also relax the requirement of ultrathin gate oxide to reduce the gate-tunneling leakage current.

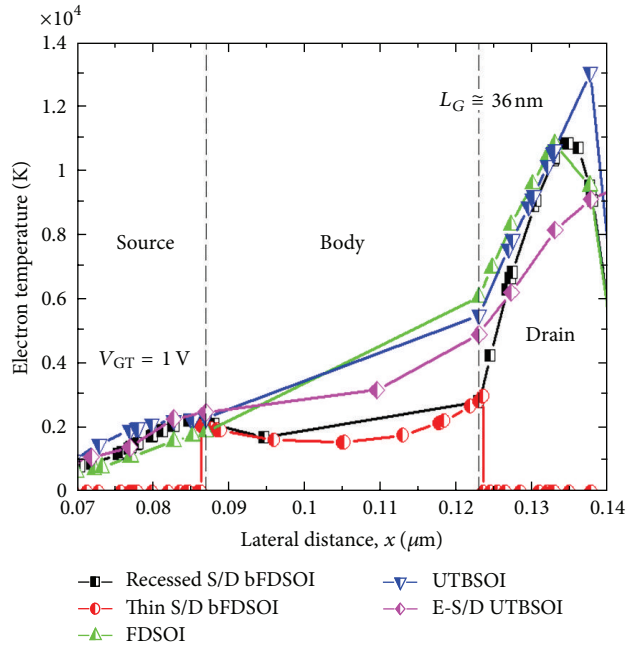

Figure 10: Simulated lateral electron temperature (K) as a function of lateral distance along the MOSFETs channel surface with gate length $L_G = 36$ nm.

Two important issues caused by the bFDSOI-FETs are addressed here: (1) the quality of poly-Si and (2) the non-self-aligned process. In the bFDSOI-FETs, the Si film used in this study for comparison is the same as that used in the FD and UTB SOI devices. The mobility of bFDSOI-FETs is actually affected by the poly-Si film. Although the lattice scattering caused by phonons in the bFDSOI-FETs can be reduced by its thick body, the poor quality of poly-Si also results in reduced mobility. Some methods of improving the quality of poly-Si are now described. In general, after making S/D regions by ion implantation, it is believed that poly-Si can be recrystallized because the poly-Si is directly connected to the single crystal Si body. Moreover, advanced recrystallization techniques can also be applied to the bFDSOI process to improve the quality of the poly-Si. Another key issue is the non-self-aligned process used in bFDSOI-FETs. In fact, self-aligned technology is not applicable in the bFDSOI-FETs presented. The misalignment problem will limit the bFDSOI-FETs' performance. All of these issues, including the quality of poly-Si channel and the self-alignment of bFDSOI-FETs, will be addressed in our future research work.

4. Conclusion

In this paper a new planar FDSOI MOSFET with block-oxide has been presented and analyzed. The bFDSOI-FET is equipped with a block-oxide on the sidewall of Si body that helps improve the control of SCEs without requiring a uniform UTBSOI structure. As indicated by the two-dimensional (2D) simulation results, the authors found that

the characteristics of the bFDSOI-FETs (a reduced DIBL, a higher on/off current ratio, an improved subthreshold swing, and a better V_{TH} rolloff behavior as compared with the FDSOI-FET) are similar to the UTBSOI-FET, because the block-oxide-enclosed Si body helps to diminish the influence of V_{DS} upon the channel current, resulting in desirable device characteristics. Although the short-channel properties of bFDSOI-FETs are somewhat worse than those of UTBSOI-FETs, the results are acceptable. Moreover, both types of bFDSOI-FETs also exhibit significantly lower channel temperature due to their thick bodies. It should be noted that this thick body, including the single crystal Si body and the poly-Si film deposited afterwards, are used to tolerate much of the heat being generated in the channel when compared with the UTBSOI-FET. As a result, the thermal stability of the bFDSOI-FETs can be improved by reducing the scattering of lattice atoms. Compared with the UTBSOI-FET, a thickness requirement of below 10 nm and uniform ultrathin film are excluded for the bFDSOI-FETs to diminish the charge-sharing effect without increasing self-heating. The bFDSOI-FETs are therefore found to improve the reliability of SOI CMOS devices and somewhat relax the critical technology requirement for potential applications.

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Research Article

Comprehension of Postmetallization Annealed MOCVD-TiO_2 on $(NH_4)_2S$ Treated III-V Semiconductors

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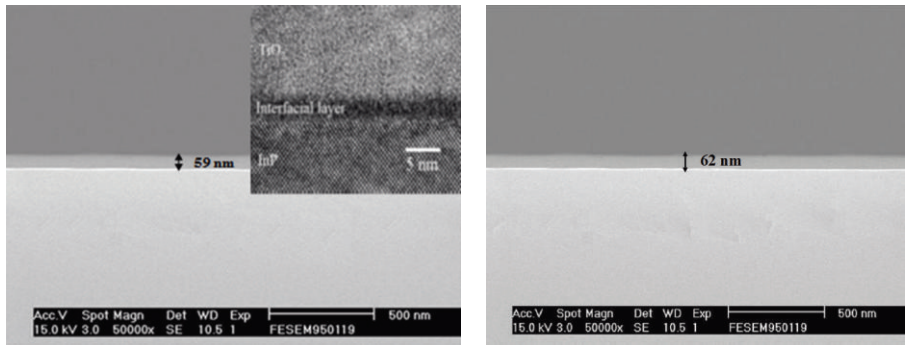
The electrical characteristics of TiO_2 films grown on III-V semiconductors (e.g., p-type InP and GaAs) by metal-organic chemical vapor deposition were studied. With $(NH_4)_2S$ treatment, the electrical characteristics of MOS capacitors are improved due to the reduction of native oxides. The electrical characteristics can be further improved by the postmetallization annealing, which causes hydrogen atomic ion to passivate defects and the grain boundary of polycrystalline TiO_2 films. For postmetallization annealed TiO_2 on $(NH_4)_2S$ treated InP MOS, the leakage current densities can reach 2.7×10^{-7} and 2.3×10^{-7} A/cm^2 at ± 1 MV/cm, respectively. The dielectric constant and effective oxide charges are 46 and 1.96×10^{12} C/cm^2, respectively. The interface state density is 7.13×10^{11} cm^{-2} eV^{-1} at the energy of 0.67 eV from the edge of valence band. For postmetallization annealed TiO_2 on $(NH_4)_2S$ treated GaAs MOS, The leakage current densities can reach 9.7×10^{-8} and 1.4×10^{-7} at ± 1 MV/cm, respectively. The dielectric constant and effective oxide charges are 66 and 1.86×10^{12} C/cm^2, respectively. The interface state density is 5.96×10^{11} cm^{-2} eV^{-1} at the energy of 0.7 eV from the edge of valence band.

1. Introduction

Due to its high electron mobility and direct energy band gap compared with Si, much attention has been focused on III-V compound semiconductor (e.g., InP and GaAs) high-speed devices. Usually, the metal-semiconductor field-effect transistor (MESFET) is one of III-V main high-speed devices due to the lack of high quality of oxide on it. The main disadvantage of MESFET is the high gate currents of Schottky contact under the positive bias of several tenths of a volt, which severely limits the maximum drain currents, the lower noise margin, and the less flexibility of the circuit design. Metal-oxide-semiconductor field-effect transistor (MOSFET) can alleviate these problems. Many high-k dielectrics, such as Al_2O_3 [1], TiO_2 [2], Ga_2O_3 [3], HfAlO [4], and HfO_2 [5], are currently being explored on III-V substrates. For high-k dielectrics, the same gate capacitance per unit area can be realized using a much thicker gate materials and results in less tunneling leakage current. Of various high-k materials, TiO_2 has generated much interest as it offers a large dielectric constant (k value 4–86) [6] and a higher transconductance of MOSFET is expected [7].

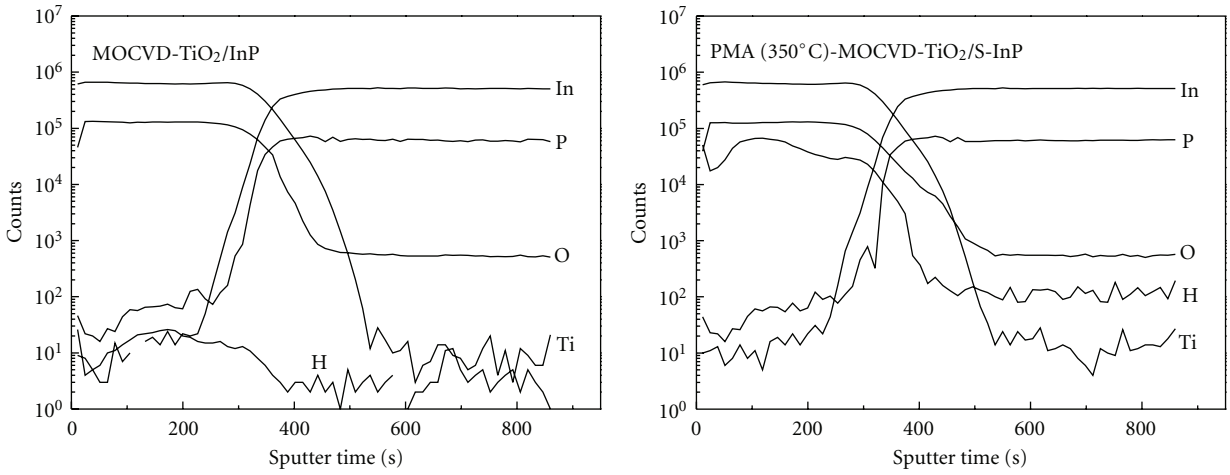
High dielectric constant polycrystalline TiO_2 films were prepared by metal-organic chemical vapor deposition (MOCVD) [8], sol-gel [9], and sputtering [10]. MOCVD-TiO_2 was used in this study because of its simple process and higher quality. Usually, the leakage current of MOCVD-TiO_2 on III-V is high from the high interface state (D_{it}) [11, 12] and the polycrystalline grain boundary [13, 14]. From previous studies [13, 14], the high D_{it} from native oxides on III-V surface can be removed by $(NH_4)_2S$ treatment. It can also passivate the surface dangling bonds of III-V surface and prevent it from oxidizing.

The low temperature postmetallization annealing (PMA) is an effective process to reduce the oxide charge density and the D_{it} in SiO_2/Si metal-oxide-semiconductor (MOS) technology [15, 16]. The mechanism of PMA process is from the reaction between the aluminum contact and hydroxyl groups existed on SiO_2 films surface resulting in hydrogen atomic ions diffusing through the oxide and passivate the



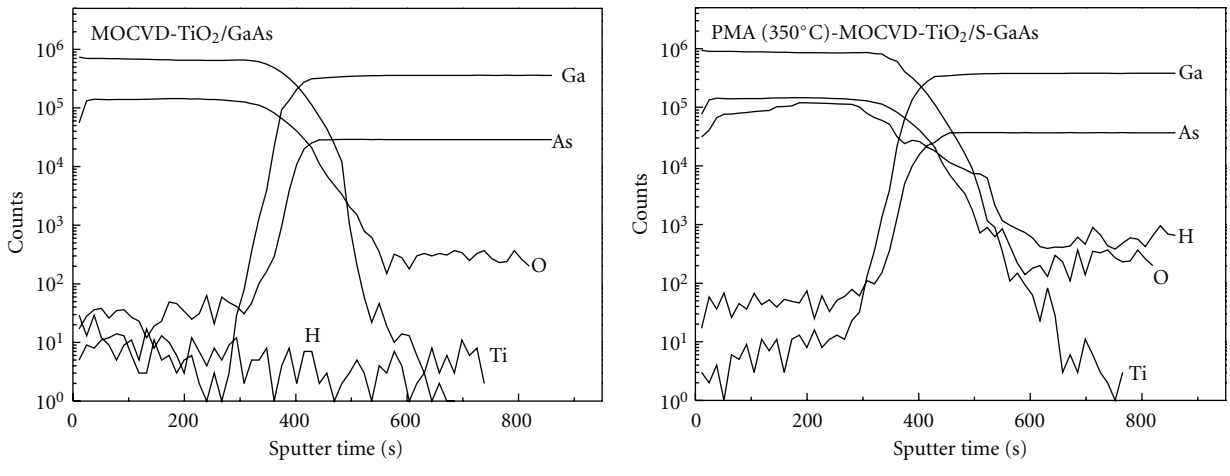
(a) (b)

Figure 1: (a) Images of SEM and HRTEM of TiO_2/S-InP and (b) SEM cross section of TiO_2/S-GaAs substrate.



(a) (b)

Figure 2: SIMS depth profiles for (a) TiO_2/S-InP and (b) PMA (350°C)-TiO_2/S-InP.



(a) (b)

Figure 3: SIMS depth profiles for (a) TiO_2/S-GaAs and (b) PMA (350°C)-TiO_2/S-GaAs.

Table 1: Electrical characteristics by PMA(350°C)-TiO_2/InP and PMA(350°C)-TiO_2/GaAs.

MOS structures	Dielectric constant	Leakage current at 1 MV/cm	Interface state density	ΔV_{FB} of hysteresis loop
PMA(350°C)-TiO_2/S-InP	44	2.7×10^{-7} and 2.3×10^{-7} A/cm^2	7.13×10^{11} cm^{-2} eV^{-1}	17 mV
PMA(350°C)-TiO_2/S-GaAs	66	9.7×10^{-8} and 1.4×10^{-7}	5.96×10^{11} cm^{-2} eV^{-1}	9 mV

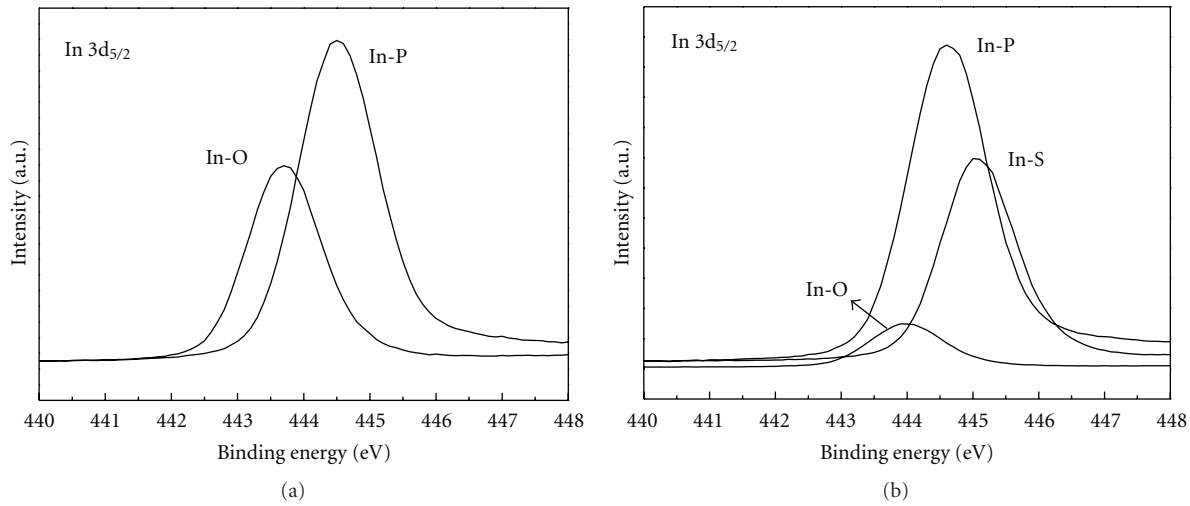


Figure 4: XPS spectra of In $3d_{5/2}$ core level from (a) InP without $(NH_4)_2S$ treatment and (b) InP with $(NH_4)_2S$ treatment.

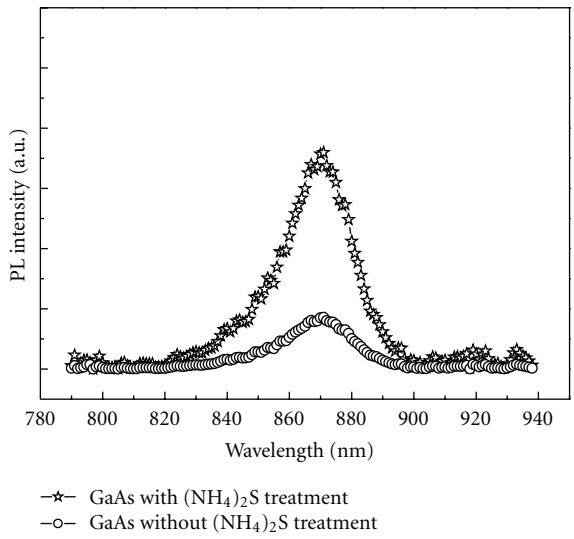


Figure 5: PL spectra of GaAs with and without $(NH_4)_2S$ treatment.

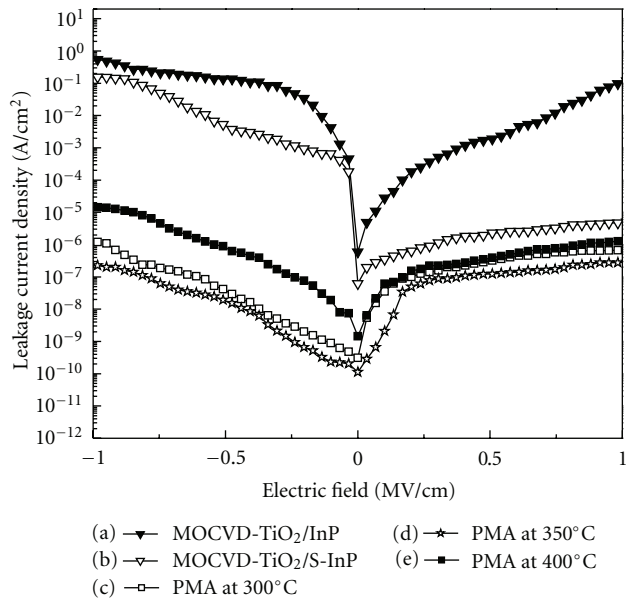


Figure 6: Leakage current densities of TiO_2/InP with and without $(NH_4)_2S$ treatments and PMA-TiO_2/S-InP at different PMA temperatures.

oxide traps [15–17]. From our previous study [18], the PMA was used to reduce the leakage current from the defects and grain boundary of polycrystalline TiO_2 films grown on silicon. Both treatments also show the same function on high-*k*/III-V. In this study, we try to review the improvement of electrical characteristics of TiO_2/InP and TiO_2/GaAs by the combination of $(NH_4)_2S$ and PMA treatments (PMA-TiO_2/S-InP (GaAs)).

2. Experimental

Zn doped p-type (100) InP and GaAs with carrier concentration of 5×10^{16} and 6×10^{16} cm^{-3} were used as the substrates. These substrates were degreased in solvent and followed by chemical etching in a solution ($H_2SO_4 : H_2O_2 : H_2O$ = 5 : 1 : 1) for 3 min and then rinsed in deionized water.

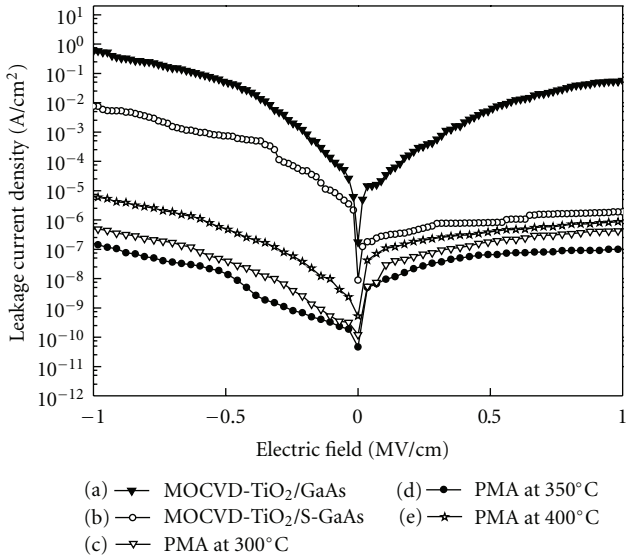


FIGURE 7: Leakage current densities of TiO_2/GaAs with and without $(NH_4)_2S$ treatments and without $(NH_4)_2S$ treatment and PMA-TiO_2/S- GaAs at different PMA tempreatures.

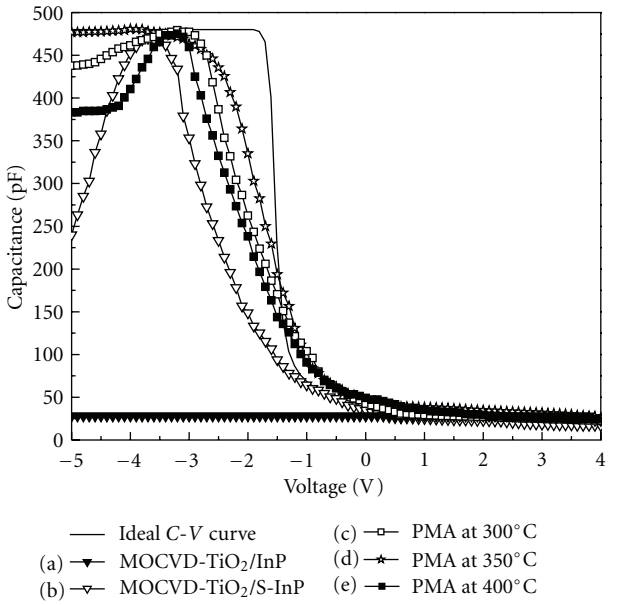


FIGURE 8: *C-V* characteristics of TiO_2/InP with and without $(NH_4)_2S$ treatments and PMA-TiO_2/S-InP at different PMA temperatures.

After cleaning, substrates were immediately dipped into $(NH_4)_2S$ solution for 40 min at 50°C and then blow-dried with nitrogen gas. After $(NH_4)_2S$ treatment, substrates were thermally treated at 220°C in a nitrogen atmosphere for 10 min in order to desorb the excess of weakly bonded sulfur and were ready for MOCVD-TiO_2 growth.

Polycrystalline TiO_2 thin films were grown on substrates by a horizontal cold-wall MOCVD system. Tetraisopropoxytitanium ($Ti(i\text{-}OC_3H_7)_4$) was used as a Ti precursor and kept at 24°C. Nitrogen was used as the carrier gas and its flow rate was 10 sccm. Nitrous oxide gas (N_2O) was used as an oxidizing agent and its flow rate was 100 sccm. Molybdenum was used as the oxidation-resist susceptor. The reactor pressure was kept at 5 Torr during the growth. The growth temperature was kept at 400°C for 5 min. The chemical reaction steps during the deposition of TiO_2 on substrate in MOCVD system are as follows.

In PMA procedure, aluminum (Al) was deposited upon the TiO_2 films as the cap layer. Then, these films were annealed in nitrogen ambient for 10 min at the temperature of 300, 350, and 400°C, respectively. Finally, the Al was etched away with an etching solution ($H_3PO_4 : HNO_3 : CH_3COOH : H_2O = 73 : 4 : 3.5 : 19.5$).

A metal-oxide-semiconductor (MOS) structure was used to examine the electrical characteristics. In-Zn alloy (In 90% and Zn 10%) was evaporated on the III-V back side for ohmic contact and then thermally annealed at 400°C for 3 min in nitrogen atmosphere. The ohmic contact was confirmed by the current-voltage characteristics. Then, Al was evaporated on TiO_2 films as the top contact with the area of 7.07×10^{-4} cm^2. Scanning electron microscopy (SEM) was used to examine the thickness of TiO_2 film. A HP4145B semiconductor-parameter analyzer was used for current-voltage (*I-V*) characterization. A high frequency (1 MHz) HP4280A capacitance-voltage (*C-V*) meter was used for *C-V* characterization scanned from accumulation region to inversion region. The DC bias was swept by 1/30 V/sec. The D_{it} was derived from *C-V* curves by Terman method [19], which can provide a good evaluation [20] of the D_{it} higher than 10^{10} cm^{-2} eV^{-1} with 10% error [21, 22].

3. Results and Discussion

The SEM cross section of TiO_2/S-InP is shown in Figure 1(a) and the thickness of TiO_2 film is 59 nm. The SEM picture shows that there is an interfacial layer. From the image of high-resolution transmission electron microscopy (HRTEM) shown in the inset in Figure 1(a), the interfacial layer is 2.5 nm. It is from the interdiffusion between TiO_2 and InP examined by SIMS depth profile shown in Figure 2(a). The SEM cross section of TiO_2/S-GaAs is shown in Figure 1(b) and the thickness of TiO_2 film is 62 nm. The SEM picture also shows an interfacial layer. The mechanism is the same as TiO_2/S-InP and examined by the SIMS depth profile shown in Figure 3(a). It indicates that a low temperature growth process is essential for decreasing the interfacial layer for ultrathin TiO_2 film. Atomic layer deposition (ALD) may be the candidate.

The X-ray photoelectron spectroscopy (XPS) core level spectra of In $3d_{5/2}$ of InP without and with $(NH_4)_2S$ treatments are shown in Figures 4(a) and 4(b), respectively. For InP without $(NH_4)_2S$ treatment, the strong In $3d_{5/2}$ XPS peak at 444.7 eV can be attributed to In-P bond [23] and the peak at 443.7 eV is from In-O bond [24]. For InP with $(NH_4)_2S$ treatment, a new strong peak at 444.9 eV [25] and a small satellite peak at 443.9 eV are from In-S and In-O, respectively. The strong In-S bond shows that In empty dangling bond is passivated by S. The much weaker

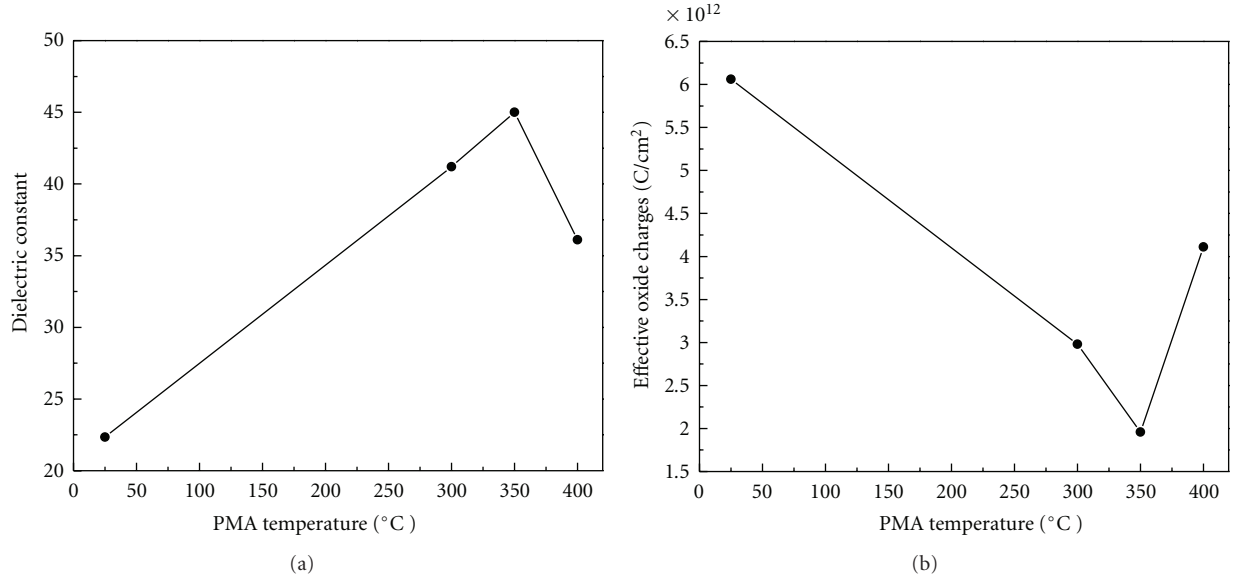


FIGURE 9: (a) Dielectric constant and (b) effective oxide charges of TiO_2/S-InP and PMA-TiO_2/S-InP at different PMA temperatures.

In-O peak indicates that native oxides are significantly reduced after $(NH_4)_2S$ treatment. It suggests the $(NH_4)_2S$ treatment can not completely remove native oxides on III-V semiconductors. It needs a further investigation.

In order to double check the function of $(NH_4)_2S$ passivation, the photoluminescence (PL) spectra of GaAs and S-GaAs are shown in the inset of Figure 5. The lower PL intensity for GaAs without $(NH_4)_2S$ treatment shows a high surface recombination velocity [26, 27]. The PL intensity is much improved for GaAs with $(NH_4)_2S$ treatment. It indicates that the $(NH_4)_2S$ passivation is an effective way to reduce the surface recombination velocity [28]. It supports that $(NH_4)_2S$ treatment can remove native oxides and prevent III-V surface from oxidizing.

The leakage current densities of TiO_2 film deposited on InP substrate with and without $(NH_4)_2S$ treatments are shown in Figure 6. It also shows the leakage current densities of PMA-TiO_2/S-InP treated at the PMA temperatures of 300, 350, and 400°C. The leakage current densities of TiO_2/InP are 0.1 and 0.57 A/cm^2 at ±1 MV/cm as shown in Figure 6(a). The high leakage currents are mainly from the high density of defects in the grain boundary of polycrystalline TiO_2 film [11, 12] and the high interface states at TiO_2/InP interface due to InP native oxide [13, 14]. For TiO_2/S-InP as shown in Figure 6(b), the leakage current densities are 4.56×10^{-6} and 0.16 A/cm^2 at ±1 MV/cm, respectively. The leakage currents are mainly from D_{it} and grain boundary of TiO_2 film. After $(NH_4)_2S$ treatment, higher quality TiO_2 film can be deposited on reconstructed InP surface [14]. The leakage current is much improved under positive bias from the reduction of D_{it}. However, only one order improvement of the leakage current under negative bias is from grain boundary.

The leakage current density can be further improved by PMA treatment as shown in Figures 6(c)–6(e). The lowest leakage current densities of PMA-TiO_2/S-InP can reach 2.7×10^{-7} and 2.3×10^{-7} A/cm^2 at ±1 MV/cm at the PMA treatment of 350°C as shown in Figure 6(d). After PMA process, the thickness of the interfacial layer does not change and is examined from SIMS depth profiles as shown in Figures 2(a) and 2(b). Therefore, the improvement of leakage current is not from the increase of interfacial layer thickness after PMA. Figure 2(b) shows that H atoms are uniformly distributed in the whole TiO_2 film due to H fast diffusion after PMA treatment. It would diffuse along and passivate the grain boundary. At the PMA treatment of 300°C, the leakage current densities are 6.58×10^{-7} and 1.2×10^{-6} A/cm^2 at ±1 MV/cm as shown in Figure 6(c). The slight increase of leakage current compared with Figure 6(d) could be from the lower PMA temperature, which cannot provide sufficient energy for H atoms for passivation. For the PMA temperature at 400°C as shown in Figure 6(e), the leakage currents are higher than that of 300 and 350°C. It is that the higher PMA temperature would destroy the H passivation and is examined by C-V characteristics.

For TiO_2 on GaAs substrate with and without $(NH_4)_2S$ treatments, the leakage current densities are shown in Figure 7. It also exhibits the leakage current densities of PMA-TiO_2/S-GaAs treated at the PMA temperatures of 300, 350, and 400°C. The leakage current densities of TiO_2/GaAs without $(NH_4)_2S$ treatment are 5×10^{-2} and 5.9×10^{-1} A/cm^2 at ±1 MV/cm as shown in Figure 7(a). For TiO_2/S-GaAs as shown in Figure 7(b), the leakage current densities are 2.1×10^{-6} and 6×10^{-3} A/cm^2 at ±1 MV/cm, respectively. The leakage current density can be further improved by PMA treatment as shown in Figures 7(c)–7(e). The leakage current densities are 4.5×10^{-7} and 4.9×10^{-7}A/cm^2 at ±1 MV/cm at the PMA treatment of 300°C as shown in Figure 7(c). The lowest leakage current densities of PMA-TiO_2/S-GaAs can reach 9.7×10^{-8} and 1.4×10^{-7} A/cm^2 at ±1 MV/cm at the PMA treatment of 350°C as shown in Figure 7(d). For the PMA temperature at 400°C,

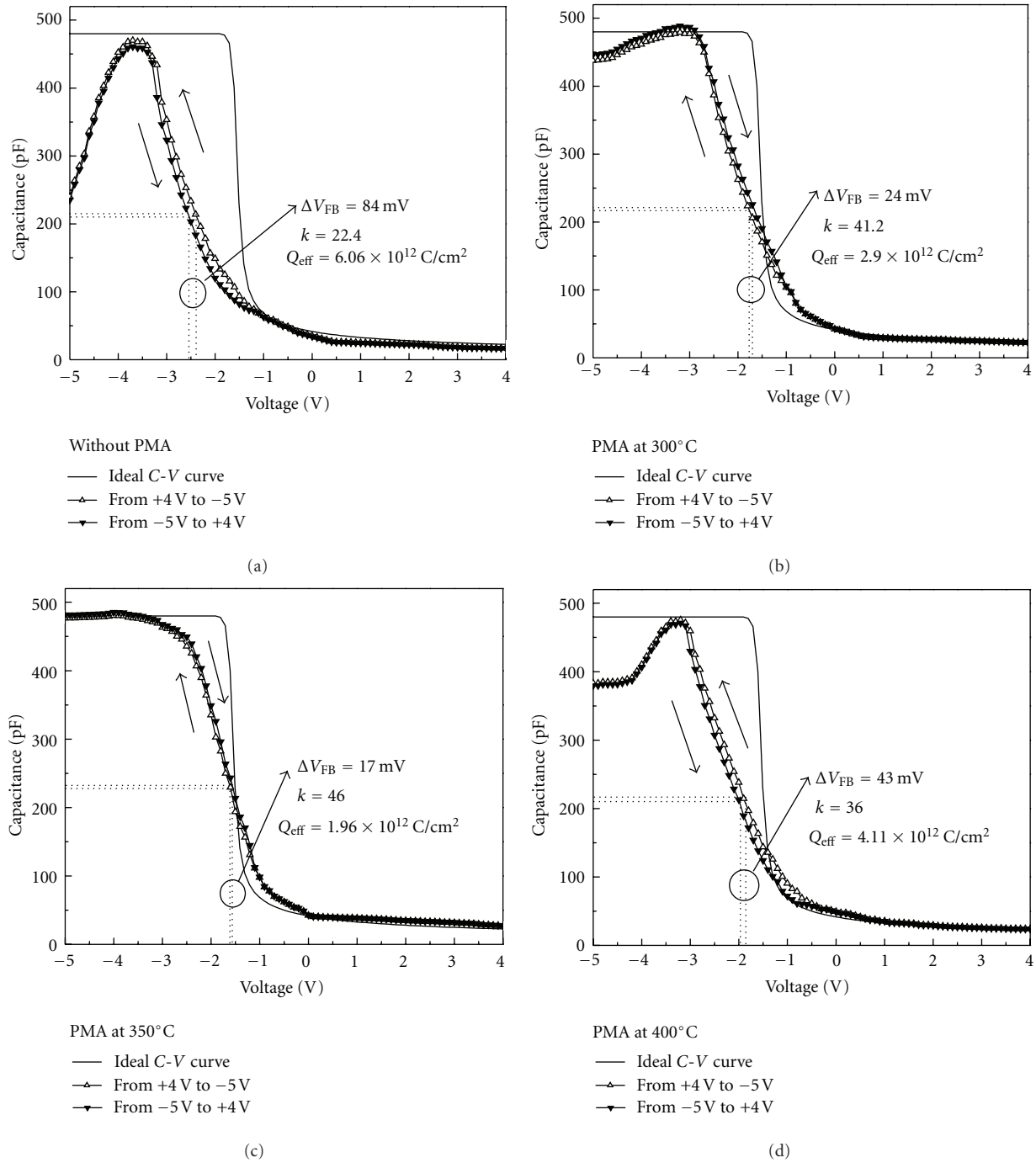


FIGURE 10: C-V hysteresis loops of (a) TiO_2/S-InP, (b) PMA at 300°C, (c) PMA at 350°C, and (d) PMA at 400°C.

the leakage currents are 9.5 $\times 10^{-7}$ and 6 $\times 10^{-6}$A/cm^2 at ±1 MV/cm as shown in Figure 3(e), which are higher than that of 300 and 350°C. The mechanisms are similar to InP as mentioned in the previous paragraph.

The C-V characteristics of TiO_2/InP, TiO_2/S-InP, and PMA-TiO_2/S-InP are shown in Figure 8. The C-V characteristics of TiO_2/InP show a flat curve as in Figure 8(a). It is from the high density of interface states due to the existence of native oxides on InP surface, which causes the pinning of the surface Fermi level near the middle of the band gap [29]. Figure 8(b) shows the C-V characteristics of TiO_2/S-InP. The capacitance in the accumulation region is high due to the improved interface quality. The capacitance decay at higher negative bias is due to the high leakage current, which comes from the defects and the grain boundary of polycrystalline TiO_2 film. Sharp C-V curves PMA-TiO_2/S-InP can be obtained after PMA treatments at 300, 350, and 400°C as shown in Figures 8(c)–8(e), respectively. The ideal

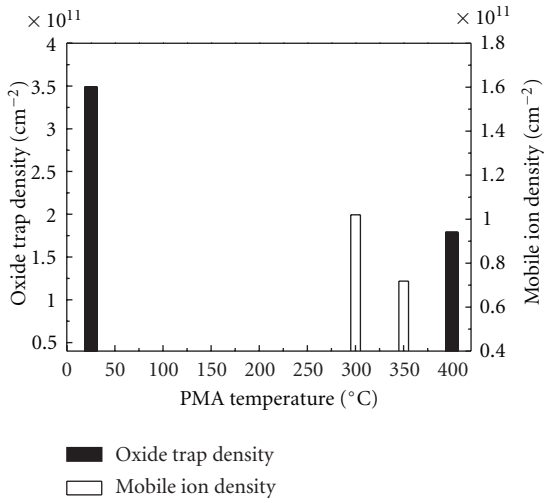


FIGURE 11: Oxide trap density and mobile ion density of TiO_2/S-InP MOS structures as a function of PMA temperature.

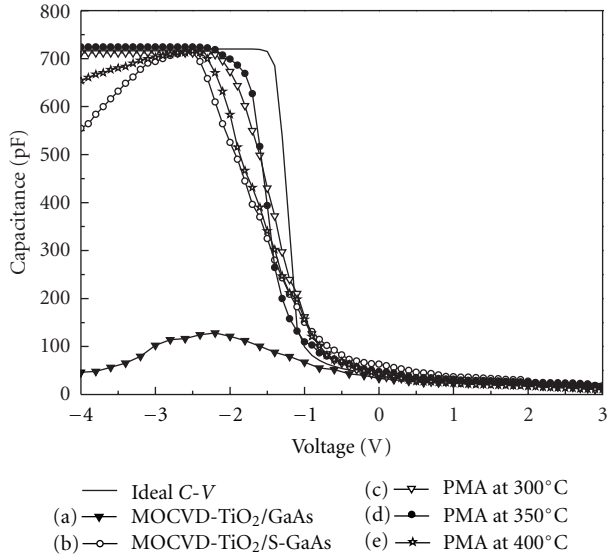


FIGURE 12: C-V characteristics of TiO_2/GaAs with and without $(NH_4)_2S$ treatments and PMA-TiO_2/S-GaAs at different PMA temperatures.

C-V curve is also shown in the figure as a reference. It is derived from the neglect of the effective oxide charges and the interface states, but the work function difference ($\Phi_{ms} = -1.51$ V) of metal (Al) and semiconductor (InP) is taken into account. The optimized PMA temperature is 350°C as shown in Figure 8(d), in which the stretch-out phenomenon and the flat-band voltage shift are minimized. The dielectric constants and effective oxide charges of PMA-TiO_2/S-InP films as functions of PMA temperature are shown in Figures 9(a) and 9(b), respectively. The dielectric constant increases with the PMA temperature due to the improvements of interface and film qualities. But the value decreases at PMA temperature high than 350°C. The higher PMA temperature will break the H bonds and lose the passivation function [30, 31] and results in the increase of leakage current as shown in Figure 6. The dielectric constant and the effective oxide charges can reach 46 and 1.96 $\times 10^{12}$ C/cm^2 at the PMA temperature of 350°C. The thickness of TiO_2 film is 59 nm. The interfacial layer is very thin, which has minor effect during the extraction of dielectric constants.

Moreover, the C-V hysteresis loops as a function of PMA temperature are shown in Figure 10. The C-V hysteresis loop of TiO_2/S-InP without PMA treatment is counterclockwise as shown in Figure 10(a), which is from high density of oxide trapped charges [18, 20] in TiO_2/S-InP film without H passivation. The C-V hysteresis loops of PMA-TiO_2/S-InP film are clockwise at 300 and 350°C as shown in Figures 10(b) and 10(c). The mobile ions are responsible for the C-V clockwise hysteresis loop due to the decrease of oxide trapped charges from film quality improvement. The C-V hysteresis loop changes back to counterclockwise at 400°C as shown in Figure 10(d). It is dominated by oxide trapped charges due to the break of H bonds and hence the loss of the passivation function at higher PMA temperature [30, 31]. The sum (N_{ot}) of oxide trapped density and mobile ion density can be derived from the difference of flat-band voltage (ΔV_{FB}) of the C-V hysteresis loops measured at high frequency [20]. The formula is as follows:

$$N_{ot} = \frac{-\Delta V_{FB} C_{ox}}{Aq}, \quad (1)$$

where C_{ox} is the oxide capacitance, A is the contact area (7.07×10^{-4} cm^{-2}), and q is magnitude of an electron charge. In C-V measurement, the bias scans first from accumulation region to inversion region (forward scan) and then back to accumulation region (backward scan). ΔV_{FB} is defined as the difference of V_{FB} between the forward scan and the backward scan. So, the polarity of oxide trapped charge is negative and that of mobile ion charge is positive. The N_{ot} of PMA-TiO_2/S-InP as a function of PMA temperature is shown in Figure 11. The lowest N_{ot} is 7.18×10^{10} C/cm^2 at the PMA temperature of 350°C.

The C-V characteristics of TiO_2/GaAs, TiO_2/S-GaAs and PMA-TiO_2/S-GaAs are shown in Figure 12. The C-V characteristics of TiO_2/GaAs show a stretch-out phenomenon under negative bias as shown in Figure 12(a). It is from the high D_{it} due to the existence of native oxides on GaAs surface. The breakdown at higher negative bias is from the higher leakage current resulted in the grain boundary of TiO_2 polycrystalline structure. Figure 12(b) shows the C-V characteristics of TiO_2/S-GaAs. The capacitance in the accumulation region is high due to the improved interface quality and the capacitance decay at higher negative bias is due to the high leakage current. Sharp C-V curves PMA-TiO_2/S-GaAs can be obtained after PMA treatments at 300, 350, and 400°C as shown in Figures 12(c), 12(d), and 12(e), respectively. The ideal C-V curve is also shown in the figure as a reference. The work function difference ($\Phi_{ms} = -1.31$ V) of metal (Al) and semiconductor (GaAs) is taken into account. The optimized PMA temperature is 350°C as shown in Figure 12(d), in which the stretch-out phenomenon and the flat-band voltage shift are minimized. The dielectric constants and effective oxide charges of PMA-TiO_2/S-GaAs

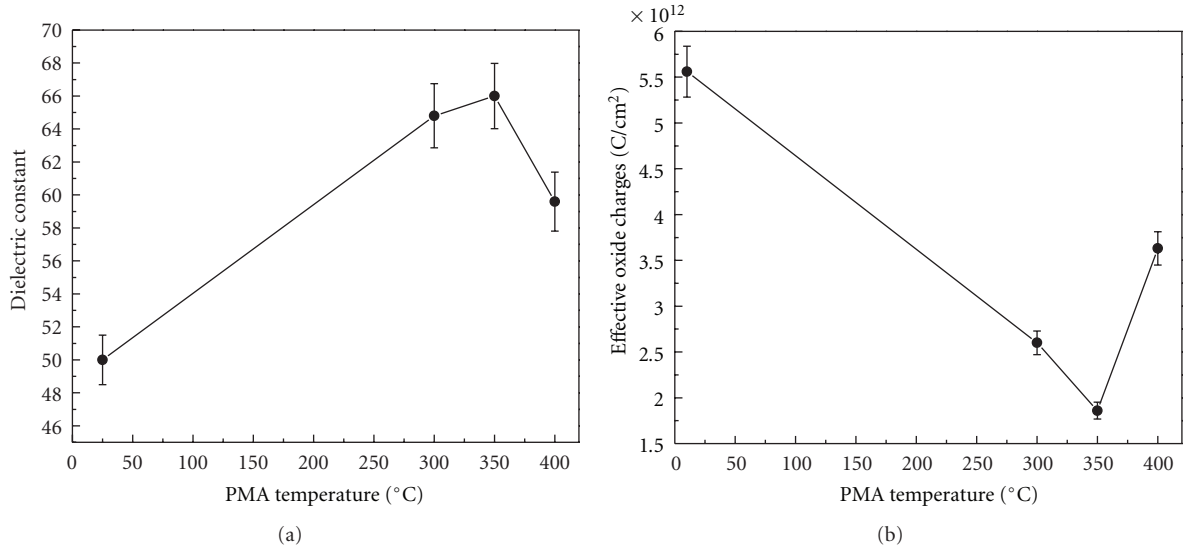


FIGURE 13: (a) Dielectric constant and (b) effective oxide charges of TiO_2/S-GaAs and PMA-TiO_2/S-GaAs at different PMA temperatures.

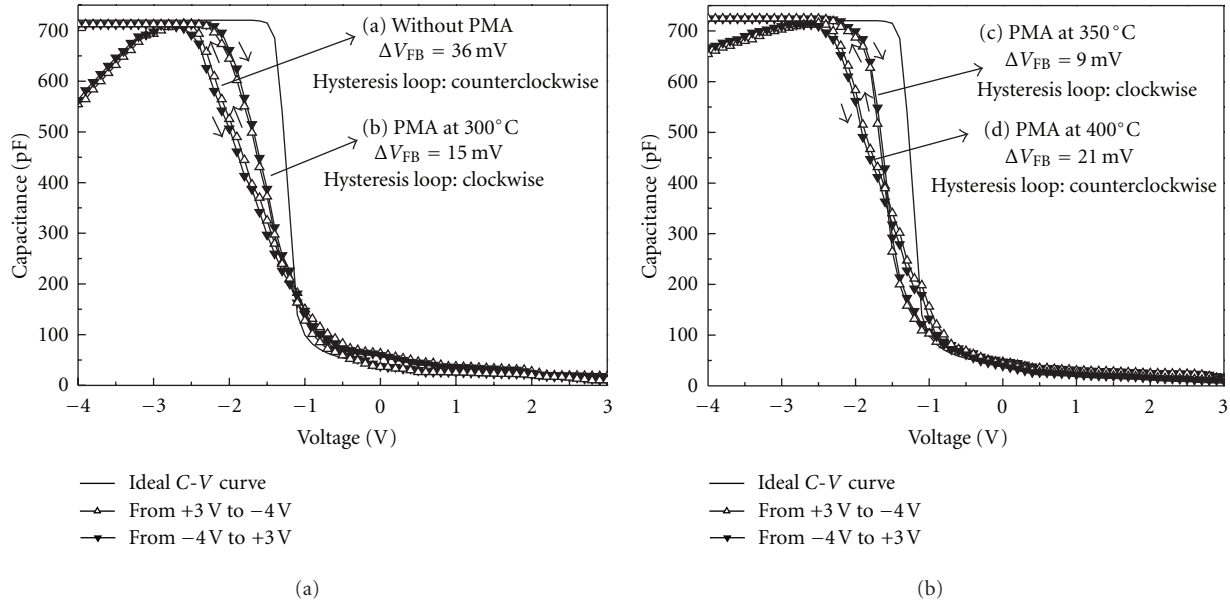


FIGURE 14: *C-V* hysteresis loops of (a) TiO_2/S-GaAs, (b) PMA at 300°C, (c) PMA at 350°C, and (d) PMA at 400°C.

films as functions of PMA temperature are shown in Figures 13(a) and 13(b), respectively. The dielectric constant and the effective oxide charges can reach 66 and 1.86 $\times 10^{12}$ C/cm^2 at the PMA temperature of 350°C.

Moreover, the *C-V* hysteresis loops as a function of PMA temperature are shown in Figure 14. The *C-V* hysteresis loop of TiO_2/S-GaAs without PMA treatment is counterclockwise as shown in Figure 14(a). The *C-V* hysteresis loops of PMA-TiO_2/S-GaAs film are clockwise at 300 and 350°C as shown in Figures 14(b) and 14(c). The *C-V* hysteresis loop changes back to counterclockwise at 400°C as shown in Figure 14(d). These *C-V* behaviors are similar to InP. The N_{ot} of PMA-TiO_2/S-GaAs as a function of PMA temperature is shown in Figure 15. The lowest N_{ot} is 5.7 $\times$ 10^{10} C/cm^2 at the PMA temperature of 350°C.

The D_{it} of TiO_2/S-InP and PMA-TiO_2/S-InP at different PMA temperatures is shown in Figure 16. The lowest D_{it} is 7.13 $\times 10^{11}$ cm^{-2} eV^{-1} at the energy of 0.67 eV from the edge of valence band. The D_{it} of TiO_2/S-GaAs and PMA-TiO_2/S-GaAs at different PMA temperatures is shown in Figure 17. The lowest D_{it} is 5.96 $\times$ 10^{11} cm^{-2} eV^{-1} at the energy of 0.7 eV from the edge of valence band. The PMA temperature of two samples was fixed at 350°C.

Table 1 shows the comparisons of electrical characteristics by PMA(350°C)-TiO_2/InP and PMA(350°C)-TiO_2/GaAs. Form this table we can clearly recognize that electrical

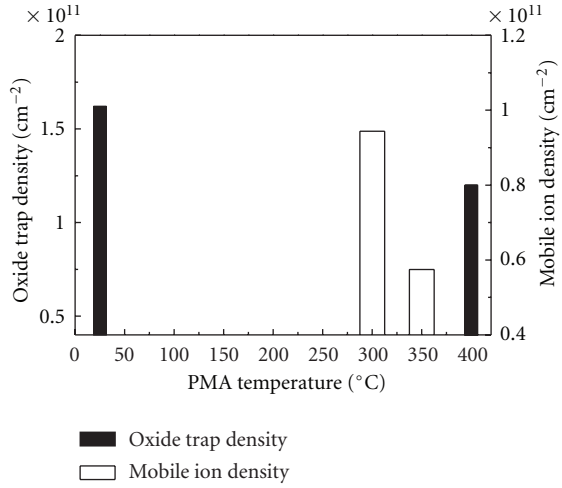


Figure 15: Oxide trap density and mobile ion density of TiO_2/S-GaAs MOS structures as a function of PMA temperature.

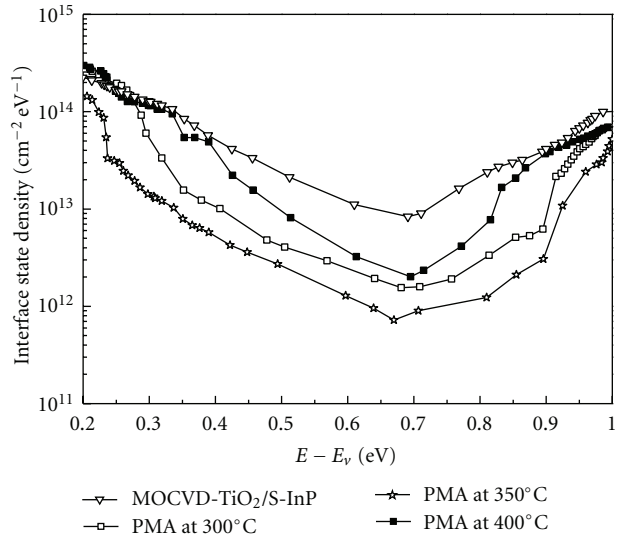


Figure 16: Interface state densities of TiO_2/S-InP and PMA-TiO_2/S-InP at different PMA temperatures.

characteristics of GaAs are superior to InP. It would be from the fact that the *P* outgas is more serious than that of As due to the higher vapor pressure. It slightly degrades the interface and film quality of InP MOS structure. PMA and $(NH_4)_2S$ treatments highly improve the electrical properties of III-V MOS structures, and dielectric films prepared by lower growth temperature can give more benefits, such as liquid phase deposition and ALD.

4. Conclusions

TiO_2 films grown on III-V semiconductors with $(NH_4)_2S$ treatments were investigated. With $(NH_4)_2S$ treatment, the interface quality of TiO_2/III-V is much improved. PMA treatment further improves the electrical characteristics. The electrical characteristics of GaAs MOS is better than that of

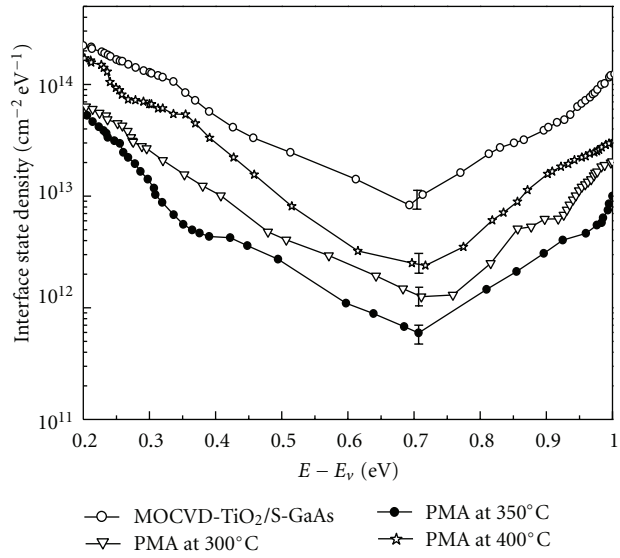


Figure 17: Interface state densities of TiO_2/S-GaAs and PMA-TiO_2/S-GaAs at different PMA temperatures.

InP, which is from the innate character of higher *P* vapor pressure. There is an interface layer from the inter-diffusion between TiO_2 and substrate. Dielectric films prepared by lower growth temperature for III-V MOS structures can give more benefits.

Acknowledgment

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Research Article

GaN-Based High-k Praseodymium Oxide Gate MISFETs with $P_2S_5/(NH_4)_2S_X$ + UV Interface Treatment Technology

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This study examines the praseodymium-oxide- (Pr_2O_3-) passivated AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) with high dielectric constant in which the AlGaN Schottky layers are treated with $P_2S_5/(NH_4)_2S_X$ + ultraviolet (UV) illumination. An electron-beam evaporated Pr_2O_3 insulator is used instead of traditional plasma-assisted chemical vapor deposition (PECVD), in order to prevent plasma-induced damage to the AlGaN. In this work, the HEMTs are pretreated with $P_2S_5/(NH_4)_2S_X$ solution and UV illumination before the gate insulator (Pr_2O_3) is deposited. Since stable sulfur that is bound to the Ga species can be obtained easily and surface oxygen atoms are reduced by the $P_2S_5/(NH_4)_2S_X$ pretreatment, the lowest leakage current is observed in MIS-HEMT. Additionally, a low flicker noise and a low surface roughness (0.38 nm) are also obtained using this novel process, which demonstrates its ability to reduce the surface states. Low gate leakage current Pr_2O_3 and high-k AlGaN/GaN MIS-HEMTs, with $P_2S_5/(NH_4)_2S_X$ + UV illumination treatment, are suited to low-noise applications, because of the electron-beam-evaporated insulator and the new chemical pretreatment.

1. Introduction

Because of their inherent high breakdown voltage (V_{BR}), high two-dimensional electron gas (2-DEG) concentration, and high saturation velocity [1, 2], and AlGaN/GaN high electron mobility transistors (HEMTs) are suitable to high-power and low-noise applications. The major factors that limit the performance and reliability of GaN-based HEMTs at radio frequencies (RF) are their high gate leakage current and drain current collapse, which is associated with native oxide-induced surface states [3, 4]. Therefore, AlGaN/GaN metal-insulator-semiconductor HEMTs (MIS-HEMTs), in which SiO_2 [5], Si_3N_4 [6], Ga_2O_3 [7], Al_2O_3 [8], and Sc_2O_3 [9] are used as the gate dielectrics, are studied, in order to address these problems. Related works focus on the formation of a high-k insulator, which reduces the Schottky gate leakage current at high input signal swings and improves channel modulation. However, the treatment of the interface between AlGaN and the insulator has not been studied systematically. Pretreatment before the deposition of the passivating layer between the source, the drain, and the gate terminals is dominated by the effect of surface traps, which cause flicker noise and current collapse problems. For example, $(NH_4)_2S_X$ sulfide treatment is known to eliminate native Ga_2O_3 and As_2O_3 dangling bonds on GaAs- and InP-related semiconductors, because of the formation of stable Ga-S and As-S bonds during immersion [10, 11]. In this work, a $P_2S_5/(NH_4)_2S_X$ + UV treatment that suppresses surface traps is studied. Furthermore, to increase the efficiency of the $P_2S_5/(NH_4)_2S_X$ treatment, the treatment is performed in a UV chamber and both the high-k ($\varepsilon \sim 10$) Pr_2O_3 gate insulator and the passivating layer are deposited using electron-beam evaporation, which effectively prevents the plasma-induced generation of surface states. A comparison of the flicker noise determined from the pulsed I-V of Pr_2O_3 AlGaN/GaN MIS-HEMT with that of traditional GaN HEMTs shows that the surface traps are markedly suppressed by $P_2S_5/(NH_4)_2S_X$ + UV treatment. The observed lower surface leakage current also improves the DC-RF dispersion of MIS-HEMT. X-ray photoelectron spectroscopy (XPS) measurement and secondary ion mass spectrometry (SIMS) are used to study the Ga-S energy bonds and the

distributions of the depths of oxygen and sulfur atoms, following $P_2S_5/(NH_4)_2S_X$ + UV treatment.

2. Device Structure and Fabrication

The AlGaN/GaN HEMT heterostructures used in this study were grown using atmospheric pressure metal organic chemical vapor deposition (AP-MOCVD) on 2 inch sapphire wafers. The 4000 nm-thick undoped GaN was grown first, to form the buffer and channel layers. Then, a 35 nm-thick undoped $Al_{0.25}Ga_{0.75}N$ layer was grown as the Schottky layer. The designed structure had a sheet charge density of 1.65 $\times$ 10^{13} cm^{-2} and a Hall mobility of 1060 cm^2/V-s at 300 K. Figure 1 shows the cross-sections of a Pr_2O_3/AlGaN/GaN MIS-HEMT with $P_2S_5/(NH_4)_2S_X$ + UV interface pretreatment. During fabrication of the device, the active region was protected by a photoresist and the mesa isolation region was removed using a BCl_3 + Cl_2 mixture gas plasma in a reactive ion etching (RIE) chamber. The ohmic contacts of the Ti/Al/Ni/Au (25 nm/125 nm/50 nm/100 nm) metal layers were deposited using electron-beam evaporation and patterned by conventional optical lithography and lift-off method, followed by 850°C RTA annealing for 30 s in an N_2 environment. Before the deposition of the high-k Pr_2O_3 insulator and the passivating layers, the samples were immersed in a standard treatment (dilute HCl), $(NH_4)_2S_X$ and $P_2S_5/(NH_4)_2S_X$ for 15 min. Figure 2 shows the pH value of the $P_2S_5/(NH_4)_2S_X$ solution versus P_2S_5 weight. The pH of the saturated $(NH_4)_2S_X$ solution is 11.2 and the pH of the mixed $P_2S_5/(NH_4)_2S_X$ solution was adjusted to a value of 7 by adding 10 g of P_2S_5 into 30 mL $(NH_4)_2S_X$ saturated solution. Although the $(NH_4)_2S_X$ treatment effectively removes the native AlGaN surface oxide layer, it cannot prevent the increase in surface roughness that is caused by the alkaline $(NH_4)_2S_X$ solution. After 15 min of pretreatment immersion, the AlGaN surface roughness was 0.24 nm for the standard treatment and 0.51 nm and 0.44 nm for the $(NH_4)_2S_X$ and $P_2S_5/(NH_4)_2S_X$ solution. Therefore, the $P_2S_5/(NH_4)_2S_X$ solution was used as the interface pretreatment solution for the MIS-HEMT. In an earlier study by the authors, the reduction of the number of native oxide-induced dangling bonds on the AlGaN surface, which are difficult to remove at room temperature, was achieved by increasing the temperature of the solution temperature to 60°C, but this increase makes the procedure more complicated and time-consuming. In this study, UV illumination is used during $P_2S_5/(NH_4)_2S_X$ pretreatment immersion, in order to rapidly eliminate the dangling bonds and form Ga-S bonds with high-binding energy. After interface treatment, a 10 nm-thick layer of praseodymium was firstly evaporated, using an optimal oxygen flow rate of 15 sccm. During this stage, the chamber pressure was increased to around 10^{-4} Torr. When the chamber pressure was reduced to 3×10^{-6} Torr, the conventional Ti/Au (30 nm/150 nm) gate metals were deposited. For comparison, a traditional Ni/Au Schottky gate GaN HEMT was also fabricated. Finally, the Ti/Au (30 nm/300 nm) metals were deposited to form the interconnection and probe pads, and a 200 nm-thick SiO_2 layer was deposited to passivate the device. The complete process was also used to fabricate a traditional Ni/Au Schottky gate GaN HEMT, for the purpose of comparison.

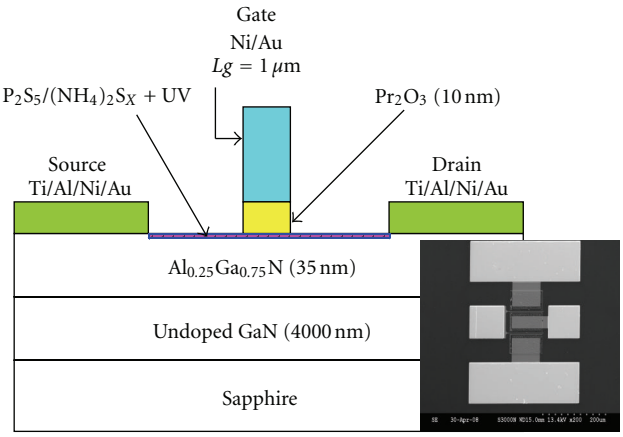


FIGURE 1: The cross-sectional structure of a $P_2S_5/(NH_4)_2S_X$+UV pretreatment Pr_2O_3 MISFET.

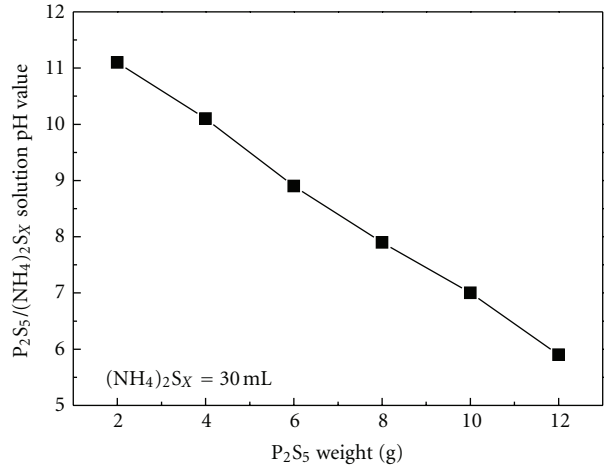


FIGURE 2: pH value of $P_2S_5/(NH_4)_2S_X$ solution versus P_2S_5 weight.

The important optimization of the flow rate of the praseodymium oxide high-k layer was also considered. The electron-beam evaporation of the high-k Pr_2O_3 thin film is optimized by adjusting the oxygen flow rate in the chamber. Figure 3 shows the EDX measurements for Pr_2O_3 grown in the electron-beam evaporator using various oxygen flow rates. An analysis of the rare-earth metal atomic concentration in the oxide layer demonstrates that the optimal flow rate for the deposition of the praseodymium oxide layer is 15 standard cubic centimeters per minute (sccm), indicating that the dielectric constant is maximized, because a strong dipole is formed at the highest possible rare-earth metal concentration in the high-k oxide layer. The thermal stability of the insulator also plays an important role in high-power GaN MIS-HEMTs because the dc power is primarily dissipated near the gate contact, which causes local Joule self-heating [10]. The channel temperature can reach 100°C during high-output-power operation, which

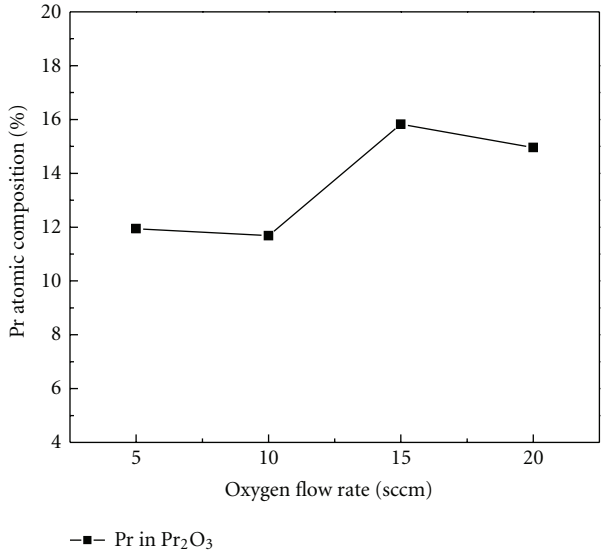
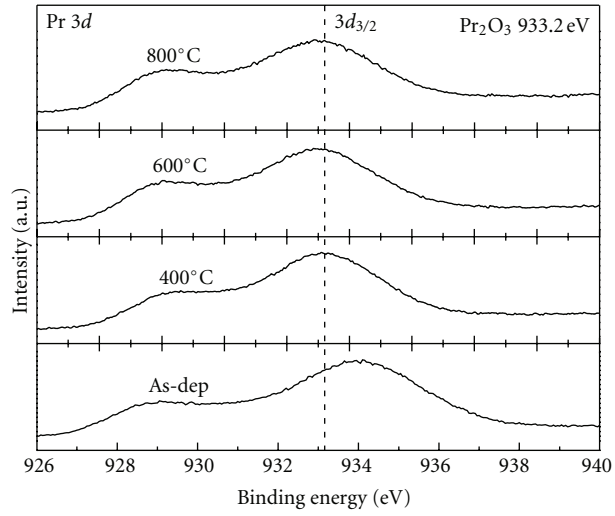
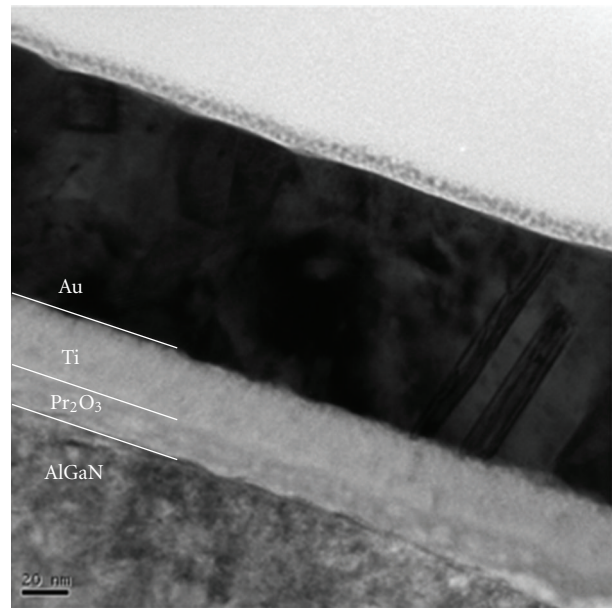


Figure 3: EDX analysis of Pr_2O_3 films with various oxygen flow rates.



(a)



(b)

Figure 4: (a) 3*d* core-level XPS spectra of Pr_2O_3 versus temperatures. (b) TEM cross-sectional photograph of Pr_2O_3 MIS-HEMT.

results in increased degradation and failure rates and a reduction in output power. In order to evaluate the thermal stability of Pr_2O_3 layer, the X-ray photoelectron spectroscopy (XPS) was used to measure the binding energy of the Pr_2O_3 thin films after 400°C, 600°C, and 800°C postannealing. Figure 4(a) shows the XPS 3*d* core-level spectra for Pr_2O_3 at various temperatures. The energy of the Ar-gun is 3 KeV, the operation current is 1 mA, and the analysis area is $2 \times 2\ mm^2$. It is seen that the binding energies of the Pr_2O_3 after 400°C, 600°C, and 800°C postannealing are close to the standard value of 934 eV in the 3*d* core level, as recorded in the XPS handbook. Figure 4(a) also shows the high signal intensities of Pr_2O_3. Therefore, it is concluded that a high-quality and a highly thermally stable high-*k* insulator is obtained by using electron-beam-evaporated Pr with a high oxygen flow rate. The results of high-resolution cross-sectional transmission electron microscopy (TEM) prove that the Pr_2O_3 grows on the GaN in a planar fashion, as shown in Figure 4(b). The Pr_2O_3 equivalent oxide thickness, measured by the TEM, is 20 nm. A $(Ga_2O_3)Pr_2O_3$ compound film occurs between the interface of the GaN and Pr_2O_3 layers, which is generated by the native GaN surface oxide layer and praseodymium materials.

3. Experimental Results for the Device

Atomic force microscopy (AFM) or scanning force microscopy (SFM) has a very high resolution, with a demonstrated resolution of the order of fractions of a nanometer, more than 1000 times better than the optical diffraction limit. It is also one of the most widely used tools for imaging, measuring, and manipulating matter at the nanoscale. The information is gathered by "feeling" the surface with a mechanical probe. Piezoelectric elements that facilitate tiny but accurate and precise movements on (electronic) command enable very precise scanning [11]. Figure 5(a) and Figure 5(b) show the 2D and 3D images of the surface roughness on the AlGaN/GaN surface with different treatments, as measured using a Park Systems XE-70. The $P_2S_5/(NH_4)_2S_X$ + UV-treated surface exhibits a better roughness than the other sulfurization treatments and forms a superior interface between the AlGaN Schottky layer and the Pr_2O_3 high-*k* gate insulator layer.

Table 1 shows the mobility, sheet charge density, and surface roughness for variously treated devices, characterized by Hall measurement at 300 K. The $P_2S_5/(NH_4)_2S_X$ + UV-treated devices have a sheet charge density of $1.403 \times 10^{13}\ cm^{-2}$ and a Hall mobility of $1150\ cm^2/V\text{-}s$ at 300 K; these

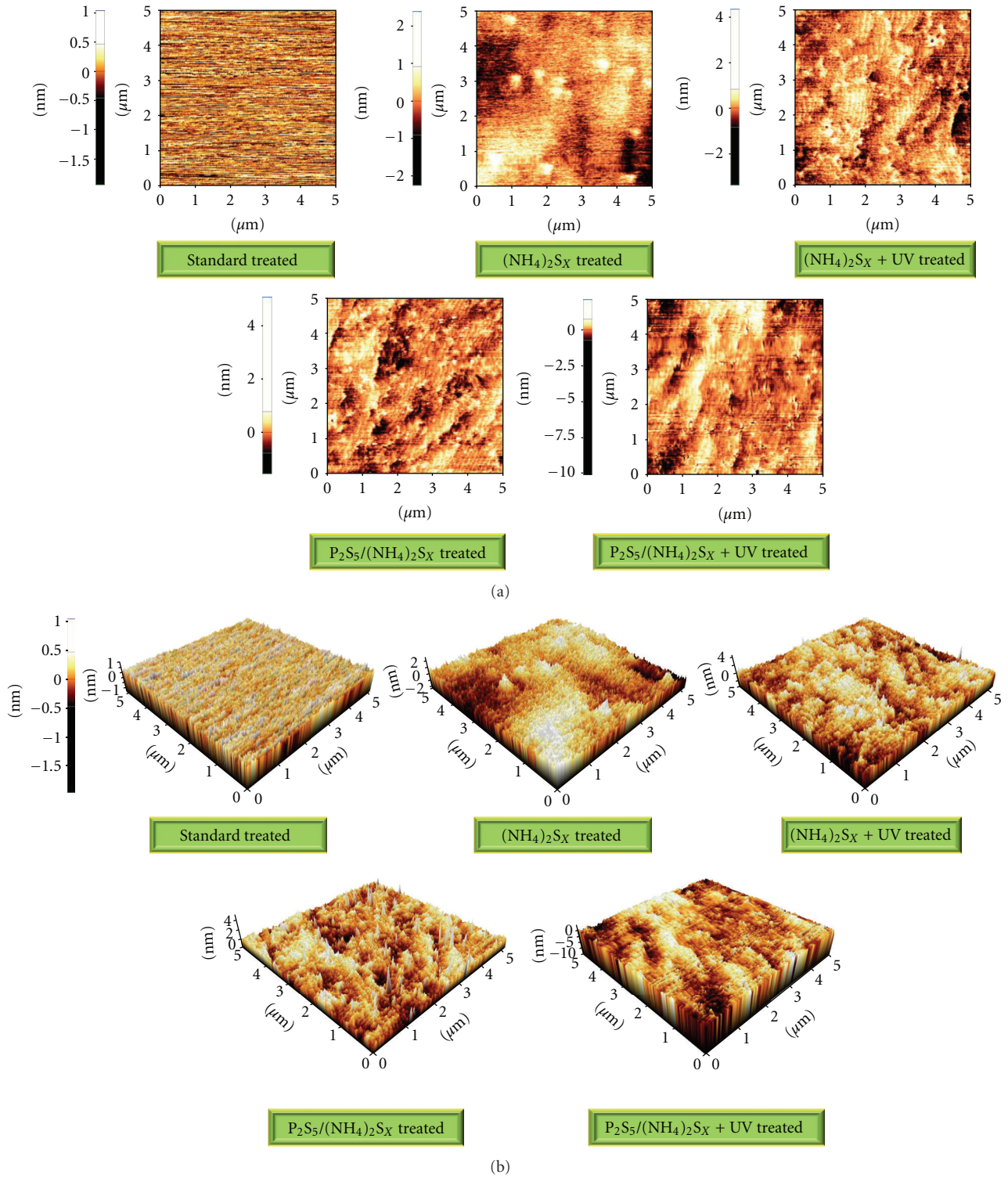


FIGURE 5: (a) 2D images of the surface roughness on AlGaN/GaN surface evaluated with different treatment. (b) 3D images of the surface roughness on AlGaN/GaN surface evaluated with different treatment.

values are, respectively, 1.648×10^{13} cm^{-2}, 1060 cm^2/V-s and 1.512×10^{13}, 1087 cm^2/V-s for the standard treatment and $(NH_4)_2S_X$ + UV treatment for the devices. These results clearly demonstrate that $P_2S_5/(NH_4)_2S_X$ + UV treatment improves the channel mobility by reducing the number of surface traps.

The surface of composite semiconductor substrates was subject to heat treatment, using an ultraviolet (UV) light,

Table 1: The Hall measurement and surface roughness results for various treatment devices.

Pretreatment	Mobility (cm^2/V-sec)	Sheet charge density (cm^{-2})	Surface roughness (nm)
Standard	1060	1.648×10^{13}	0.238
$(NH_4)_2S_X$	985	1.784×10^{13}	0.514
$(NH_4)_2S_X$ + UV	1087	1.512×10^{13}	0.471
$P_2S_5/(NH_4)_2S_X$	1100	1.485×10^{13}	0.443
$P_2S_5/(NH_4)_2S_X$ + UV	1150	1.403×10^{13}	0.382

in order to enhance the surface reaction [12]. The photoluminescence (PL) measurements in Figure 6 apply to the complete structure of AlGaN/GaN after sulfurization and demonstrate that $P_2S_5/(NH_4)_2S_X$ + UV treatment yields a greater PL intensity for the AlGaN Schottky layer than either $P_2S_5/(NH_4)_2S_X$ treatment or standard treatment. The increase in PL intensity is due to the elimination of surface states, which generates nonradiative recombination centers on the AlGaN surface [13]. No obvious $Al_{0.25}Ga_{0.75}N$ signal is evident, because the laser used is He-Cd laser and the PL signal intensity of $Al_{0.25}Ga_{0.75}N$ is much smaller than that for GaN. Because only 35 nm AlGaN was grown on GaN for the PL evaluation structure after sulfurization, the $Al_{0.25}Ga_{0.75}N$ signals are not obvious in the PL measurements. Although the $P_2S_5/(NH_4)_2S_X$ treatment can suppress the surface state density, as demonstrated by the PL results, a more concentrated $P_2S_5/(NH_4)_2S_X$ solution with UV illumination treatment produces a stable phosphorus oxide layer and more Ga-S bonds, because the phosphorus and sulfur concentrations are higher [14].

Figure 7 shows the S_{2p} and Ga_{2p} XPS spectra of the variously treated devices. The sulfur 2*p* core level and the binding energy of pure sulfur are all 163.8 eV. The binding energy of gallium is 160 eV at the signal peak in the spectrum of the standard treated GaN sample while the signal peak of the $P_2S_5/(NH_4)_2S_X$-treated device is shifted to 160.3 eV, because the AlGaN surface contains Ga-S bonds (Ga-S = 163.2 eV) after this process. However, $P_2S_5/(NH_4)_2S_X$ + UV treatment shifts the signal peak in the spectrum to 160.4 eV, with a linear distribution of intensity from 160 eV to 161 eV. The Ga_{2p} peaks are shifted to a higher binding energy after $P_2S_5/(NH_4)_2S_X$ + UV treatment. This phenomenon is related to the Ga sulfurized states [15]. Therefore, more Ga-S bonds are generated on the AlGaN surface by $P_2S_5/(NH_4)_2S_X$ + UV treatment than by $P_2S_5/(NH_4)_2S_X$ treatment and these high-energy bonds are more stable than the Ga-O bonds that are formed in a moist environment.

In order to investigate the material atomic composition of the AlGaN surface after various sulfide treatments, the samples were subject to secondary ion mass spectroscopy (SIMS). Figure 8 shows the sulfur and oxygen atom concentration profiles of the samples treated using the three aforementioned methods. Based on the measurement results shown in Figure 8(a), the concentration of S atoms in the $P_2S_5/(NH_4)_2S_X$ and $P_2S_5/(NH_4)_2S_X$ + UV-treated samples

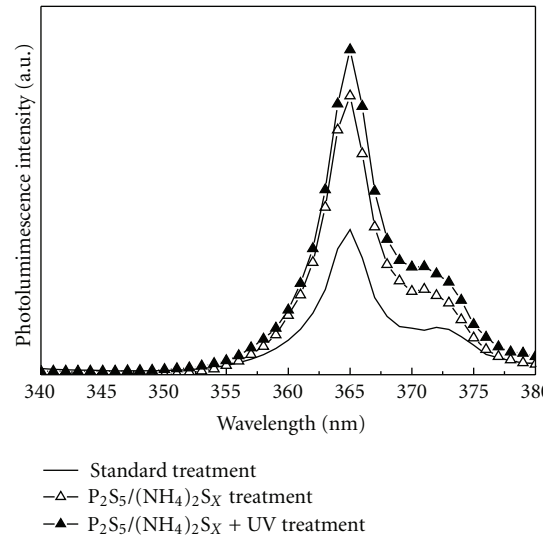


Figure 6: PL measurement results for AlGaN/GaN full structure standard, $P_2S_5/(NH_4)_2S_X$ and $P_2S_5/(NH_4)_2S_X$ + UV treatments.

is relatively high near the AlGaN surface, dropping by two to three orders of magnitude in the channel. However, few S atoms are observed after the standard treatment. The S atoms produced from the sulfide solution are incorporated into the sample surface, which is similar to the effect of the immersion of CF_4 in plasma, used to enable a GaN HEMT to operate in enhancement mode [16]. In order to further investigate the mechanism for the removal of Ga-O bonds by sulfur treatments, an experiment was conducted to determine the oxygen concentration distribution; Figure 8(b) shows the results. The lowest curve in the figure shows that the $P_2S_5/(NH_4)_2S_X$ + UV treatment removes a huge amount of AlGaN/GaN native oxide and reduces the number of oxygen atoms more effectively than the other treatments, because UV illumination provides enough energy to the sulfur atoms to replace the Ga-O bonds and form stable Ga-S bonds. Therefore, $P_2S_5/(NH_4)_2S_X$ + UV treatment not only produces a smoother Schottky interface, reducing the gate leakage current, but also reduces the number of oxygen atoms more effectively. Both effects reduce the density of the surface states.

Figure 9 plots the gate-to-drain *I-V* curves for a standard GaN HEMT, a Pr_2O_3 MIS-HEMT, and a $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MIS-HEMT. A reduction in the number surface states and leakage current in the sulfide-treated sample means that $P_2S_5/(NH_4)_2S_X$ + UV-treated MIS-HEMTs have a higher V_{ON} value than the others. The improved V_{ON} value of 1.71 V for the $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3-gate device results in a significant reduction in the gate leakage current at a high pumped gate voltage, which improves the linearity and results in a reduction in the signal dispersion of the device. The reversed gate-to-drain breakdown voltages (V_{BR}), defined as the voltage at which the gate leakage current is −1 mA/mm, are −131.3 V for the $P_2S_5/(NH_4)_2S_X$ + UV-treated samples, which allows operation at high drain voltage, and only −128.2 V and

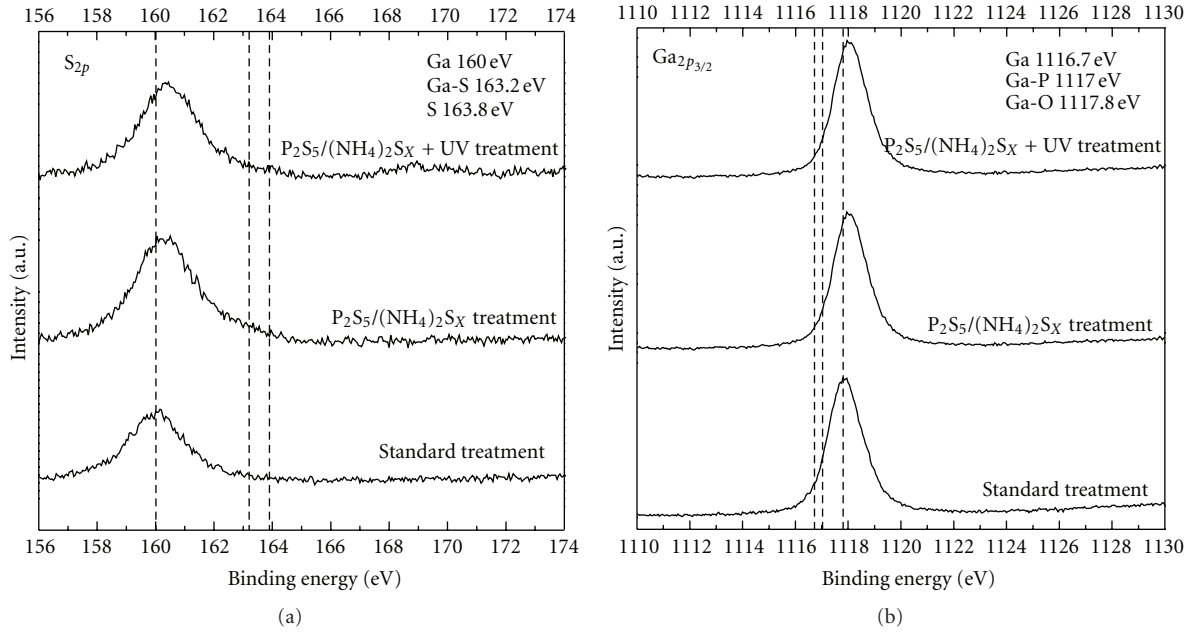


FIGURE 7: The XPS spectra of S_{2p} (a) and Ga_{2p} (b) and core level of various treatment samples.

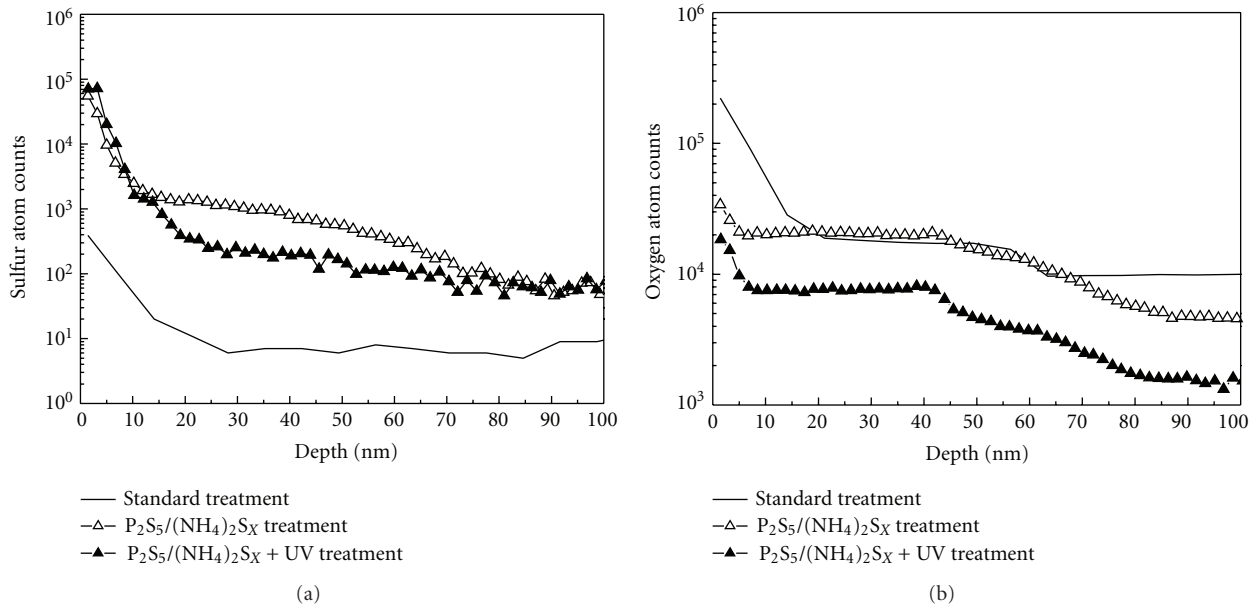


FIGURE 8: The SIMS measurements of the S atoms (a) and O atoms (b) distribution versus AlGaN/GaN depth for various treatment samples.

−107.5 V for the Pr_2O_3 MIS-HEMT and standard-treated samples, respectively.

In order to study the dc characteristics, the drain-to-source current (I_{ds}) versus drain-to-source voltage (V_{ds}) curves for three devices are shown in Figure 10. The drain current does not vary significantly between the treated devices. The turn-on resistance (R_{ON}) is 3.958 Ω for the HEMTs subject to standard treatment, at V_{gs} of 0 V, and 4.675 Ω and 4.210 Ω for the Pr_2O_3 MIS-HEMTs and the $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MIS-HEMTs, respectively. This is primarily because the sulfide solution influences only the surface states, rather than the intrinsic parameters. However, since the traps within the interface between the gate and channel are suppressed by $P_2S_5/(NH_4)_2S_X$ + UV treatment, the sample with this treatment has the highest output resistance, which results in an increase in device linearity and power gain cut-off frequency (f_{max}). The output conductance (g_0) of the $P_2S_5/(NH_4)_2S_X$ + UV-treated

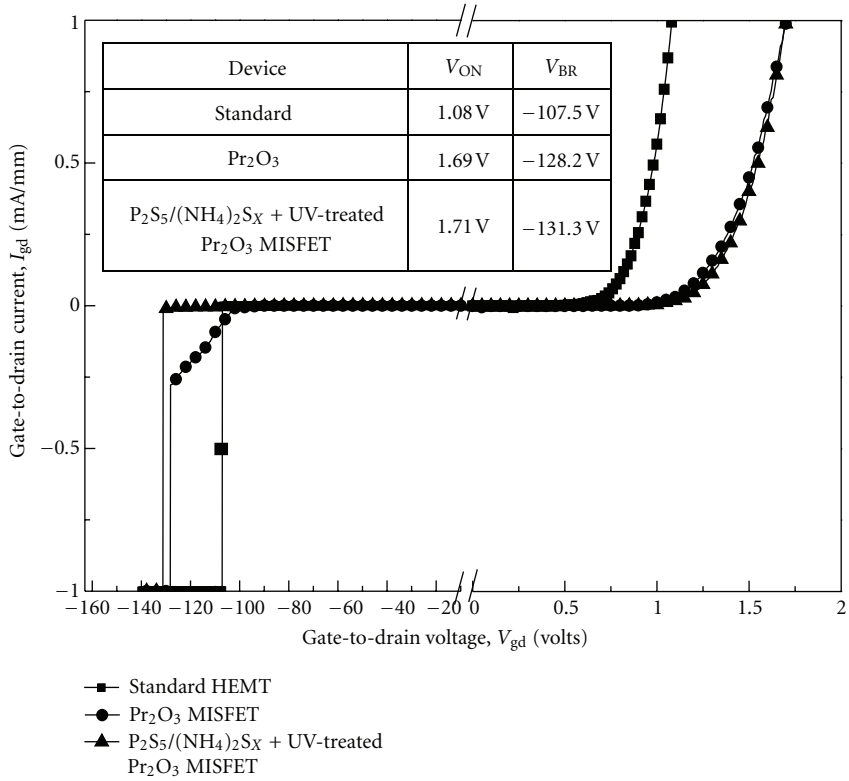


Figure 9: The device gate-to-drain I-V characteristics of standard HEMT, Pr_2O_3 MISFET, and $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MISFET.

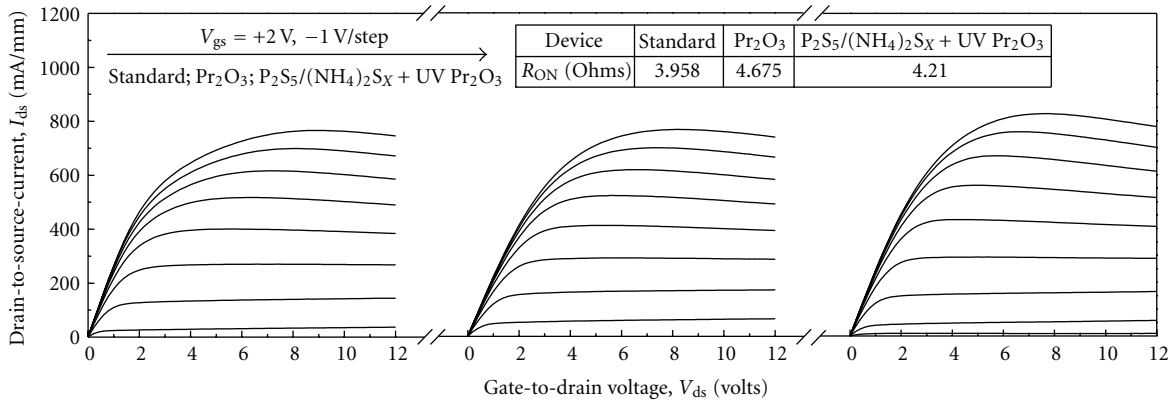


Figure 10: The I_{ds}-V_{ds} characteristics of various devices.

Pr_2O_3 MIS-HEMTs is 0.46 mS/mm; the corresponding values for the Pr_2O_3 MIS-HEMTs and the standard device are 0.6 mS/mm and 1 mS/mm, respectively.

Figure 11 plots the transistor transconductance (g_m) versus V_{gs} curves for the three devices of interest at a V_{ds} of 8 V. The maximum drain-to-source currents ($I_{d\,max}$) at V_{gs} = 4 V are 923 mA/mm, 864 mA/mm, and 920 mA/mm, for the standard HEMTs, the Pr_2O_3 MIS-HEMTs, and the $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MIS-HEMTs, respectively. The maximum transconductance values (g_m), biased at V_{ds} = 8 V, are 144 mS/mm, 121 mS/mm, and 132 mS/mm, respectively. All of these values are reasonably favorable. The standard HEMTs exhibit a higher peak g_m, because a high-k insulator is inserted in the MIS-HEMTs structure. The gate-to-channel improves channel modulation and effectively modulates any increase in the depletion region between the metal gate and the channel. Obviously, high-k GaN MIS-HEMTs demonstrate large swing voltage and low gate leakage current.

The measurement of on-wafer microwave S-parameters for $1 \times 200\,\mu m^2$ devices was performed in a common-source configuration using an Agilent E8364C PNA network analyzer, from 0.1 GHz to 20.1 GHz. S-parameter measurements demonstrate a maximum current gain cut-off frequency (f_T) of 9.2 GHz and a maximum oscillation frequency (f_{max}) of 16.8 GHz for standard HEMTs. These values are 7.9 GHz

Table 2: The dc and RF characteristics comparisons of a standard HEMT, a Pr_2O_3 MISFET, and a $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MISFET.

Measurement results	Standard	Pr_2O_3	$P_2S_5/(NH_4)_2S_X$ + UV Pr_2O_3
Schottky turn-on voltage (V_{ON})	1.08 V	1.69 V	1.71 V
Breakdown voltage (V_{BR})	−107.5 V	−128.2 V	−131.3 V
Pinch-off voltage (V_p)	−5.8 V	−6.4 V	−6.8 V
Maximum drain current ($I_{d\max}$)	923.4 mA/mm	864.4 mA/mm	920.04 mA/mm
Peak transconductance (g_m)	143.58 mS/mm	121 mS/mm	132.36 mS/mm
Current gain cut-off frequency (f_T)	9.2 GHz	7.9 GHz	8.5 GHz
Maximum oscillation frequency (f_{max})	16.8 GHz	19.2 GHz	16.2 GHz

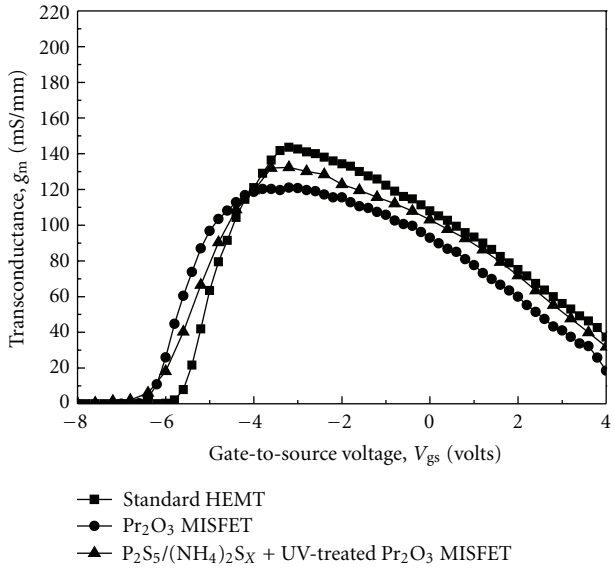


Figure 11: The g_m-V_{gs} characteristics of various devices.

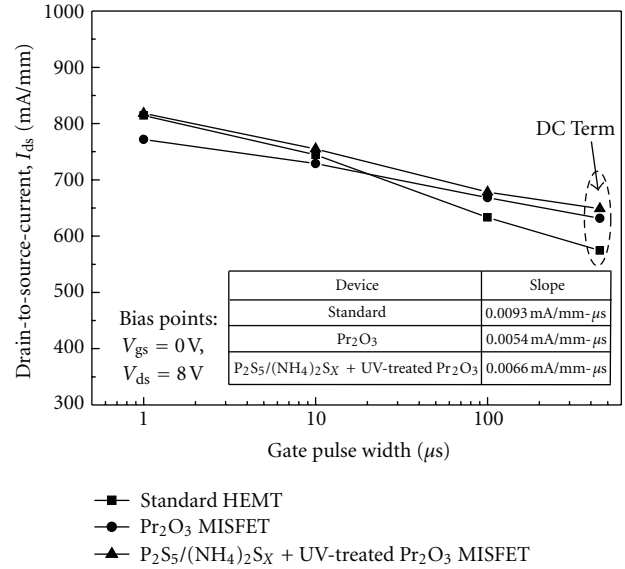
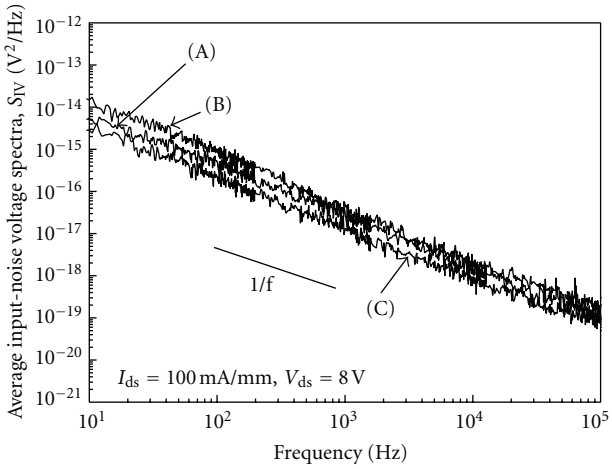


Figure 12: Pulse measurement characteristics of various devices.

and 10.7 GHz for Pr_2O_3 MIS-HEMTs and 8.5 GHz and 16.2 GHz for $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MIS-HEMTs, at V_{ds} = 8 V and V_{gs} = −3.2 V, respectively. The superior RF characteristics for $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MIS-HEMTs prove their greater power and linearity. Table 2 presents dc and radio RF characteristics for various devices.

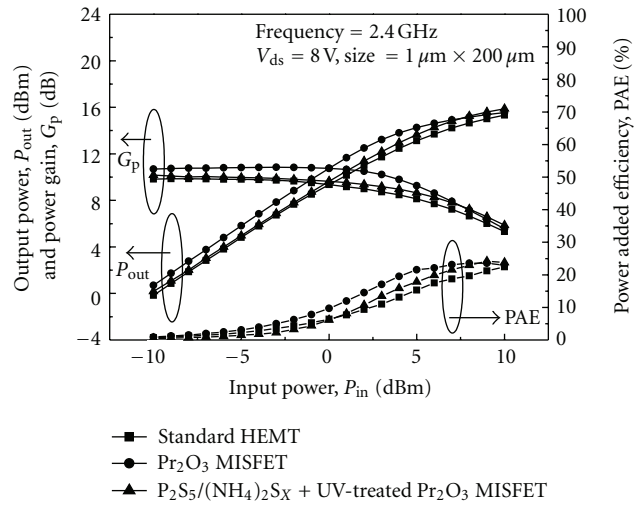
Pulse measurements were made to characterize the carrier trapping phenomenon and heating effect in the device. With respect to the trapping carriers, the response time dominates the pulse measurement. The response time for these trapping carriers is typically of the order of μs longer than the ns of carrier transportation, especially for high-speed and high-power devices. In order to more easily observe the output signals from the drains of each device, a 50 Ω resistor was added between the drain electrode and the power supply, in order to determine the total drain-to-source current and to reduce the damping effect in the output square waveform. Pulse *I-V* measurements for the three devices were also made, in order to confirm their surface trapping effects. Figure 12 plots the dc to 1 μs pulse *I-V* measurement for $1 \times 100\,\mu m^2$ devices at a V_{gs} of 0 V and a V_{ds} of 8 V, for the three devices. The gate width of the measured devices is 100 μm, so the heating effect could therefore be neglected. Since the surface states determine the dispersion effect, the current density at high current decays as the pulse width decreases. As shown in the figure, the standard GaN HEMTs demonstrate a larger slope with respect to the pulse period than do the Pr_2O_3 MIS-HEMTs and $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MIS-HEMTs. It is evident that $P_2S_5/(NH_4)_2S_X$ + UV treatment produces reliable and stable surface performance and less load-line hysteresis and better linearity for the device in high-power applications are which both expected.

To investigate the relationship between the flicker noise and the quantity of the variously treated devices, a low-frequency noise measurement was performed, because, at low frequency, this is sensitive to the semiconductor surface [17]. The bias point for low-frequency noise measurement was selected as V_{ds} = 8 V, which gives an I_{ds} of 100 mA/mm for all devices. Since the measurement is dominated by the series resistance of each device, identical I_{ds} bias point confirms the flicker noise characteristics. As shown in Figure 13, the $P_2S_5/(NH_4)_2S_X$ + UV-treated MIS-HEMT demonstrates a lower 1/f spectral noise than both the Pr_2O_3 MIS-HEMT and the GaN HEMT, which proves



(A) Standard HEMT
(B) Pr_2O_3 MISFET
(C) $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MISFET

Figure 13: The 1/f noise comparisons for various devices.



Standard HEMT
Pr_2O_3 MISFET
$P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MISFET

Figure 14: Power performances of three devices under 2.4 GHz and V_{ds} of 8 V operation.

the reduction in the number of surface dangling bonds due to $P_2S_5/(NH_4)_2S_X$ + UV treatment.

The fabricated 1 μm long gate GaN HEMT, Pr_2O_3 MIS-HEMT, and $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3MIS-HEMT were tested on-wafer and the microwave power characteristics were evaluated using a load-pull system with automatic tuners, which simultaneously provides conjugate-matched input and load impedances for the maximum output power. The microwave load-pull power performance was conducted at 2.4 GHz, with a drain bias of 8 V, using various devices. The bias points for class AB operation of the standard HEMT, the Pr_2O_3 MIS-HEMT, and the $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MIS-HEMT must be biased at −3.1 V, −3.7 V, and −3.4 V (at 1/4 $I_{d\,max}$), respectively. Figure 14 shows the output power (P_{out}), power gain (G_p), and PAE as a function of the input power (P_{in}), for various devices with gate dimensions of 1 × 200 μm^2. The $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MIS-HEMT has better dc current and lower gate leakage current than that of the standard HEMT or the Pr_2O_3 MIS-HEMT, at high-input-power swing. The PAE values are 22.4%, 23.6%, and 24.2%, for the standard HEMT, the Pr_2O_3 MIS-HEMT and the $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MIS-HEMT, respectively. As a result, the microwave-power performance is improved by the MIS-gate structure, and the power-gain degradation is also improved in the high-input-power regime. The reduction in gate leakage current in the $P_2S_5/(NH_4)_2S_X$ + UV-treated Pr_2O_3 MIS-HEMT allows a significant improvement in device linearity [18].

4. Conclusion

In summary, Pr_2O_3 MIS-HEMTs with low gate leakage current and low flicker noise, as a result of $P_2S_5/(NH_4)_2S_X$ + UV treatment, were developed and characterized. An electron-beam-evaporated high-k insulator and a passivating layer prevent the formation of surface states by plasma. $P_2S_5/(NH_4)_2S_X$ + UV treatment represents a simple and efficient means of reducing the number of surface dangling bonds. Based on the results of Hall, XPS, and SIMS measurements, this $P_2S_5/(NH_4)_2S_X$ + UV treatment prevents the formation of strong Ga-S bonds on the AlGaN surface. This reduction in surface states improves carrier mobility and simultaneously suppresses unstable native Ga-O bonds. This novel pretreatment is therefore proven to be eminently suitable to low-noise GaN MIS-HEMT applications.

Acknowledgments

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Research Article

Comparative Study of SiO_2, Al_2O_3, and BeO Ultrathin Interfacial Barrier Layers in Si Metal-Oxide-Semiconductor Devices

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In a previous study, we have demonstrated that beryllium oxide (BeO) film grown by atomic layer deposition (ALD) on Si and III-V MOS devices has excellent electrical and physical characteristics. In this paper, we compare the electrical characteristics of inserting an ultrathin interfacial barrier layer such as SiO_2, Al_2O_3, or BeO between the HfO_2 gate dielectric and Si substrate in metal oxide semiconductor capacitors (MOSCAPs) and n-channel inversion type metal oxide semiconductor field effect transistors (MOSFETs). Si MOSCAPs and MOSFETs with a BeO/HfO_2 gate stack exhibited high performance and reliability characteristics, including a 34% improvement in drive current, slightly better reduction in subthreshold swing, 42% increase in effective electron mobility at an electric field of 1 MV/cm, slightly low equivalent oxide thickness, less stress-induced flat-band voltage shift, less stress induced leakage current, and less interface charge.

1. Introduction

The CMOS scaling is bringing the SiO_2 thickness below 1.5 nm. For these very thin oxides, the leakage current becomes unacceptably large. One way to reduce the leakage current is the substitution of the SiO_2 by a material with a higher dielectric constant. The main advantage of high-k dielectrics is the low gale leakage achieved due to its high physical thickness. That also makes it attractive for low power applications. Because of these requirements, over the past 10 years, hafnium oxide (HfO_2) has gained considerable interest as a high dielectric constant material for fabricating complementary metal oxide semiconductor (CMOS) devices. It has several attractive properties such as a high dielectric constant, good thermodynamic stability with Si, and good electrical properties [1]. Unfortunately, some of the other physical properties like mobility reduction, charge trapping, and threshold voltage (V_{th}) instability are a major drawback for the performance of metal oxide semiconductor field effect transistors (MOSFETs) [2]. Especially HfO_2 high-k dielectric stacked MOSFETs were reported with low carrier mobility [3]. The main cause for the low mobility is still unknown, but has been attributed to remote Coulomb scattering caused by charges in the high-k dielectric [4] or optical phonon scattering [5]. Many researchers have believed that it is inevitable for all high-k dielectrics to have low energy bandgap and high scattering, compared to SiO_2. Therefore, if high-k dielectric with high energy bandgap and low scattering can be found, it will be the true solution for the above problems.

An alternative promising high-k gate dielectric material is beryllium oxide (BeO), which has superior interface stability [6–10] and is already known as an excellent gas diffusion barrier. This makes it a potentially suitable diffusion barrier

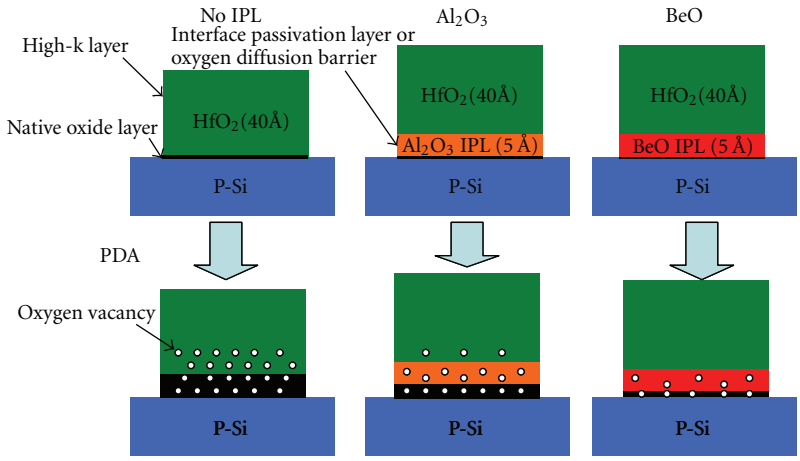

Figure 1: Cross-sectional MOS devices with various IL. The BeO interfacial layer is placed between HfO_2 and p-type Si substrate.

between HfO_2 and Si in CMOS processing. BeO also has metal-like thermal conductivity and a large energy bandgap (10.6 eV). These properties are indicative of low optical phonon and remote Coulomb scattering. Generally, a flow of phonons is responsible for heat conduction in dielectric materials. As the temperature increases, phonon density increases, but above 20 K, the phonon-phonon interaction becomes dominant and reduces the mean free path of the phonon drift, degrading thermal conductivity in the dielectrics [11]. BeO, however, has high thermal conductivity due to low phonon scattering because electrons in BeO are tightly and closely bound, so that the phonons in BeO are coupled to each other and have low energy and long wavelengths (or low phonon frequency). The high energy bandgap and band offset of BeO on Si makes intrinsic charge trapping difficult and results in a low trapped charge in the BeO dielectric (trapped charges in high-k dielectrics are the source of Coulomb scattering) [10]. Our previous studies have showed electrical and physical characteristics that BeO deposited with dimethylberyllium and water improves interface quality on III-V MOS devices by preventing sub-oxidation between high-k and III-V substrate during PDA [6]. In this paper, we compare the effect of interfacial barrier layer by inserting ultrathin SiO_2, Al_2O_3, or BeO barrier layer (IL) between the HfO_2 gate dielectric and Si substrate in metal oxide semiconductor capacitors (MOSCAPs) and NMOSFETs. The aim of using such a barrier layer was to improve the device performance and reliability while maintaining, as much as possible, the overall dielectric constant of the resulting film.

2. Fabrication Procedure

An ALD BeO IL was deposited on HF-last p-type Si substrates using dimethylberyllium precursors and water as an oxygen source. As a reference, ALD Al_2O_3 IL was deposited on the same cleaned substrate using trimethylaluminum and the same oxygen source. Samples with a BeO IL, Al_2O_3 IL, and without an IL were followed by ALD HfO_2. They were annealed for 3 min at 600°C in N_2 at atmospheric pressure. The physical thickness of the BeO and Al_2O_3 IL layers was controlled from the deposition rate which was measured on the bulk oxide using multiple-wavelength (200~900 nm) ellipsometry. The TaN electrode was deposited using reactive dc magnetron sputtering at 2000 Å followed by reactive ion etching (RIE) with Ar + CF_4 after electrode patterning of the gate. The source/drain (S/D) regions of NMOSFETs were implanted with phosphorus at 50 keV and a dose of 5×10^{15} cm^{-2}. High temperature (900°C, 1 min) annealing in N_2 ambient was used for S/D activation. E-beam evaporated Ni/AuGe/Au was used for both S/D and backside metallization. The final sintering was done at 400°C in forming gas for 30 min. For all MOSCAPs samples, PMA (500°C, 2 min) was done.

3. Results and Discussion

Figure 1 shows the cross-sectional MOS structure with various IL (or IPL). It is constructed based on the electrical and physical results in the previous experiments [10]. SiO_2, Al_2O_3, or BeO IL is placed between HfO_2 and the P-Si substrate. Al_2O_3 and BeO IL are intentionally inserted, but SiO_2 IL is thermally grown during post-deposition and S/D activation anneals. In Figure 2, the BeO(IL)/HfO_2 structures show the lowest leakage, comparable to those of SiO_2(IL)/HfO_2 and Al_2O_3(IL)/HfO_2 gate stacks. Insertion of BeO IL (5~10 Å) doesn't increase the EOT significantly after the post-deposition anneal (PDA) due to the efficient suppression of the oxygen diffusion during PDA. The effectiveness of oxygen diffusion barrier for BeO IL is more presented as the annealing temperature increases in Figure 3. BeO IL may have some advantage for EOT scaling and reliability improvement After S/D activation, around 15 Å SiO_2 is grown at the interface between HfO_2 and the Si substrate. The low EOT of BeO IL is an indication of efficient oxygen diffusion barrier. The similar results were presented using X-ray photoelectron spectroscopy (XPS) [10]. Oxygen diffusion through thin films is proportional to the number and size of pinholes in the respective film [12]. In general, smaller pinholes cause more collisions between the diffusing

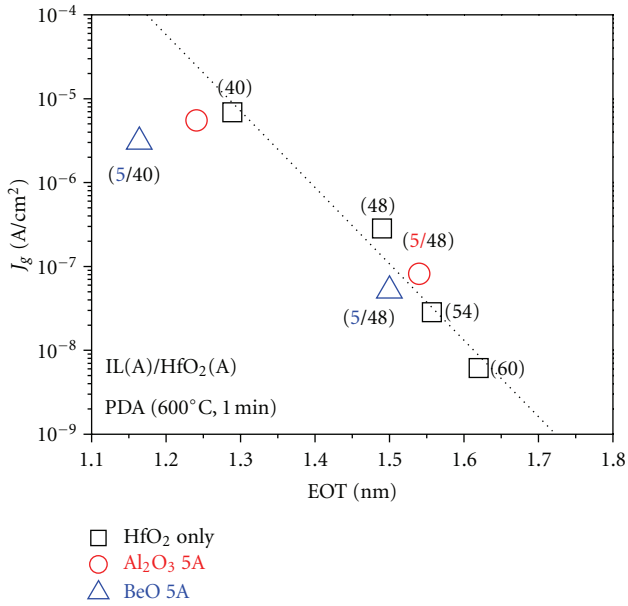

FIGURE 2: Gate leakage current versus EOT for SiO_2/HfO_2, Al_2O_3(IL)/HfO_2, and BeO(IL)/HfO_2 gate stacks.

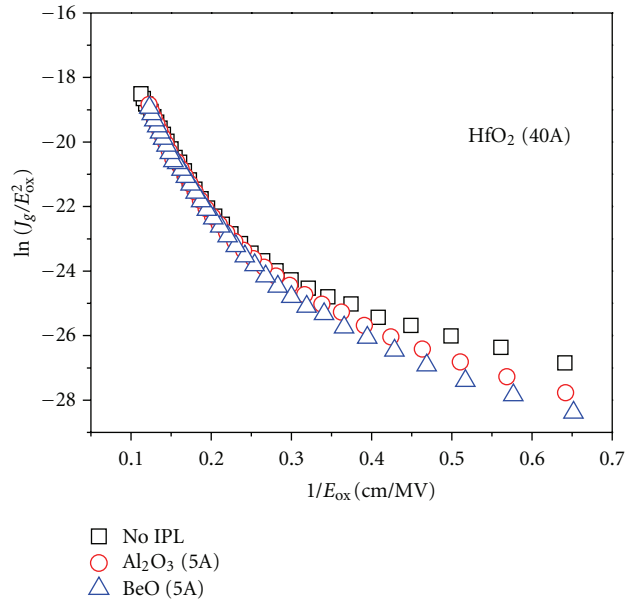

FIGURE 4: F-N plots to compare the effective potential barrier height for three different gate stacks.

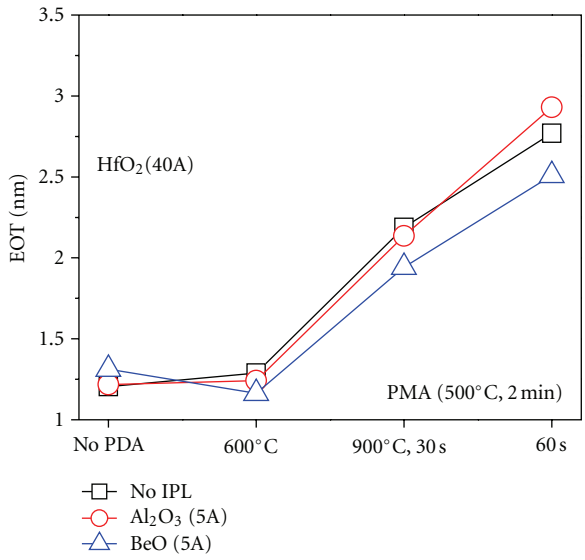

FIGURE 3: The change of EOT with the annealing temperature and duration for three different gate stacks.

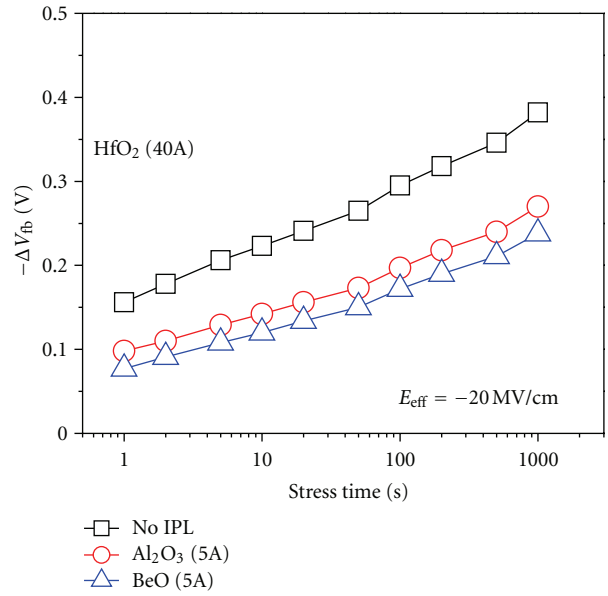

FIGURE 5: Stress-induced V_{fb} shift (ΔV_{fb}) versus stress time for three different gate stacks. $E_{eff} = (V_g - V_{fb})$/EOT.

molecules (e.g., oxygen) and the chemical groups present in the bulk film, reducing the rate of permeation. For reasons that are still under investigation, films of BeO, which have small molecular size, appear to exhibit relatively low oxygen diffusivity and are capable of effectively blocking the diffusion of impurities, such as Hf, thus minimizing defects in the substrate.

In general, the bandgap of the high-k material is inversely proportional to its permittivity, but BeO is an exception, having a very large energy bandgap (10.6 eV) combined with a still high dielectric constant of 6.8. As the bandgap, or correspondingly, band offset increases, a charge trapping in the dielectric decreases. The effective potential barrier heights for SiO_2/HfO_2, Al_2O_3(IL)/HfO_2, and BeO(IL)/HfO_2 gate stacks are compared using the Fowler-Nordheim plot in Figure 4. Due to bilayer gate structure, exact number of the effective barrier height is not extracted. But a higher barrier of the BeO IL stack is observed and it may results in the smaller electron tunneling currents, compared to other different gate stacks. Figures 5 and 6 are the representative results of reliability statistics characteristics. In Figure 5,

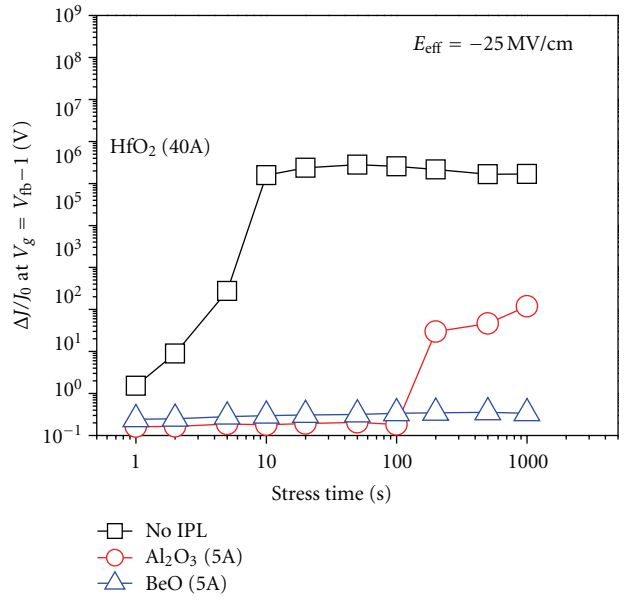

FIGURE 6: Stress-induced leakage current ($\Delta J_g/J_0$) versus stress time. $E_{eff} = (V_g - V_{fb})/EOT$.

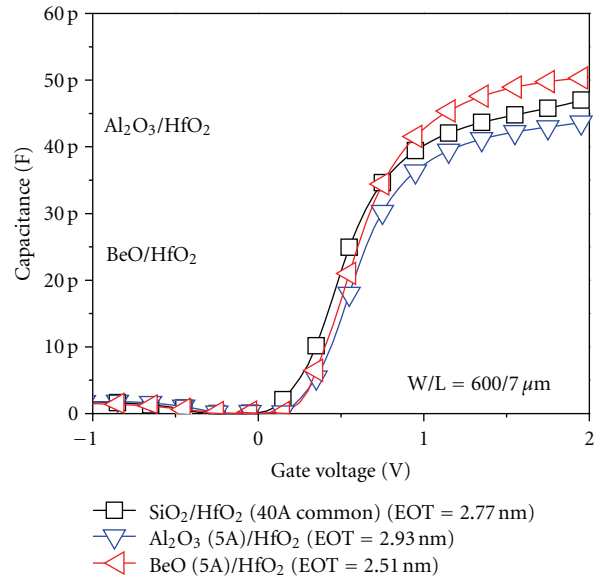

FIGURE 7: NMOSFETs inversion capacitance for three different gate stacks.

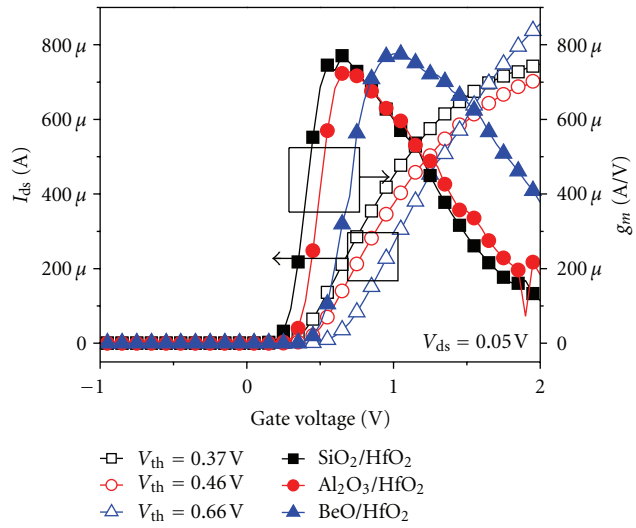

FIGURE 8: NMOSFETs $I_d - V_g$ characteristics of three gate stacks. BeO IL shows slightly higher V_{th}, G_m, and I_d.

the $BeO(IL)/HfO_2$ gate stack shows less initial V_{fb} shift (after 1 sec stress) indicating fewer preexisting traps in the dielectric. A slightly smaller trap generation rate was also observed compared to other two gate stacks. In Figure 6, the $BeO(IPL)/HfO_2$ also shows the reduced stress-induced leakage current (SILC) degradation and no significant breakdown. But SiO_2/HfO_2 and $Al_2O_3(IL)/HfO_2$ show gradual breakdown with stress time. The lower trap generation rate and the reduced tunneling current of the $BeO(IPL)/HfO_2$ gate stack may improve the reliability characteristics and it may be the indication of the high structural stability. In the view point of thermodynamics of materials, the total entropy of a material consists of its thermal entropy, which is related to thermal conductivity, and configurational entropy, which is related to the crystallization (or crystallinity) of the material [13]. With high crystallinity and thermal conductivity, BeO may have high total entropy, and it means that BeO is more structurally stable, compared to other gate dielectrics, even though the direct correlation between thermodynamic stability and device performance is still questionable. For more details of BeO thermal stability, please see the reference [14]

Figure 7 is NMOSFET inversion capacitance for SiO_2/HfO_2 (40 Å), Al_2O_3(5 Å)/HfO_2 (40 Å), and BeO(5 Å)/HfO_2 (40 Å) gate stacks. The BeO/HfO_2 gate stack shows a slightly lower equivalent oxide thickness (EOT) (2.51 nm) than SiO_2/HfO_2 (2.77 nm) and Al_2O_3/HfO_2 (2.93 nm) even though the EOTs for all gate stacks significantly increased after S/D activation annealing (Figure 3). From the XPS analysis, EOT increase is mainly due to the oxygen in HfO_2 dielectric, instead of oxygen residue in anneal tool [10]. For SiO_2/HfO_2, Al_2O_3/HfO_2, and BeO/HfO_2 gate stacks, 1.7 nm, 1.5 nm, and 1.0 nm are expected for native oxide to be grown, respectively, based on Figure 3 results. Figure 8 shows NMOSFET drain current-gate voltage ($I_d - V_g$) characteristics of SiO_2/HfO_2, Al_2O_3/HfO_2, and BeO/HfO_2 gate stacks. With the slightly lower EOT, the BeO/HfO_2 stack exhibits more positive V_{th} (0.66 V), higher drive current at V_g = 2 V, and better subthreshold swing (69 mV/dec), compared to those of the SiO_2/HfO_2 stack (V_{th} = 0.37 V, SS = 77 mV/dec) and Al_2O_3/HfO_2 stack (V_{th} = 0.46 V, SS = 70 mV/dec). The threshold voltage equation obtained from an ideal MOS structure [15] is

$$V_{th} = \Phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F, \quad (1)$$

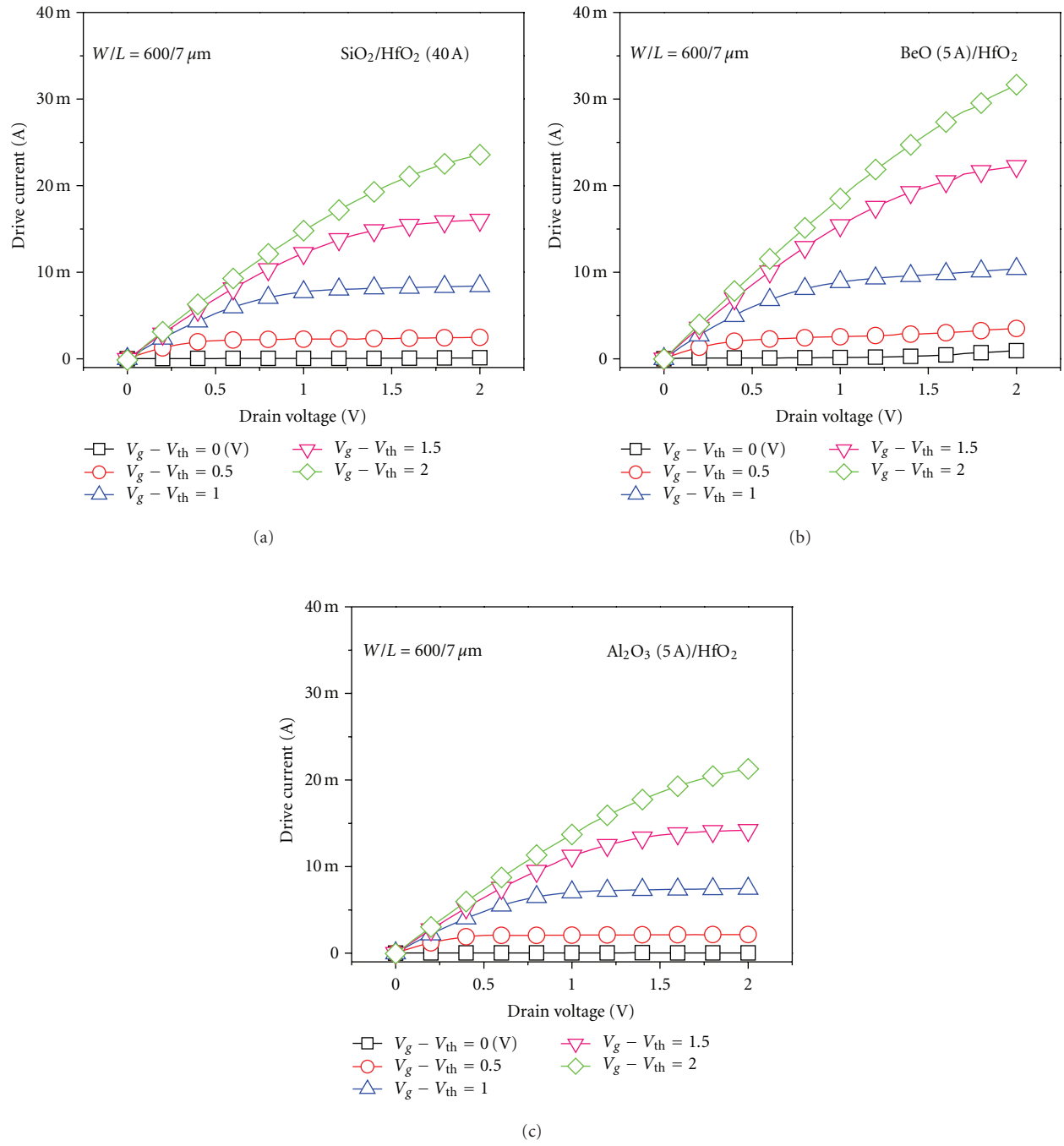

FIGURE 9: $I_d - V_d$ characteristics of three gate stacks. BeO IL shows significant increased drive current compared to SiO_2 and Al_2O_3 IL gate stacks.

where Φ_{ms}, Q_i, Q_d, and ϕ_F are the work function differences between the metal and semiconductor ("−" value), interface charge ("+" value), depletion charge ("−" value) for the n-channel, and energy differences between the intrinsic energy level and Fermi energy level (+) for the n-channel, $\phi_F = (E_i - E_F)/q$. If we assume that Φ_{ms}, Q_d, and ϕ_F are the same for all gate stacks because the only difference is interfacial layer, then the positive shift of V_{th} of the BeO/HfO_2 stack is due to the less positive interface charges between BeO and the Si substrate. The fewer fixed charges in BeO layer may contribute to the fewer interface charges [10].

In Figure 9, the BeO/HfO_2 stack shows around 34% higher drive current (31.67 mA) at $V_d = 2$ V & $V_g - V_{th} = 2$ V than the SiO_2/HfO_2 stack (23.56 mA) and Al_2O_3/HfO_2 stack (21.28 mA). Only 5 Å BeO insertion between high-k and Si channel makes the drive current much improved. There is some reduction of drive current with the IL thickness increase for both the Al_2O_3/HfO_2 and BeO/HfO_2

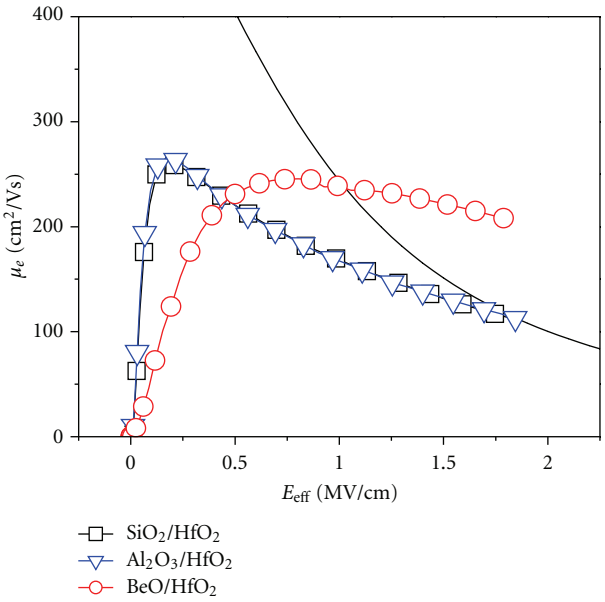

FIGURE 10: Effective channel mobility of NMOSFETs with three gate stacks.

gate stacks, but it is more significant on Al_2O_3/HfO_2 stack. It may be due to the less native interfacial oxide (SiO_2) growth for Al_2O_3/HfO_2, stack. Figure 10 illustrates the effective channel electron mobility using the split capacitance-voltage (C-V) method. The BeO/HfO_2 stack shows a 42% higher effective field (E_{eff}) mobility (238 cm^2/Vs) than SiO_2/HfO_2 (167 cm^2/Vs) and Al_2O_3/HfO_2 (166 cm^2/Vs) at E_{eff} = 1 MV/cm. It may require further investigation to confirm and explain these results. The electron mobility in SiO_2/HfO_2 and Al_2O_3/HfO_2 are fast-saturated to the universal trend, likely due to the thick SiO_2 interfacial layer grown during S/D activation. If the SiO_2 interfacial layer is thinner, the peak electron mobilities of the HfO_2 gate stack will decrease significantly [16]. In atomic configuration, physical roughness difference between amorphous Al_2O_3 and crystalline BeO is similar, but in electronic configuration, the electropotential roughness between them is quite different. In terms of electrostatic potential roughness, the two-dimensional ordered arrays of atoms on a crystalline surface generally give atomic scale surface height fluctuation, which exhibits low electrostatic potential roughness [17]. In a previous study, we demonstrated that ALD BeO on Si grows almost epitaxially [7], thereby may improve surface electro-potential roughness and high field electron mobility.

In this work, a BeO (IL)/HfO_2 gate stack was investigated and systematically compared to a SiO_2/HfO_2 gate stack. Inserting an ALD BeO IL between the Si channel and high-k gate dielectric enhances high field carrier mobility and improves MOSFET parameter and reliability characteristics while maintaining a similar EOT. Excellent BeO properties, such as a high energy bandgap, efficient oxygen diffusion barrier, and high crystallinity, improve the charge trapping, the suppression in EOT increase during S/D activation, and MOSFET performance, thus imparting significant advantages to MOS devices with a BeO IL.

Acknowledgments

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Research Article

Gate Stack Engineering and Thermal Treatment on Electrical and Interfacial Properties of Ti/Pt/HfO_2/InAs *p*MOS Capacitors

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Effects of gate stack engineering and thermal treatment on electrical and interfacial properties of Ti/Pt/HfO_2/InAs metal insulator semiconductor (MIS) capacitors were systematically evaluated in terms of transmission electron microscopy, energy dispersive X-ray spectroscopy, current-voltage, and capacitance-voltage characterizations. A 10 nm thick Pt metal effectively suppresses the formation of interfacial oxide, TiO_2, between the Ti gate and HfO_2 gate dielectric layer, enhancing the gate modulation on the surface potential of InAs. An *in situ* HfO_2 deposition onto the *n*-InAs channel with an interfacial layer (IL) of one-monolayer InP followed by a 300°C post-metal-anneal produces a high-quality HfO_2/InAs interface and thus unravels the annoying Fermi-level pinning, which is evidenced by the distinct capacitance dips in the high-/low-frequency *C-V* characteristics. The interface trap states could be further suppressed by replacing the InP IL by an As-rich InAs, which is substantiated by a gate leakage reduction and a steep voltage-dependent depletion capacitance.

1. Introduction

Motivation to study low band-gap InAs and InSb channels for next-generation metal oxide semiconductor (MOS) transistors is strong in light of their superior carrier mobility [1] and established epitaxy techniques [2, 3] among other emerging technologies such as carbon nanotube and graphite. However, the progress of realizing high-performance InAs and InSb MOS transistors has been impeded by the stringent restraint on thermal budget as well as the lack of robust gate dielectrics and suitable surface treatments for unraveling annoying Fermi-level pinning [4] at the oxide/semiconductor interface. Recently encouraging experimental demonstrations of high-*K* gate dielectrics (Gd_2O_3, Al_2O_3, and HfO_2) on GaAs [5–7], InP [8], and InAs [9–11] channels using atomic-layer deposition (ALD) techniques have shed lights and attracted tremendous attentions on this venerable subject. In spite that various chemical and plasma surface treatments [12–14] have been proposed for annihilating surface states of III-V compound semiconductors, it still remains elusive how to produce a clean and well-passivated channel surface for subsequent high-quality gate dielectric growth. The most practical and promising approach for the surface preparation of III-V channels appears to be the *in situ* growth of gate dielectrics on channels.

In this paper, the authors report the interfacial and electrical properties of Ti/Pt/HfO_2/InAs *p*MOS capacitors, in which a high-*K* gate dielectric, HfO_2 was grown on an *n*-InAs epitaxial layer without breaking vacuum by means of the integration of a molecular beam epitaxy system (Riber-32 MBE) with an atomic layer deposition system (Picoson R-100 ALD). In order to prevent thermal evaporation of InAs, all the device fabrication processes were kept below 300°C. Both Ti and Pt metals were evaluated for the gate materials. The interfacial layer effect arising from one-monolayer InP or As-rich InAs between HfO_2 and InAs channel, the deposition conditions of HfO_2, and post-metal-anneal (PMA) processes were systematically studied for improving the interfacial and electrical properties of HfO_2/InAs *p*MOS capacitors.

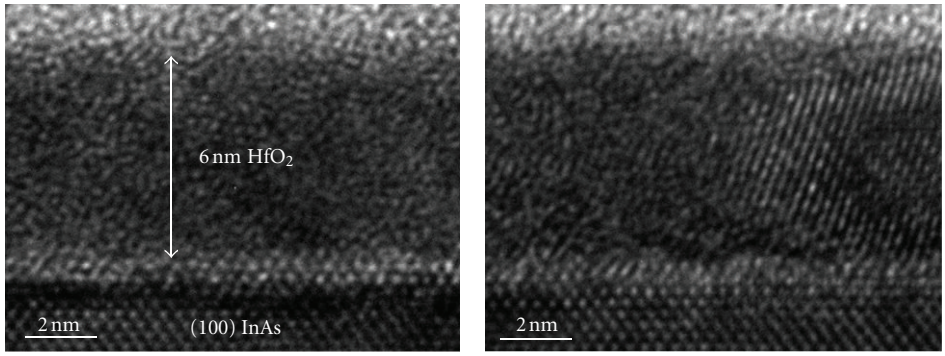

Figure 1: CTEM images of HfO_2 *in situ* deposited on InP/InAs channel at (a) 200°C and (b) 300°C. Abrupt and native oxide free interface provides a promising interface for MOS applications.

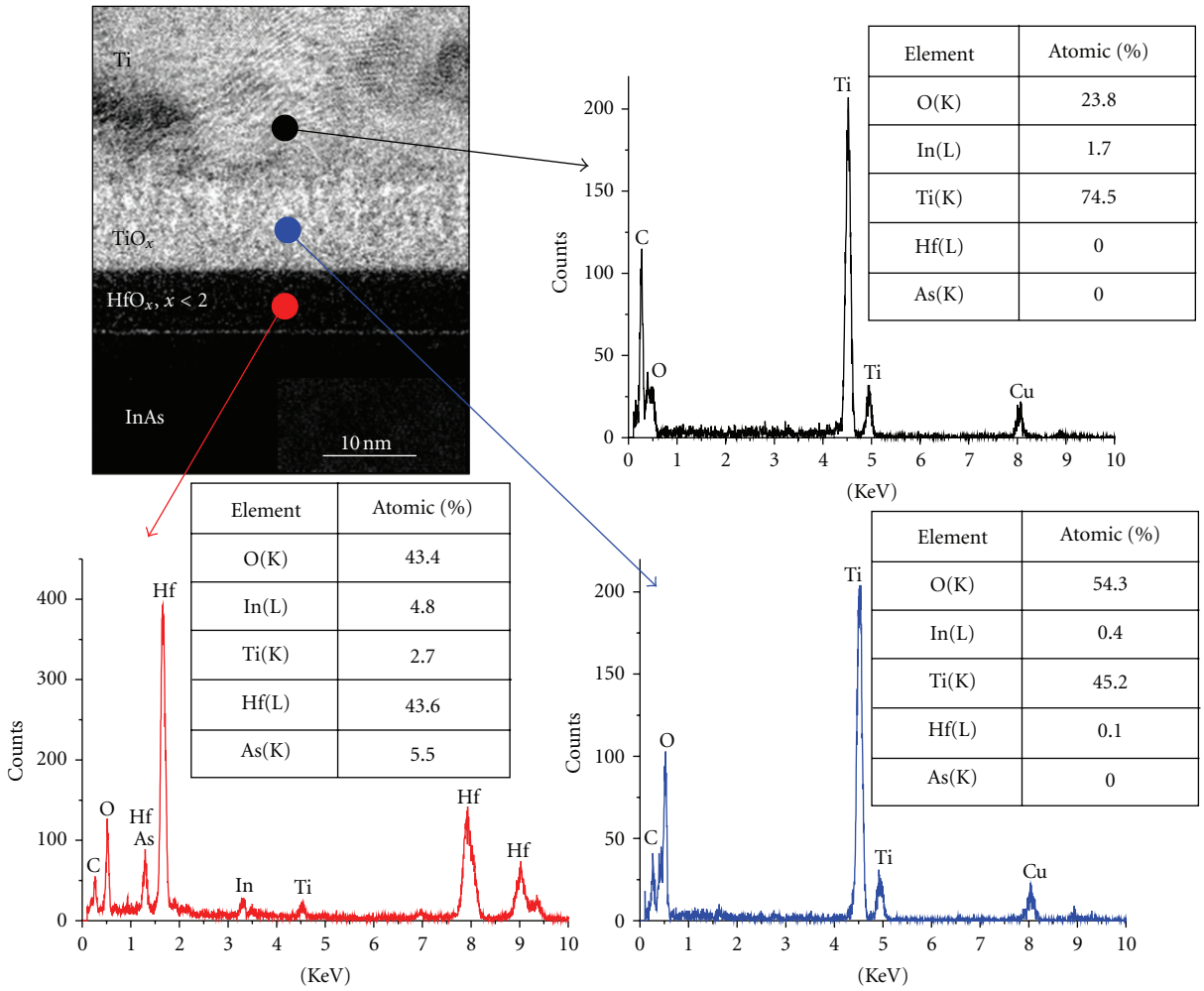

Figure 2: Energy dispersive X-ray spectroscopy (EDX) analysis obtained from various locations of Ti/InP/InAs MOS structure. EDX analysis reveals that an interfacial TiO_x ($x \sim 1.2$) and Hf-rich oxide were formed after Ti deposition onto HfO_2/InP/InAs structure.

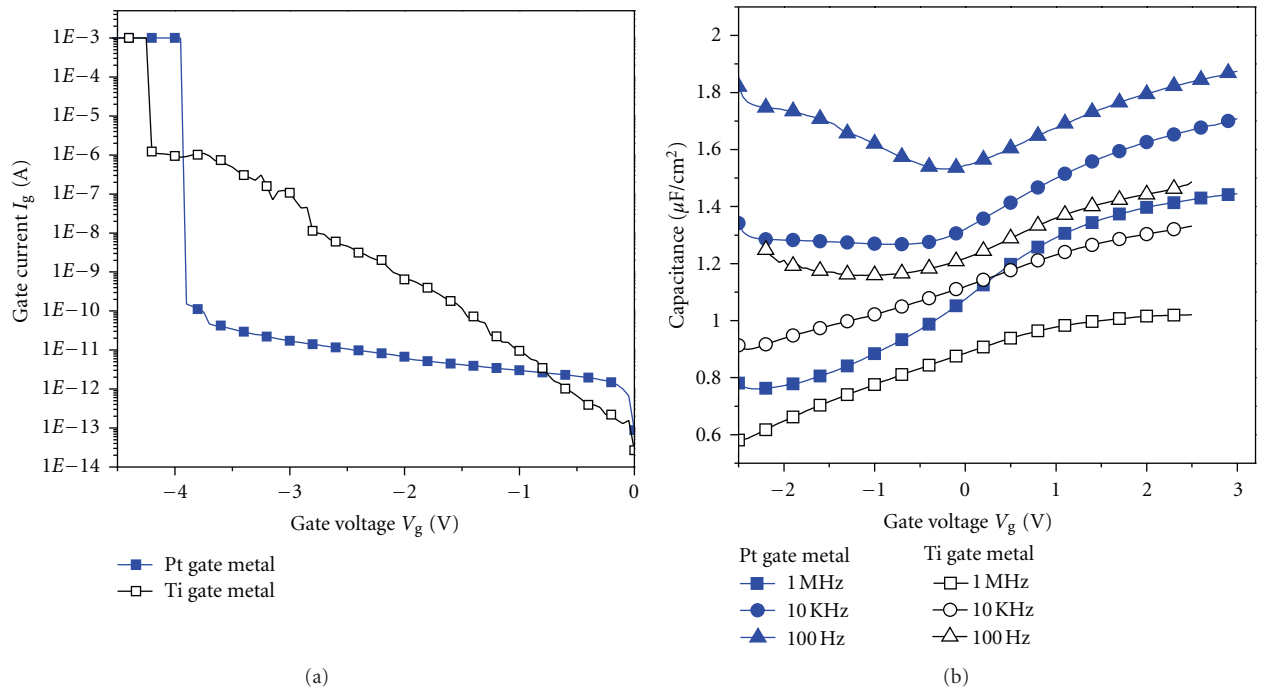

FIGURE 3: (a) I-V and (b) C-V characteristics of HfO_2/InP/InAs MOS capacitors of $100 \times 100\,\mu m^2$ with Ti and Pt gate metal, respectively.

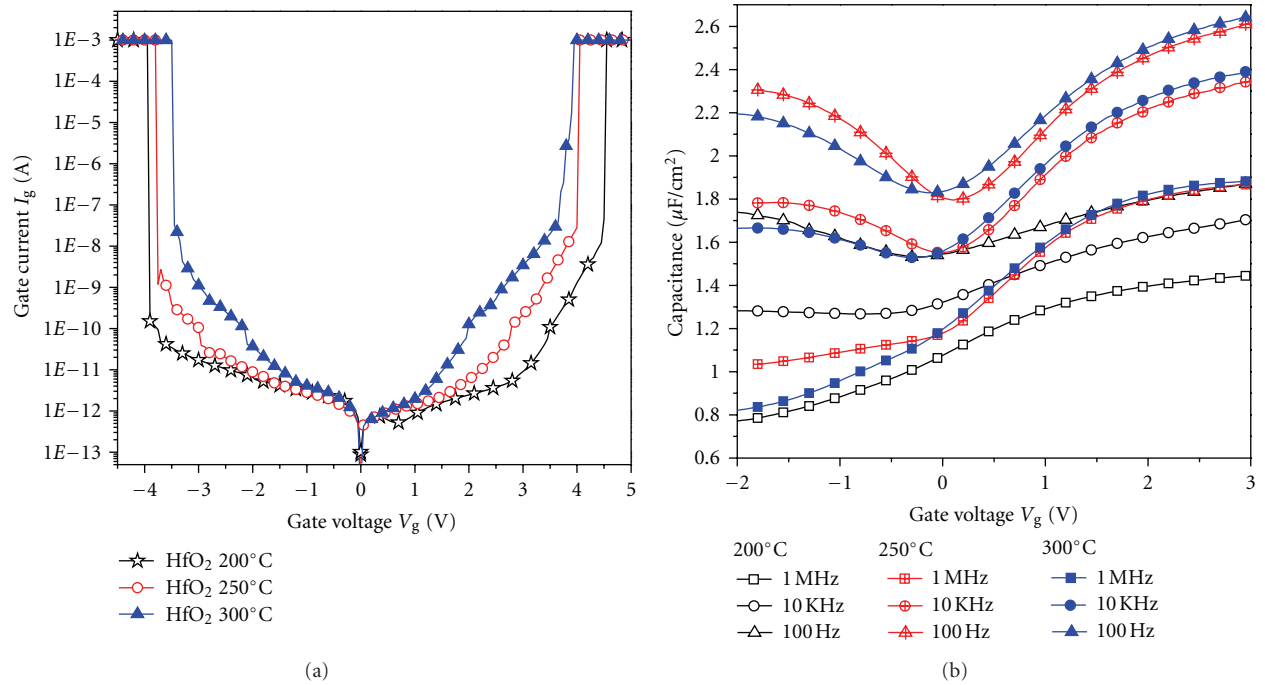

FIGURE 4: (a) I-V and (b) frequency-dependent C-V characteristics of Pt/HfO_2/InP/InAs MOS capacitors in which HfO_2 was deposited at 200, 250, and 300°C, respectively.

2. Experimental

The fabrication of HfO_2/InAs MOS capacitors started with a 2″ (100) n-InAs substrate doped with Si [$(2–5) \times 10^{17}\,cm^{-3}$], followed by an epitaxial growth of a 200 nm thick n-InAs channel layer uniformly doped with Si in a concentration of $2 \times 10^{17}\,cm^{-3}$ and an one-monolayer InP or As-rich InAs IL on the top of InAs channel. After transferring the sample from the MBE growth chamber to ALD system through a high-vacuum

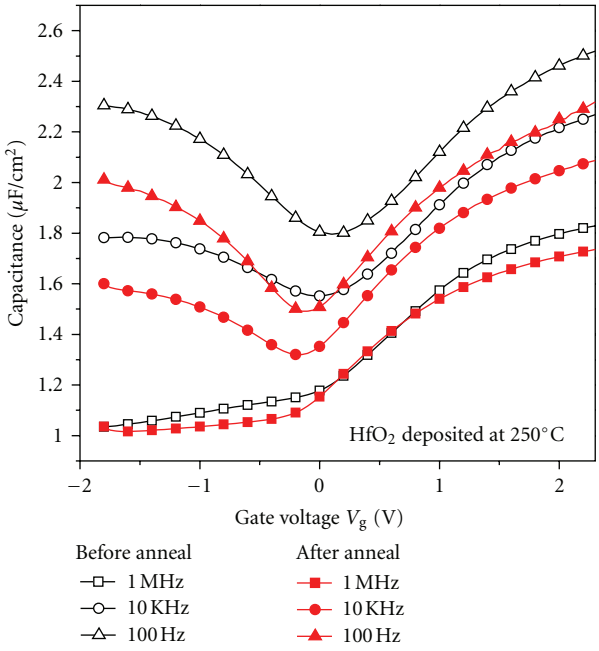

FIGURE 5: Frequency-dependent C-V characteristics of Pt/HfO_2/InP/InAs MOS capacitors in which HfO_2 was deposited at 250°C before and after a subsequent 300°C forming gas PMA.

chamber with a base pressure of 6×10^{-8} Torr, a 6 nm thick HfO_2 layer was deposited at 200-300°C using water vapor and tetrakis(ethylmethylamino)hafnium [TEMAH, $Hf[N(C_2H_5)(CH_3)]_4$] precursors. A 300 nm thick Ti or a 50 nm thick Pt was evaporated as gate materials followed by the gate definition either using photolithography and HF/H_2O_2 chemical etching or through a shadow mask. Finally, the fabrication of MOS capacitors was completed by the evaporation of a 100 nm thick Al onto the substrate as the back-gate electrode and a 300°C PMA for 30 min. The interfacial and structural properties of the Ti/Pt/HfO_2/InAs system were examined using high-resolution transmission electron microscopy (HRTEM) and energy dispersive X-ray spectroscopy (EDX). The current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the HfO_2/InAs MOS capacitors were characterized using Keithley-4200 and HP4284 semiconductor analyzers.

3. Results and Discussion

Figure 1 shows the cross-sectional TEM (CTEM) images of the gate stack of Ti/HfO_2/InP/InAs structure. The *in situ* growth of HfO_2 on an InP/InAs channel produces a native-oxide free and abrupt HfO_2/InP/InAs interface, indicating dangling bonds or surface states of InP/InAs are suppressed and providing a good interface for charge inversion under gate modulation. Additionally, there appears to be a 10–12 nm thick interfacial layer between a 6 nm thick HfO_2 layer and Ti-gate, and EDX analysis reveals that the chemical composition of the interfacial layer is TiO_x ($x \sim 1.2$) and the underlay hafnium oxide becomes a Hf-rich oxide (Figure 2), suggesting Ti catalytically releases oxygen from the stoichiometric HfO_2, forming a Hf-rich oxide, and the subsequent reaction of Ti and released oxygen generates TiO_x. The undesired interfacial TiO_x and Hf-rich oxide layers not only deteriorate the oxide integrity but also thicken the gate dielectrics thickness, which are evidenced by a high-gate leakage, a poor gate modulation on the surface potential of InAs channel but a slightly higher breakdown voltage as illustrated in the I-V and C-V characteristics (Figure 3).

An interesting finding that we have made through TEM observation is that a thin Pt barrier metal before Ti deposition effectively suppresses the formation of an interfacial oxide layer and retains the stoichiometry and high quality of HfO_2. The dielectric thickness of the Pt-gated MIS capacitor is 6 nm thick HfO_2, whereas the Ti-gated MIS capacitors have a gate oxide of 16–18 nm (10–12 nm TiO_x and 6 nm Hf-rich oxide). Although the thinner gate dielectric in the Pt-gated MIS capacitors sustains a smaller breakdown voltage than Ti-gated devices do, the reduction of gate leakage is more than 4 orders in magnitude as compared with the Ti-gated MIS capacitors. As a consequence, there appear a significant increase in the accumulation capacitance for a Pt-gated MIS diode and an enhanced gate modulation from C-V characteristics in Figure 3(b).

The gate-oxide integrity appears to be strongly dependent on the HfO_2 deposition temperature and the thermal treatment after metal patterning. Increasing the deposition temperature from 200 to 250°C not only enhances the accumulation capacitance because of an increase in the dielectric constant of HfO_2 from 11 to 15, but also improves the inversion capacitance as a consequence of a better HfO_2/InP/InAs interface. This is evidenced by a steep C-V transition in the depletion regime and a distinct capacitance dip when gate voltage modulates the surface potential of the InAs channel from depletion to inversion regimes (Figure 4). However, a higher HfO_2 deposition temperature at 300°C degrades the gate leakage and breakdown E-field accordingly, possibly originating from the crystallinity of HfO_2 transitioning from amorphous to polycrystalline phases from 200 to 300°C (Figure 1(b)). An additional 300°C PMA in H_2/N_2 ambient for 30 min further appears to reduce the dangling-bonds and annihilates the surface states at the HfO_2/InP/InAs interface, but also improves the frequency-dependence of the accumulation capacitance as a result of the dielectric constant dispersion (Figure 5). The above mentioned experimental results also suggests that the InAs epitaxial layer is of high quality and does not degrade after a long duration (45 min) of 300°C ALD and PMA process.

The interfacial properties and electrical characteristics of InAs MOS capacitors could be further improved by replacing the unrelaxed InP IL with a latticed match As-rich InAs IL, in spite that the bandgap of InAs (0.345 eV) is smaller than InP (1.344 eV). This is evidenced by a reduction of the gate leakage by one order in magnitude as shown in Figure 6(a). This is also substantiated by a steeper slope in the depletion region of the C-V characteristics in Figure 6(b). Suppressed surface states by As-rich IL and a high-thermal generation rate in narrow band-gap InAs [15] make the C-V curves

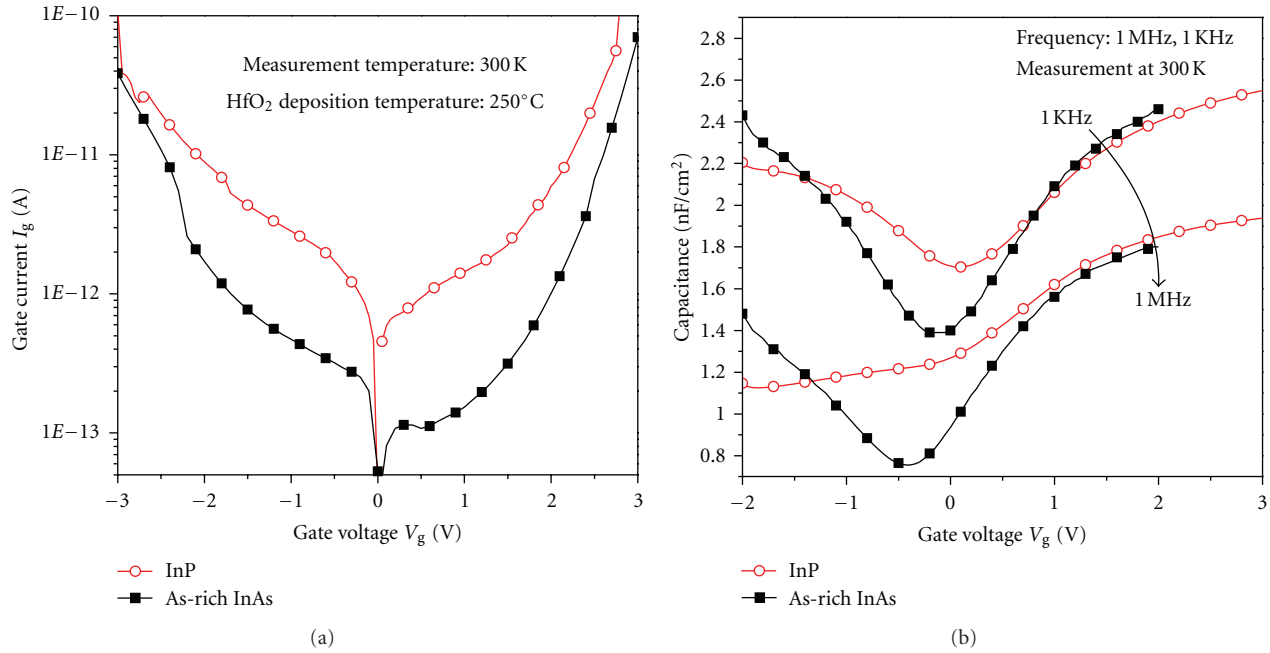

Figure 6: (a) I-V and (b) C-V characteristics of Pt/HfO_2/InAs MOS capacitors with respective InP or As-rich InAs interfacial layers.

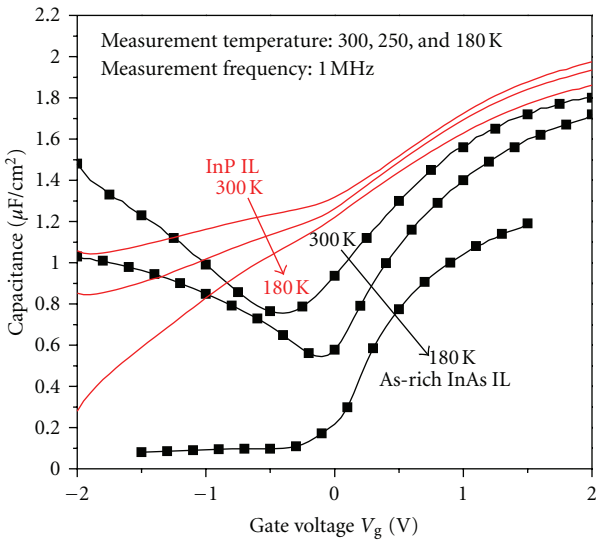

Figure 7: 1 MHz temperature-dependent C-V characteristics of InAs MOS capacitor with respective InP or As-rich interfacial layers.

measured at 1 MHz deviate from the conventional high-frequency C-V characteristics, in particular, at the inversion regime (Figure 7). For example, the inversion capacitances at 300 and 250 K are voltage dependent and getting close to the value of the gate oxide capacitance, instead of the effective capacitance of gate oxide capacitance in series with the depletion capacitance. Decreasing measurement temperature from 300 to 180 K decreases the thermal-generated carrier population and makes the inversion capacitance value restoring back to the one of typical high-frequency C-V characteristics. The extracted interface trap density (D_{it}) using a conductance method from the Pt/HfO_2/InAs MOS capacitors with InP and As-rich interfacial layer is 1.59×10^{13} and 7×10^{12} cm^{-2} eV^{-1}, respectively, which are comparable with reported data [9–11].

4. Conclusion

The *in situ* growth of HfO_2 on InAs channel produces an abrupt and oxide-free interface, which is an important prerequisite for high-performance InAs MOS devices. The interfacial and electrical properties of HfO_2/InAs MOS capacitors are strongly influenced by the gate metal, HfO_2 deposition temperature, the post-metal anneal, and interfacial control layer between HfO_2 and InAs channel. A Pt barrier metal effectively suppresses the formation of interfacial TiO_x oxide and thus significantly improves the gate leakage and insulating quality of the gate stack. The gate oxide integrity and the gate dielectric constant of HfO_2 could be further improved by a 250°C ALD deposition and a 300°C PMA treatment. An As-rich InAs IL further suppress surface states, evidenced by the reduction of gate leakage, and depletion/inversion capacitances.

Acknowledgments

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Research Article

The Improvement of Reliability of High-k/Metal Gate pMOSFET Device with Various PMA Conditions

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The oxygen and nitrogen were shown to diffuse through the TiN layer in the high-k/metal gate devices during PMA. Both the oxygen and nitrogen annealing will reduce the gate leakage current without increasing oxide thickness. The threshold voltages of the devices changed with various PMA conditions. The reliability of the devices, especially for the oxygen annealed devices, was improved after PMA treatments.

1. Introduction

High-k/metal gates are needed to continuous device scaling-down. However, threshold voltage instability and performance degradation are important problems for high-k devices [1]. The defect density in the interface of gate stack is the major cause for negative bias temperature instability (NBTI) as well as mobility degradation [1]. Oxygen vacancy is known to play an important role in threshold voltage variations [2] and is a significant defect in the HfO_2/Si system [3]. The influence of charge oxygen vacancies introduces a dipole offset between the gate metal and the substrate [4].

Post metallization annealing (PMA) is used to reduce the defects at the interface, such as fixed oxide charges, oxide trapped charges, and interface charges [5]. Previous work has demonstrated that oxygen vacancies can be passivated for device with noble metal gate by oxygen diffusion through the gate metal [6]. However, these suffer from high equivalent oxide thickness. In this work, we show that both oxygen and nitrogen can be diffused through thin TiN layer and passivate the oxygen vacancies without increasing the oxide thickness by using PMA with various temperatures. Negative bias instability for pFET is improved, especially for the oxygen annealed one.

2. Experimental

28 nm FET high-k/metal gate was formed on bulk Si. After interfacial SiO_2 layer/high-k and TiN deposition, TiN layer was then deposited with the thickness of 100∼200 Å. The fabrication process of the high-k metal gate last device was sketched in Figure 1. Some of the samples were annealed at 400°C and 450°C in oxygen or nitrogen ambient for several minutes, respectively.

The capacitance-voltage (C-V) curves were measured with an HP4280 precision LCR meter and the current-voltage (I-V) curves with an HP-4156B. After the basic electric measurements, the samples were then stressed by using a constant voltage of $V_{\text{stress}} = V_t - 1$. After stressing, the samples were measured again to find out the performance of reliability.

3. Results and Discussions

Figure 2 shows the C-V curves of the samples measured with 1 MHz. The extracted EOT for all samples is about 13 Å. The merged C-V curves at low voltage for all samples indicate that there is no extra growth in oxide thickness even after 450°C PMA in O_2 ambient. Figure 3 shows the I_G-V_G curves for all samples. It could be found that the sample without

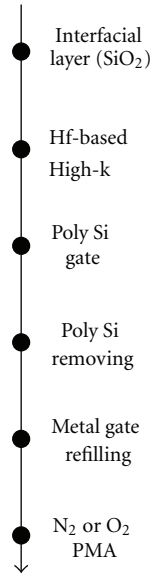


FIGURE 1: The fabrication process of the high-k metal gate last device.

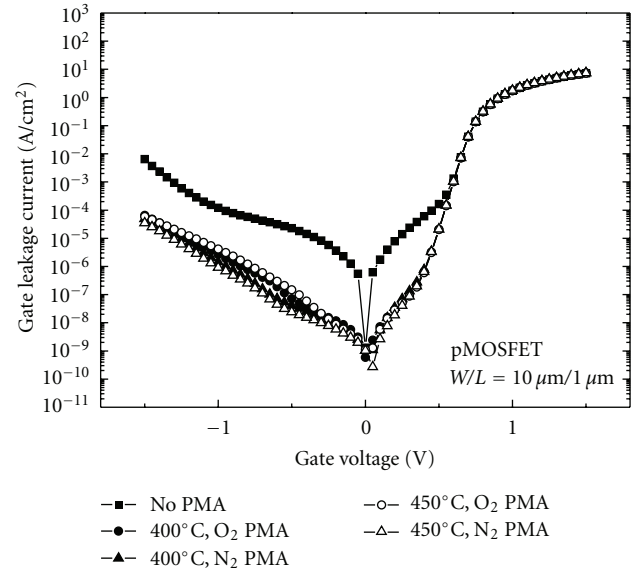


FIGURE 3: The I_G-V_G curves for samples with various PMA treatments.

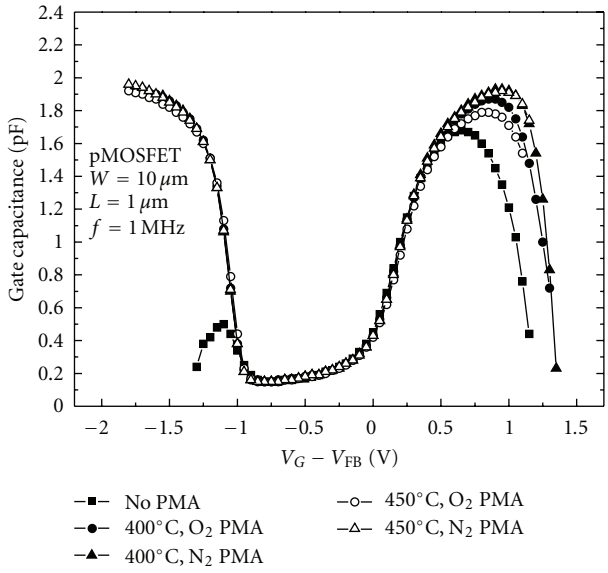


FIGURE 2: The C-V curves with V_{FB} normalization.

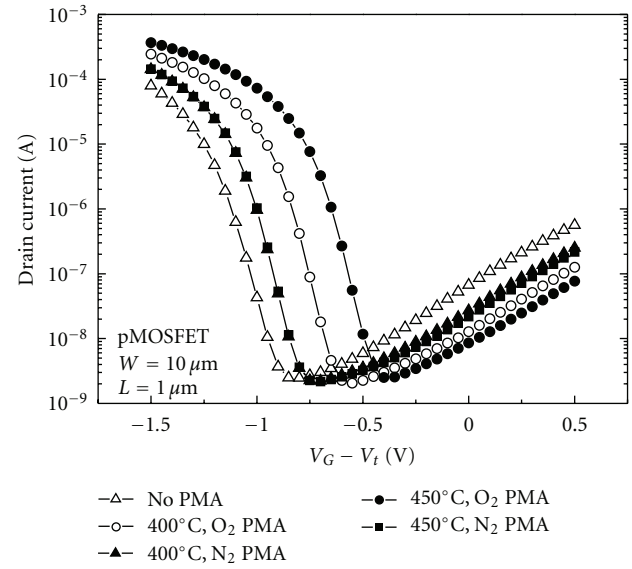
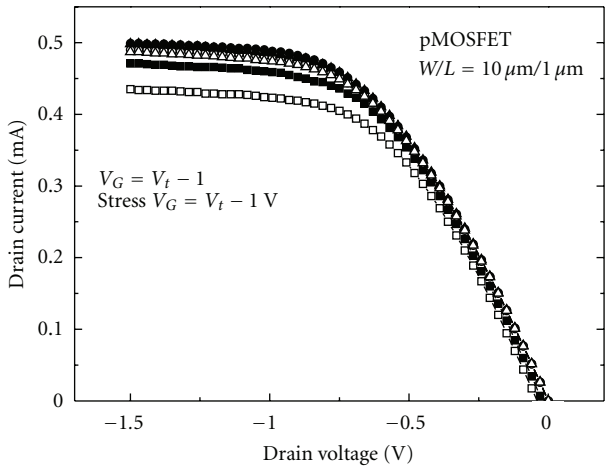


FIGURE 4: The I_D-V_G curves for samples with various PMA treatments.

PMA shows an obviously huge gate leakage current than other samples. On the other hand, the gate leakage current reduced after PMA in all conditions. The reduction of gate leakage current is because of the defects passivation in high-k/Si interface [7].

Figure 4 shows the I_G-V_G curves for samples with various PMA treatments. It could be observed that the device without annealing shows the most negative threshold voltage due to the existence of charged oxygen vacancy, and the threshold voltage shifts positiveward after PMA treatment. Both the threshold voltages are similar with various annealing temperatures for the nitrogen-annealed devices. On the other hand, the amount of threshold voltage shift of oxygen-annealed device is strongly dependent on the annealing temperature. The positive shift of threshold voltage might be due to the passivation of oxygen vacancies in the interfacial layer (IL) region [6]. Both the oxygen and nitrogen could be permeated through the TiN region and reach the IL region although TiN is commonly used as diffusion barrier. The phenomenon is suggested to reduce the threshold voltage of pMOSFET for the high-performance application.

Figure 5 shows the I_D-V_D curves with various PMA conditions before and after constant voltage stress, and the amount of degradation of I_D was extracted and shown in



Square: W/G PMA
Circle: 400°C, O_2 PMA
Triangle: 400°C, N_2 PMA
Solid: before CVS
Open: after CVS

FIGURE 5: I_D-V_D curve of pMOSFET with various PMA conditions before and after constant voltage stress.

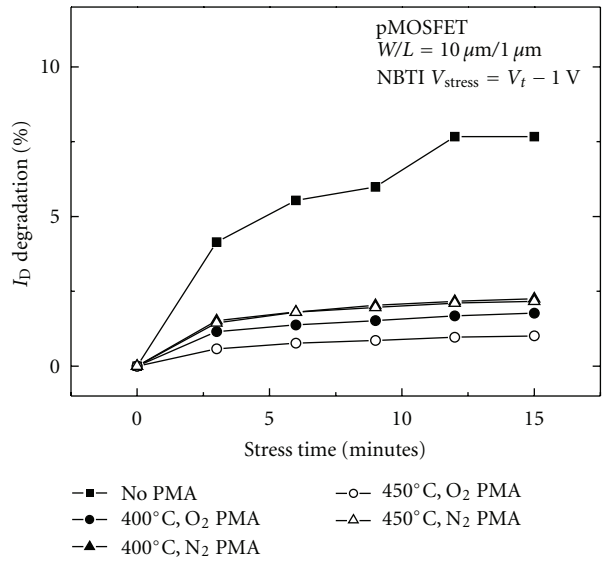


FIGURE 6: The extracted I_D degradation after constant voltage stress.

Figure 6. It could be observed that the device without PMA shows the worst device performance. On the other hand, the reliability is improved for devices with PMA treatment. As compared to the various PMA conditions, the oxygen devices with oxygen annealing show the better reliability than the device with oxygen annealing. The I_D degradation is suggested due to the breaking of passivated oxygen vacancies during stress. Compared to nitrogen, oxygen is believed to cause stronger bonding when passivating the dangling bonds of oxygen vacancies. As a result, the device with oxygen annealing shows the lowest I_D degradation.

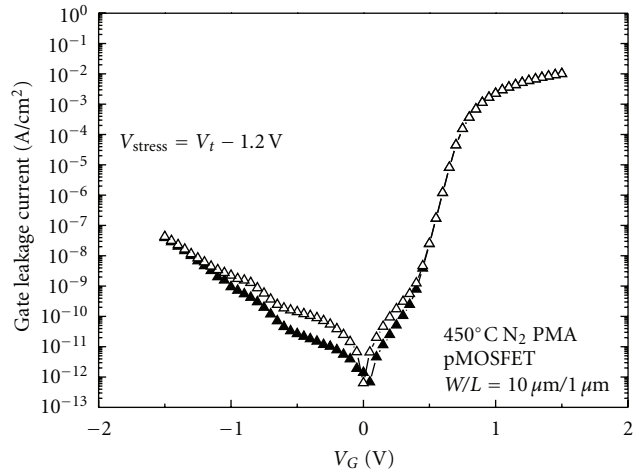


FIGURE 7: The I_G-V_G curves of 450°C, N_2 annealed sample before and after stress.

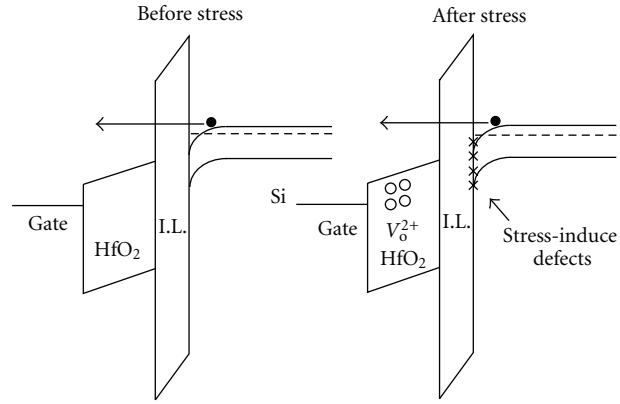


FIGURE 8: Band diagram of I_G-V_G curve in accumulation region.

In order to realize the mechanism of I_D degradation, the variation of gate leakage current before and after stress was investigated in this work. Figure 7 shows the I_G-V_G curves of samples annealed in N_2 ambient at 450°C before and after constant voltage stress. It could be found that the two curves overlap in the region of accumulation and strong inversion, and it divides in the region of depletion and weak inversion. The results could be explained using the following models as shown from Figure 8 to Figure 10. After applying a constant voltage stress, it is believed that some traps would be generated in both interface and high-k dielectric layer. When the device is biased to accumulation (see Figure 8), enough electrons would be injected from the substrate into the gate electrode by tunneling; as a result, the gate leakage current is independent of the generated traps. When the device is biased to depletion and weak inversion (see Figure 9), the gate leakage current includes two components: the generation holes and the gate-injected electrons. The stress-induced traps in the high-k dielectric layer would result in trap assistant tunneling from the gate

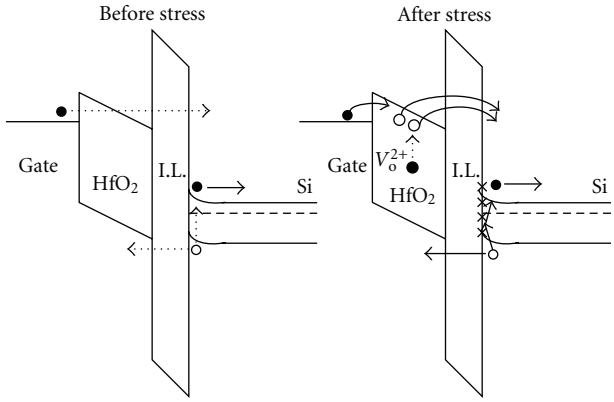


Figure 9: Band diagram of I_G-V_G curve in depletion and weak inversion region.

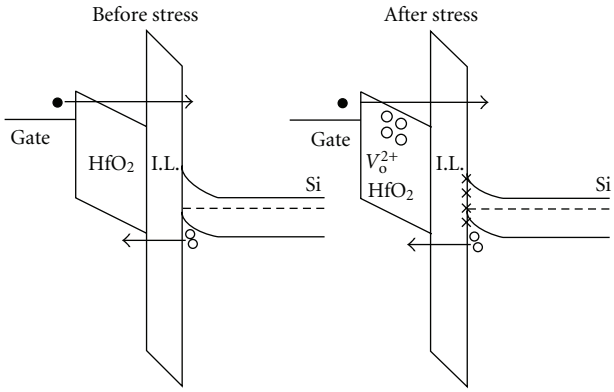


Figure 10: Band diagram of I_G-V_G curve in strong inversion region.

electrode, and the traps in the high-k/Si interface would enhance the generation holes. Both traps would increase the gate leakage current. In other words, more traps generated in both the gate dielectric layer and the interface would induce larger gate leakage current. As the electric field is large enough (see Figure 10), the electrons and holes would, respectively, pass through conduction band and valance band of the high-k layer. Therefore, the gate leakage current is independent of the stress-induced traps. From the above model, the gate leakage current variation is mainly attributed to both trap assistant tunneling and holes generation in depletion and weak inversion region. As shown in Figure 7, the devices with oxygen annealing have less variation of gate leakage current than those with nitrogen annealing. This could be explained that oxygen annealing has stronger bonding to passivate the dangling bonds of oxygen vacancies, which results in fewer traps generated during stress.

4. Conclusions

Postmetallization annealing was used in this work to improve the performance and reliability of the high-k/metal gate pMOSFET devices. The models show that the increase of gate leakage current after stress must be due to the traps generation in both high-k gate dielectric layer and high-k/Si interface. It is believed that oxygen would cause the stronger bonding than nitrogen as passivating the dangling bonds of oxygen vacancies. As the results show, the devices with oxygen annealing show the least I_D degradation and gate leakage current variation than the others.

Acknowledgments

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