Journal of Electrical and Computer Engineering

Advanced Power Electronic Converters and Power Quality Conditioning

Lead Guest Editor: Chi-Seng Lam
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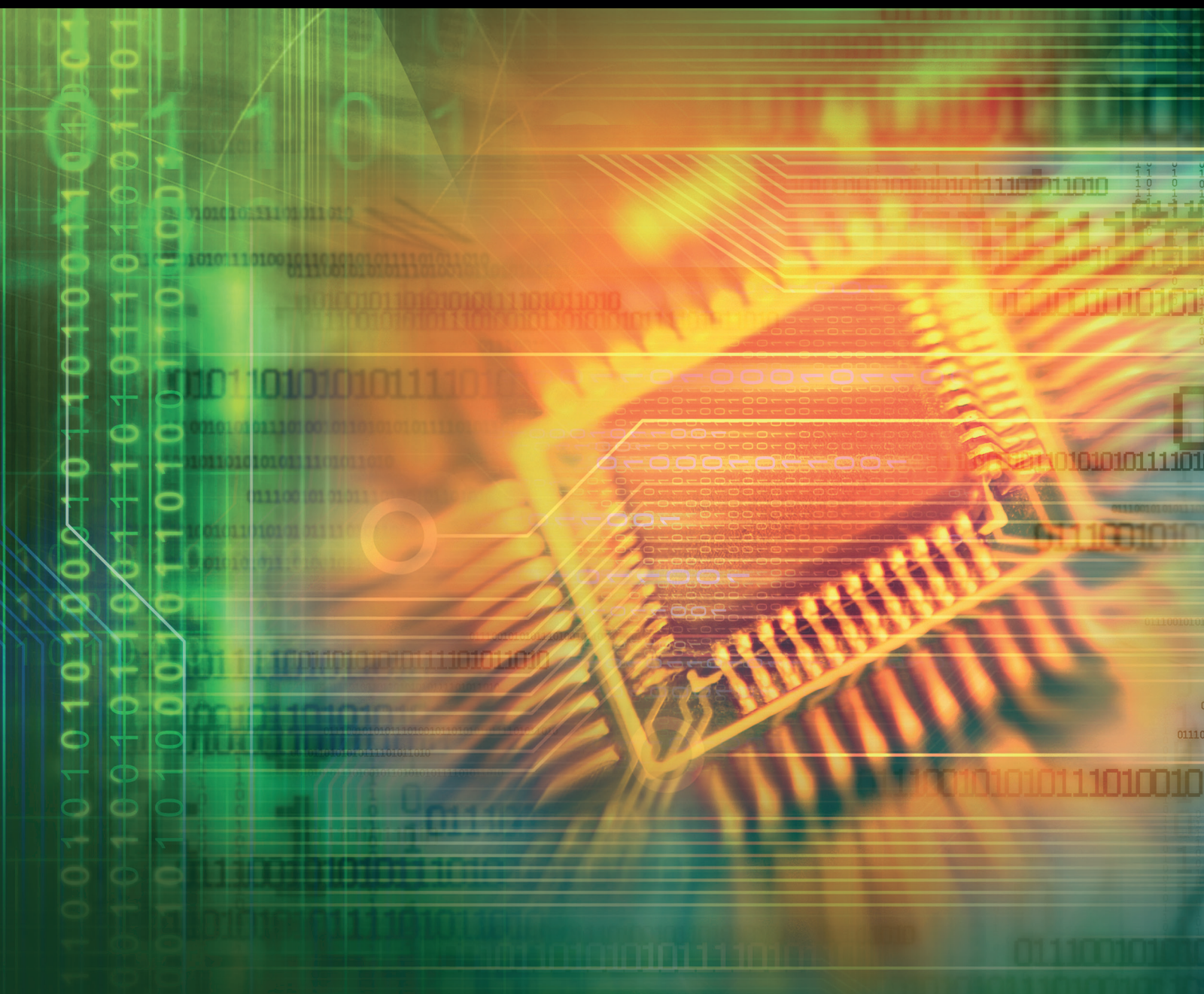

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Editorial Board

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Editorial

Advanced Power Electronic Converters and Power Quality Conditioning

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With the proliferation and increased use of power electronic devices (nonlinear loads) in adjustable speed drives (ASDs), arc furnaces, bulk rectifiers, power supplies, fluorescent lamps, elevators, escalators, large air conditioning systems, etc. and also rapid increase in renewable energy generation and railway electrification systems in grid or microgrids recently, the power quality (PQ) problems become more serious, especially for lower power factor, harmonic pollution, unbalanced current, neutral current, voltage sag, voltage swell, voltage fluctuation, and resonance problems, which strongly affect the performance, efficiency, and reliability of the grid or microgrids. Advanced PQ solutions, compensator topologies, detection methods, control algorithms, and PWM techniques are the key driven force to achieve the goal of power quality enhancement in power grid or microgrids.

The purpose of this special issue is to collect high-quality research articles as well as review papers on the recent theoretical, structure, control, and analysis advancement on PQ problems and their corresponding solutions in power grid, microgrids, and railway electrification system. This special issue has attracted the submission of many high-quality papers. After going through the peer-review process, six papers have been accepted and published.

In the paper entitled "Feedforward Harmonic Mitigation Strategy for Single-Phase Voltage Source Converter," Q. Zhong et al. present a harmonic analysis model of single-phase voltage source converters (SPVSCs) based on dynamic phasor (DP).With the model, the harmonics interaction between the ac side and the dc side can be analyzed, which reveals the generation mechanism of the harmonics in the SPVSC. Based on the mechanism, a feedforward harmonic mitigation strategy has been presented. The principle of the strategy is to add low-order harmonic signal to the PWM signals to reduce the harmonic current on the ac side. As the SPVSC has been widely used with the rapid development of distributed generations (DGs) in the grid or microgrid, this paper aims at mitigating the harmonic injection problem of the SPVSC.

In the paper entitled "A Novel Hybrid T-Type Three-Level Inverter Based on VPWM for PV Application," A. Tuluhong et al. compare different multilevel grid-connected inverter topologies for PV applications and propose a hybrid T-type inverter topology, which can reduce the harmonic content and the power loss of the converter and improve the conversion efficiency of the system. The space vector pulse width modulation (SVPWM) method is applied for the proposed topology. The results show that the proposed

structure is superior to the most widely used topology, i.e., the diode clamped and the T-type three-level circuits.

In the paper entitled "Analysis of Transient Voltage Stability in a Low Voltage Distribution Network Using SST for the Integration of Distributed Generations," S. Li et al. analyze the transient voltage stability issue of a low-voltage distribution network integrated with distributed generations (DGs) with and without using tertiary-structure solid-state transformers (SSTs). Although the SST control makes the load bus have better transient voltage stability, the DC bus voltage is easy to keep climbing continually when the short circuit occurs at the line side that is close to the SST input stage or the line disconnection occurs at any location of the line. If a battery energy storage station is installed, the transient voltage stability of DC bus and load bus will be improved effectively and guarantee the system safety.

In the paper entitled "A Double Update PWM Method to Improve Robustness for the Deadbeat Current Controller in Three-Phase Grid-Connected System," L. Yang et al. propose a double-update PWM method for the deadbeat current controller in three-phase grid-connected systems. It not only effectively decreases the grid current distortion and control delay but also improves the system stability and dynamic response speed due to reducing the characteristic root equation order of the closed-loop transfer function. The influence of the filter inductance deviation coefficient on the system performance is analyzed. Considering the system stability and dynamic response, the optimal range of the control parameters is acquired.

In the paper entitled "Shunt Active Power Filter Based on Proportional Integral and Multi Vector Resonant Controllers for Compensating Nonlinear Loads," S. Ye et al. propose a control algorithm based on PI and multi vector resonant (VR) controllers to control shunt active power filter (SAPF). Through detailed analysis on the frequency response characteristic of the current closed loop, the PI and VR controller can compensate the harmonic currents with zero steady-state error, negligible phase delay, and good dynamic performance. Under the synchronous reference frame, the proposed method is simple to compensate the harmonic, which reduces the computation and is better adapted to the frequency fluctuation.

In the paper entitled "Review and Selection Strategy for High-Accuracy Modeling of PWM Converters in DCM," Y.-J. Mao et al. review, study, and compare the two most general and popular small signal modelling methods: state-space averaging (SSA) and circuit averaging (CA) for various DC-DC converters operating in the discontinuous conduction mode (DCM). The authors also streamline the general model deriving processes, such that their corresponding DCM small-signal models can be easily determined. Finally, a selection strategy for a high-accuracy modelling method for different DC-DC converters operating in DCM is provided, and it is beneficial for designing a more accurate DCM closed-loop controller for DC-DC converters, thus achieving better stability and transient response.

We believe that the papers appearing in this special issue provide a good contribution and representation of significant research topics in the field of power electronics converters and also power quality conditioning.

Conflicts of Interest

The editors declare that there are no conflicts of interest regarding the publication of this special issue.

Acknowledgments

We would like to thank the authors for their contributions and the reviewers for their competent and timely work for this special issue.

Chi-Seng Lam
Yongheng Yang
Qing Zhong
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Review Article

Review and Selection Strategy for High-Accuracy Modeling of PWM Converters in DCM

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Among various modeling methods for DC-DC converters introduced in the past two decades, the state-space averaging (SSA) and the circuit averaging (CA) are the most general and popular exhibiting high accuracy. However, their deduction approaches are not entirely equivalent since they incorporate different averaging processes, thus yielding different small signal transfer functions even under identical operating conditions. Some research studies claimed that the improved SSA can obtain the highest accuracy among all the modeling methods, but this paper discovers and clearly verifies that this is not the case. In this paper, we first review and study these two modeling methods for various DC-DC converters operating in the discontinuous conduction mode (DCM). We also streamline the general model-deriving processes for DC-DC converters, and test and compare the accuracy of these two methods under various conditions. Finally, we provide a selection strategy for a high-accuracy modeling method for different DC-DC converters operating in DCM and verified by simulations, which revealed necessary and beneficial for designing a more accurate DCM closed-loop controller for DC-DC converters, thus achieving better stability and transient response.

1. Introduction

A PWM DC-DC converter operates either in the continuous conduction mode (CCM) or in the discontinuous conduction mode (DCM). For small inductances or light loads, DCM operation is occasionally unavoidable in DC-DC converters, their design being intentionally in DCM to reduce both the inductor's size and the switching frequency. Then, it is necessary to develop a modeling analysis for the DC-DC converter operation in DCM to design a closed-loop controller. In previous works [1–22], various small signal modeling methods of PWM DC-DC converters in CCM and DCM are proposed, where different modeling methods provide either an analytical equation or an equivalent circuit and can be categorized as reduced-order or full-order models, as summarized in Table 1.

Among these small signal modeling methods, the improved state-space averaging (SSA) and the circuit averaging (CA) are the latest to present, with high accuracy, an analytical equation, and an equivalent circuit, respectively. The improved SSA method [6] claims that it has the highest accuracy among all the other modeling methods and can be applied to any circuit composed by inductors and capacitors. But, this conclusion is only proven and verified in a boost converter under specific operating conditions [6]. Besides, this may not hold in other DC-DC converters and under different operating conditions. Moreover, Zeng et al. [13] used the CA method from [5] to deduce the small signal model of a KY converter, but when applying the improved

Table 1: Summary of small signal modeling methods.

Method name	Order	Model type
Conventional state-space averaging (SSA) [1]	Reduced order (low accuracy)	Analytical equation
Converter cell [2]	Reduced order (low accuracy)	Equivalent circuit
Full-order SSA [3, 8, 11, 12, 20]	Full order (high accuracy)	Analytical equation
Circuit averaging (CA) [4, 5, 8–10, 13, 14, 17–19, 21, 22]	Full order (high accuracy)	Equivalent circuit
Improved SSA [6, 7, 15, 16]	Full order (high accuracy)	Analytical equation

SSA method to the same case, the CA method yields a better modeling accuracy under some conditions that are discussed in this paper. Contradictions met in CA and SSA methods motivate further analysis and retesting their accuracy in various DC-DC converters under different operating conditions in DCM, in order to derive a selection criterion that allows higher accuracy in the small signal modeling method.

Also, the rather complicated (and not general) original derivation processes of the CA and the improved SSA methods, in which the whole small signal model derivation process should be repeated whenever the DC-DC circuit topology changes, whenever the DC-DC circuit topology changes, leads to unnecessary and time-consuming efforts. Then, another motivation for this paper is to generalize the whole derivation process to attain a general and intuitive model-deriving solution.

The main contributions of this paper are as follows:

(1) To propose and deduct a general and intuitive derivation process of the improved SSA and CA modeling methods for different DC-DC converters, such that their corresponding DCM small signal models can be easily determined.

(2) To study, retest, and compare, through simulations, the accuracy of the improved SSA and CA modeling methods for various DC-DC converters under different operating conditions. Since most of the previous works are either based on the improved SSA or CA, they lack a detailed comparison among them.

(3) To propose a selection strategy of the DCM small signal modeling method in order to obtain high accuracy for different DC-DC converters under different operating conditions.

This paper contributes significantly to the design of a stable and fast transient response DCM closed-loop controller for different DC-DC converters. Section 2 presents the DC analysis of different DC-DC converters in DCM. Section 3 introduces two small signal relationship calculation methods based on the large-signal equation. Section 4 discusses the general DCM large-signal and small signal modeling deduction based on the improved SSA method applied to different DC-DC converters. Then, Section 5 determines the general DCM large-signal and small signal modeling deduction based on the CA method. Section 6 compares the simulation results of the small signal modeling obtained through the improved SSA and the CA methods. Section 7 presents a selection strategy of the DCM small signal modeling for different DC-DC converters. Finally, the conclusions are drawn in Section 8.

2. DC Analysis of DC-DC Converters in DCM

In the discussion hereafter, if we use the capital letter X to denote the averaged value of a specific variable in one switching frequency (DC value), then the lowercase letter x denotes its large-signal value and $\hat{x}$ denotes its small signal value. The relationship between these three variables is [10]

$$x = X + \hat{x}. \tag{1}$$

2.1. DCM Operation. The DCM operation of the DC-DC converters consists of three intervals. Here, we use D_1, D_2, and D_3 to denote the duty ratio of each interval, respectively, and T_s denotes the switching period. Figure 1 shows the inductor current, i_L, waveform of the DC-DC converters operating in DCM [10].

For a typical DC-DC converter, i_L starts to rise during the charging of the inductor L and begins to drop while the L is discharging. In this paper, we use V_{on} (charging) and V_{off} (discharging) to denote the voltage across the L in the first and the second intervals, respectively. From Figure 1, we can obtain

$$I_{pk} = \frac{V_{on}}{L} D_1 T_s, \tag{2}$$

where I_{pk} denotes the peak value of inductor current i_L, D_1 denotes the duty ratio of charging interval, and T_s denotes the switching period. From Figure 1, the relationship between the peak value (I_{pk}) and average value (I_L) of the inductor current can be expressed as

$$\frac{1}{2} I_{pk} (D_1 + D_2) T_s = I_L T_s, \tag{3}$$

where I_L denotes the average value of the inductor current i_L while T_s and D_2 denotes the duty ratio of the discharging interval. From Figure 1,

$$\frac{V_{on}}{L} D_1 T_s = \frac{-V_{off}}{L} D_2 T_s = I_{pk}. \tag{4}$$

Equation (4) yields the following

$$D_2 = -\frac{V_{on}}{V_{off}} D_1, \tag{5}$$

where V_{on} (charging) and V_{off} (discharging) denote the voltage across the L in the first and the second intervals,

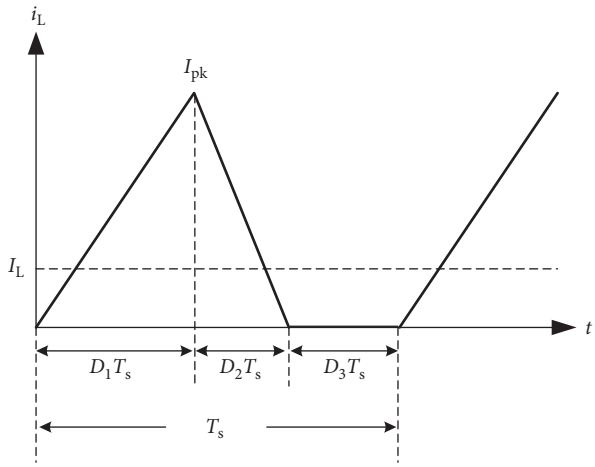


Figure 1: Inductor current of DC-DC converters operating in DCM.

respectively. Considering (2), (3), and (5), I_L can be expressed as

$$I_L = \frac{D_1^2 T_s V_{on}(V_{off} - V_{on})}{2LV_{off}}. \quad (6)$$

2.2. DC Parameters Calculation for Different DC-DC Converters in DCM. Before we derive the small signal model, some DC parameters of the circuit operating in DCM need to be calculated beforehand. Figure 2 shows the four DC-DC converters that will be studied throughout this paper; they are the buck converter, the boost converter, the buck-boost converter, and the KY converter [23], where v_i/i_i and v_o/i_o represent the input and output voltage/current of the converter, respectively, and L represents the inductor, D the diode, S the switch, C the output capacitor, R the loading, C_f the flying capacitor, i_L the inductor current, i_D the diode current, and i_S the switch current. As the equivalent series resistance (ESR) for the passive components are usually small due to high Q design, which are neglected in this paper for simplification. Thus, the left-hand plane zero caused by the ESR of the output capacitor C will not present in the small signal transfer functions for different DC-DC converters.

For calculating the necessary DC parameters of different DC-DC converters, we can just input different V_{on} and V_{off} into (5) and (6). For the buck converter, $V_{on} = V_i - V_o$ and $V_{off} = -V_o$; for the boost converter, $V_{on} = V_i$ and $V_{off} = V_i - V_o$; for the buck-boost converter, $V_{on} = V_i$ and $V_{off} = -V_o$, and for the KY converter, $V_{on} = 2V_i - V_o$ and $V_{off} = V_i - V_o$. On the other hand, using $M = V_o/V_i$ to denote the voltage gain, then D_2 and I_L can be calculated via (5) and (6), as summarized in Table 2.

For the DC relationship between D_1 and M, according to [4], the DC relationships among the inductor current i_L, the switch current i_S, and the diode current i_D are

$$I_S = \frac{D_1}{D_1 + D_2} I_L, \quad (7)$$

$$I_D = \frac{D_2}{D_1 + D_2} I_L. \quad (8)$$

For different DC-DC converters' configurations as in Figure 2, the output current $I_o = I_L$ for the buck and the KY converters and $I_o = I_D$ for the boost and the buck-boost converters. With the D_2 and I_L in Table 2 and the help of (7) and (8), the relationship between D_1 (expressed as $D_1^2 T_s R/2L$) and M can be calculated as presented in Table 2. These parameters are essential for the small-signal transfer function calculation as shown in Sections 4 and 5.

3. Calculation of the Small-Signal Relationship with the Proposed Differentiation Method

If f is a large-signal function of some variables x, y, and z, to attain the small-signal model of these variables, we can express them as the sums of DC and small signal components [10],

$$f = F + \hat{f}, \quad (9)$$

$$x = X + \hat{x}, \quad (10)$$

$$y = Y + \hat{y}, \quad (11)$$

$$z = Z + \hat{z}. \quad (12)$$

By neglecting the DC terms and the high-order small signal terms, we can realize the linear approximation. During the small signal calculation, the following approximation can be used:

$$\frac{1}{1 + \hat{x}} \approx 1 - \hat{x}. \quad (13)$$

For example, the large-signal inductor current of the buck converter given by Kazimierczuk [10] is shown in (14), which can also be given by referring to the expression of I_L in Table 2 and replacing all DC quantities with large-signal quantities. The basis for this replacement is that large-signal analysis is based on DC relationship of circuit variables [10, 15, 19, 21]:

$$i_L = \frac{d_1^2 T_s v_i (1 - m)}{2Lm}, \quad (14)$$

where m denotes the large-signal voltage gain and v_i denotes the small signal input voltage. Expressing the variables as the sums of DC and AC components as (9)–(12) do yield (15), after cancelling the DC components, the small signal expression of the inductor current $\hat{i}_L$ will become (16):

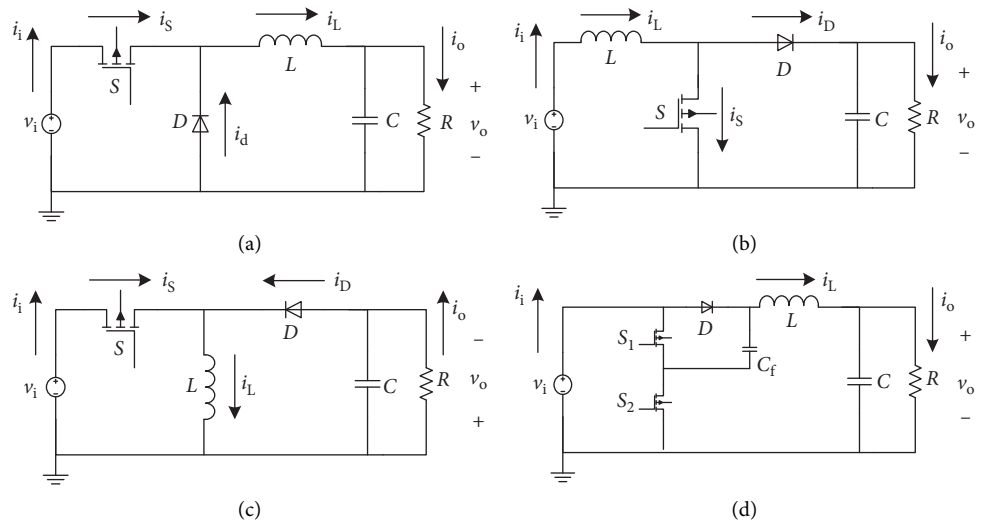


Figure 2: Circuit configuration of (a) buck, (b) boost, (c) buck-boost, and (d) KY converters.

Table 2: DC parameters for different DC-DC converters.

DC-DC converter	D_2	I_L	$(D_1^2 T_s R)/(2L)$
Buck	$((1-M)/M)D_1$	$(D_1^2 T_s V_i (1-M))/(2LM)$	$(M^2/(1-M))$
Boost	$(1/(M-1))D_1$	$(D_1^2 T_s V_i M)/(2L(M-1))$	$M^2 - M$
Buck-boost	$(1/M)D_1$	$(D_1^2 T_s V_i (1+M))/(2LM)$	M^2
KY	$((2-M)/(M-1))D_1$	$D_1^2 T_s V_i (2-M)/2L(M-1)$	$(M(M-1))/(2-M)$

$$I_L + \hat{i}_L = \frac{\left(D_1 + \hat{d}_1\right)^2 T_s \left(V_i + \hat{v}_i\right)(1 - M - \hat{m})}{2L(M + \hat{m})} \approx \frac{T_s\left(D_1^2 + 2D_1\hat{d}_1\right)\left(V_i + \hat{v}_i\right)(1 - M - \hat{m})(1 - (\hat{m}/M))}{2LM}, \tag{15}$$

$$\hat{i}_L = \frac{T_s\left[2D_1 V_i (1-M)\hat{d}_1 + D_1^2(1-M)\hat{v}_i - D_1^2 V_i \hat{m} - D_1^2 V_i (1-M)(\hat{m}/M)\right]}{2LM} = \frac{D_1 T_s V_i (1-M)}{LM}\hat{d}_1 + \frac{D_1^2 T_s (1-M)}{2LM}\hat{v}_i - \frac{D_1^2 T_s V_i}{2LM^2}\hat{m}. \tag{16}$$

However, the above deduction process is quite complicated and time-consuming. To simplify the analysis, we can utilize the calculation of the small signal perturbation as shown in Figure 3.

With a small variation of $\hat{x}$, the corresponding variation of $\hat{f}$ is also very small such that the value $\hat{f}/\hat{x}$ is equal to the derivative of f to x, thus yielding

$$\hat{f} = f'_x \hat{x} + f'_y \hat{y} + f'_z \hat{z}. \tag{17}$$

Following (17) and taking the derivative of (14) with respect to each variable, we can easily get

$$\hat{i}_L = \frac{D_1 T_s V_i (1-M)}{LM}\hat{d}_1 + \frac{D_1^2 T_s (1-M)}{2LM}\hat{v}_i - \frac{D_1^2 T_s V_i}{2LM^2}\hat{m}, \tag{18}$$

where the results in (16) and (18) are equivalent. In the following section, we will use the proposed differentiation method (17) to calculate the small signal relationship.

4. Improved State-Space Averaging Method for Large-Signal and Small Signal Modeling Deduction

In this section, the approach for deducing the DCM small signal models for different DC-DC converters by using the improved SSA method will be discussed.

4.1. General Large-Signal and Corresponding Small Signal Modeling Using the SSA Method. According to the conclusion from [10], the large-signal value relationship and the DC value relationship are identical. Then, (2) and (3) lead to the following large-signal duty ratio d_2:

$$d_2 = \frac{2Li_L}{v_{on} d_1 T_s} - d_1. \tag{19}$$

By applying the SSA to the inductor voltage and using (19), we get

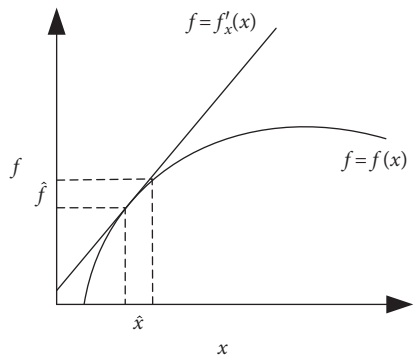


Figure 3: Small signal perturbation.

$$L\frac{di_L}{dt} = v_{on}d_1 + v_{off}d_2 = (v_{on} - v_{off})d_1 + \frac{2v_{off}Li_L}{v_{on}d_1T_s}. \quad (20)$$

Taking the derivative of (20) with respect to v_{on}, v_{off}, d_1, and i_L, which are variables in (20), and using (6), we will have the corresponding small signal model given by

$$L\frac{d\hat{i}_L}{dt} = \left(\frac{2V_{on} - V_{off}}{V_{on}}D_1\right)\hat{v}_{on} + \left(-\frac{V_{on}}{V_{off}}D_1\right)\hat{v}_{off} + 2(V_{on} - V_{off})\hat{d}_1 + \left(\frac{V_{off} - V_{on}}{I_L}D_1\right)\hat{i}_L. \quad (21)$$

Then, using the SSA to the capacitor current yields

$$C\frac{du_C}{dt} = i_o - \frac{u_C}{R}. \quad (22)$$

If $i_o = i_L$, and taking the derivative of (22), the corresponding small signal model becomes

$$C\frac{d\hat{u}_C}{dt} = \hat{i}_L - \frac{\hat{u}_C}{R}. \quad (23)$$

If $i_o = i_D$, then (8), (19), and (22) lead to

$$C\frac{du_C}{dt} = i_L - \frac{d_1^2T_sv_{on}}{2L} - \frac{u_C}{R}. \quad (24)$$

Finally, taking the derivative of (24), we obtain the corresponding small signal model as follows:

$$C\frac{d\hat{u}_C}{dt} = \hat{i}_L - \frac{D_1T_sV_{on}}{L}\hat{d}_1 - \frac{D_1^2T_s}{2L}\hat{v}_{on} - \frac{\hat{u}_C}{R}, \quad (25)$$

where (21), (23), and (25) are the three general equations for deducing the DCM small signal models of different DC-DC converters. Then, after input, the values of the inductor voltage drops during the charging (V_{on}) and discharging (V_{off}) cycles, as well as the DC parameters of each DC-DC converter from Table 2, into (21), (23), and (25), and the corresponding DCM small signal models can be deduced easily, as detailed next.

4.2. Buck Converter Small Signal Transfer Function. For the buck converter, $V_{on} = V_i - V_o$, $V_{off} = -V_o$, and $i_o = i_L$. Besides, Table 2 gives $I_L = (D_1^2T_sV_i(1-M))/(2LM)$ and $(D_1^2T_sR)/(2L) = (M^2)/(1-M)$, and substituting them into (21) and (23), gives

$$L\frac{d\hat{i}_L}{dt} = \left(\frac{2V_i - V_o}{V_i - V_o}D_1\right)(\hat{v}_i - \hat{v}_o) - \left(\frac{V_i - V_o}{V_o}D_1\right)\hat{v}_o + 2V_i\hat{d}_1 - \frac{V_i}{I_L}D_1\hat{i}_L, \quad (26)$$

$$C\frac{d\hat{u}_C}{dt} = \hat{i}_L - \frac{\hat{u}_C}{R}. \quad (27)$$

Let $\hat{v}_i = 0$, then (26) becomes

$$\left(sL + \frac{2LM}{D_1T_s(1-M)}\right)\hat{i}_L = \frac{1}{M^2 - M}D_1\hat{v}_o + 2V_i\hat{d}_1. \quad (28)$$

Further, if $u_c = v_o$, then (27) will be

$$\left(sC + \frac{1}{R}\right)\hat{v}_o = \hat{i}_L. \quad (29)$$

Considering (28) and (29) simultaneously, the transfer function (V_o over d_1) of the buck converter can be obtained as

$$\frac{\hat{v}_o(s)}{\hat{d}_1(s)} = \frac{2V_i}{s^2LC + s\left((L/R) + \left((2LCM)/\left(D_1T_s(1-M)\right)\right)\right) + \left(((2-M)D_1)/((1-M)M)\right)}. \quad (30)$$

4.3. Boost Converter Small Signal Transfer Function. For the boost converter, $V_{on} = V_i$, $V_{off} = V_i - V_o$, and $i_o = i_D$, and Table 2 gives $I_L = (D_1^2 T_s V_i M)/(2L(M-1))$ and $(D_1^2 T_s R)/(2L) = M^2 - M$; by substituting them into (21) and (25), it leads to

$$L\frac{d\hat{i}_L}{dt} = \left(\frac{V_i + V_o}{V_i}D_1\right)\hat{v}_i - \left(\frac{V_i}{V_i - V_o}D_1\right)(\hat{v}_i - \hat{v}_o) + 2V_o\hat{d}_1 - \frac{V_o}{I_L}D_1\hat{i}_L, \tag{31}$$

$$C\frac{d\hat{u}_C}{dt} = \hat{i}_L - \frac{D_1 T_s V_i}{L}\hat{d}_1 - \frac{D_1^2 T_s}{2L}\hat{v}_i - \frac{\hat{u}_C}{R}. \tag{32}$$

Let $\hat{v}_i = 0$, then (31) will be

$$\left(sL + \frac{2L(M-1)}{D_1 T_s}\right)\hat{i}_L = \frac{1}{1-M}D_1\hat{v}_o + 2V_o\hat{d}_1, \tag{33}$$

and if $u_c = v_o$ and $\hat{v}_i = 0$, then we can obtain the following equation from (32):

$$\left(sC + \frac{1}{R}\right)\hat{v}_o + \frac{D_1 T_s V_i}{L}\hat{d}_1 = \hat{i}_L. \tag{34}$$

Also considering (33) and (34) simultaneously, in this case, the transfer function of the boost converter will become

$$\frac{\hat{v}_o(s)}{\hat{d}_1(s)} = \frac{D_1 T_s V_i\left(((2)/(D_1 T_s)) - s\right)}{s^2 LC + s\left((L/R) + ((2LC(M-1))/(D_1 T_s))\right) + (((2M-1)D_1)/(M(M-1)))}. \tag{35}$$

4.4. Buck-Boost Converter Small Signal Transfer Function. For the boost converter, $V_{on} = V_i$, $V_{off} = -V_o$, and $i_o = i_D$, and from Table 2, $I_L = (D_1^2 T_s V_i(1+M))/(2LM)$ and $(D_1^2 T_s R)/(2L) = M^2$. Then, by substituting them into (21) and (25), we have

$$L\frac{d\hat{i}_L}{dt} = \left(\frac{2V_i + V_o}{V_i}D_1\right)\hat{v}_i - \frac{V_i}{V_o}D_1\hat{v}_o + 2(V_i + V_o)\hat{d}_1 - \frac{(V_i + V_o)}{I_L}D_1\hat{i}_L, \tag{36}$$

$$C\frac{d\hat{u}_C}{dt} = \hat{i}_L - \frac{D_1 T_s V_i}{L}\hat{d}_1 - \frac{D_1^2 T_s}{2L}\hat{v}_i - \frac{\hat{u}_C}{R}. \tag{37}$$

With $\hat{v}_i = 0$, then (36) will lead to

$$\left(sL + \frac{2LM}{D_1 T_s}\right)\hat{i}_L = -\frac{1}{M}D_1\hat{v}_o + 2(V_i + V_o)\hat{d}_1, \tag{38}$$

and again if $u_c = v_o$ and $\hat{v}_i = 0$, (37) yields

$$\left(sC + \frac{1}{R}\right)\hat{v}_o + \frac{D_1 T_s V_i}{L}\hat{d}_1 = \hat{i}_L. \tag{39}$$

Finally, considering (38) and (39) simultaneously, again the transfer function of the buck-boost converter will be

$$\frac{\hat{v}_o(s)}{\hat{d}_1(s)} = \frac{D_1 T_s V_i\left((2/(D_1 T_s)) - s\right)}{s^2 LC + s\left((L/R) + ((2LCM)/(D_1 T_s))\right) + ((2D_1)/M)}. \tag{40}$$

4.5. KY Converter Small Signal Transfer Function. For the KY converter, $V_{on} = 2V_i - V_o$, $V_{off} = V_i - V_o$, and $i_o = i_L$, and from Table 2, $I_L = (D_1^2 T_s V_i(2-M))/(2L(M-1))$ and $(D_1^2 T_s R)/(2L) = (M(M-1))/(2-M)$. Then, substituting them into (21) and (23) will lead to

$$L\frac{d\hat{i}_L}{dt} = \frac{3V_i - V_o}{2V_i - V_o}D_1(2\hat{v}_i - \hat{v}_o) - \frac{2V_i - V_o}{V_i - V_o}D_1(\hat{v}_i - \hat{v}_o) + 2V_i\hat{d}_1 - \frac{V_i}{I_L}D_1\hat{i}_L, \tag{41}$$

$$C\frac{d\hat{u}_C}{dt} = \hat{i}_L - \frac{\hat{u}_C}{R}. \tag{42}$$

Let $\hat{v}_i = 0$, then (41) becomes

$$\left(sL + \frac{2L(M-1)}{D_1 T_s(2-M)}\right)\hat{i}_L = \frac{1}{((2-M)(1-M))}D_1\hat{v}_o + 2V_i\hat{d}_1. \tag{43}$$

Then with uc = vo, (42) gives

$$\left(sC + \frac{1}{R}\right)\hat{v}_o = \hat{i}_L. \tag{44}$$

Again with (43) and (44) considered simultaneously, the transfer function of the KY converter can be obtained as

$$\frac{\hat{v}_o(s)}{\hat{d}_1(s)} = \frac{2V_i}{s^2 LC + s\left((L/R) + ((2LC(M-1))/(D_1 T_s(2-M)))\right) + (((M^2 - 4M + 2)D_1)/((2-M)(1-M)M))}. \tag{45}$$

5. Circuit Averaging Method for Large-Signal and Small Signal Modeling Deduction

In this section, the approach for deducing the DCM small signal models for different DC-DC converters by using the CA method will be discussed.

5.1. General Large-Signal and Corresponding Small Signal Modeling Using the CA Method. With the help of Reference [10], according to (7) and (8), the switching network of the DC-DC converter can be transformed into the circuit as shown in Figure 4.

When the circuit reaches the steady-state, the average voltage across the inductor is zero, then Figure 4 imposes,

$$V_{\mathrm{LM}} = 0. \tag{46}$$

From Figure 4, we can obtain

$$V_{\mathrm{LS}} = V_{\mathrm{LM}} + V_{\mathrm{MS}} = V_{\mathrm{MS}}, \tag{47}$$

$$V_{\mathrm{LD}} = V_{\mathrm{LM}} + V_{\mathrm{MD}} = V_{\mathrm{MD}}. \tag{48}$$

By using (5)–(8), they yield the following large-signal equations (considering identical the large-signal value and the DC value relationships):

$$i_{\mathrm{S}} = \frac{d_1^2 T_s v_{\mathrm{on}}}{2L}, \tag{49}$$

$$i_{\mathrm{D}} = -\frac{d_1^2 T_s v_{\mathrm{on}}^2}{2L v_{\mathrm{off}}}. \tag{50}$$

Taking the derivative of (49) and (50), the corresponding small signal equations will emerge as follows:

$$\begin{aligned} \hat{i}_{\mathrm{S}} &= \frac{D_1 T_s V_{\mathrm{on}}}{L}\hat{d}_1 + \frac{D_1^2 T_s}{2L}\hat{v}_{\mathrm{on}}, \\ \hat{i}_{\mathrm{D}} &= -\frac{D_1 T_s V_{\mathrm{on}}^2}{L V_{\mathrm{off}}}\hat{d}_1 - \frac{D_1^2 T_s V_{\mathrm{on}}}{L V_{\mathrm{off}}}\hat{v}_{\mathrm{on}} + \frac{D_1^2 T_s V_{\mathrm{on}}^2}{2L V_{\mathrm{off}}^2}\hat{v}_{\mathrm{off}}, \end{aligned} \tag{51}$$

and from (47) and (48), $V_{\mathrm{on}} = V_{\mathrm{LS}} = V_{\mathrm{MS}}$ and $V_{\mathrm{off}} = V_{\mathrm{LD}} = V_{\mathrm{MD}}$. Then, the small signal circuit of the switching network in Figure 4 can be transformed into Figure 5, where

$$\begin{aligned} k_S &= \frac{D_1 T_s V_{\mathrm{on}}}{L}, \\ g_{\mathrm{S}} &= \frac{D_1^2 T_s}{2L}, \\ k_{\mathrm{D}} &= -\frac{D_1 T_s V_{\mathrm{on}}^2}{L V_{\mathrm{off}}}, \\ g_{\mathrm{D}} &= -\frac{D_1^2 T_s V_{\mathrm{on}}}{L V_{\mathrm{off}}}, \\ g_{\mathrm{M}} &= \frac{D_1^2 T_s V_{\mathrm{on}}^2}{2L V_{\mathrm{off}}^2}. \end{aligned} \tag{52}$$

From Figure 5, we can write

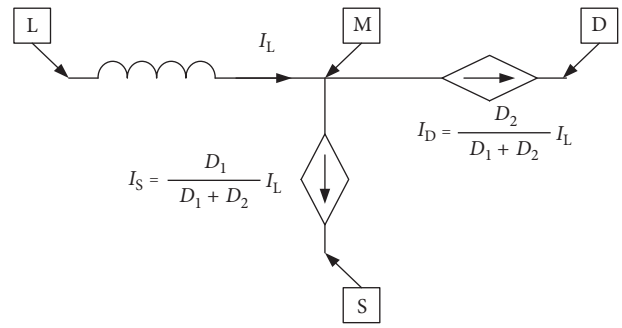


Figure 4: Equivalent circuit of the switching network (current source).

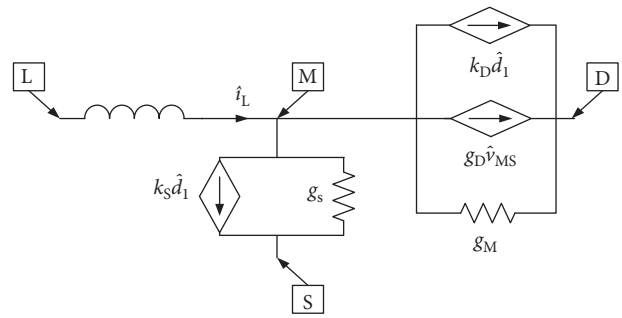


Figure 5: Small signal equivalent circuit of the switching network.

$$\begin{aligned} \hat{i}_{\mathrm{L}} &= (k_{\mathrm{S}} + k_{\mathrm{D}})\hat{d}_1 + (g_{\mathrm{S}} + g_{\mathrm{D}})\hat{v}_{\mathrm{MS}} + g_{\mathrm{M}}\hat{v}_{\mathrm{MD}}, \\ &= (k_{\mathrm{S}} + k_{\mathrm{D}})\hat{d}_1 + (g_{\mathrm{S}} + g_{\mathrm{D}} + g_{\mathrm{M}})\hat{v}_{\mathrm{MS}} + g_{\mathrm{M}}\hat{v}_{\mathrm{SD}}. \end{aligned} \tag{53}$$

Then, with $k_{\mathrm{d1}} = k_{\mathrm{S}} + k_{\mathrm{D}}$ and $g_{\mathrm{MS}} = g_{\mathrm{S}} + g_{\mathrm{D}} + g_{\mathrm{M}}$, we can obtain the factors k_{S}, k_{D}, k_{d1}, g_{S}, g_{D}, g_{M}, and g_{MS} of the four DC-DC converters (buck, boost, buck-boost, and KY) as shown in Table 3.

With these factors, we can substantially simplify the calculation process, as shown next. Further, we can deduce that

$$\hat{v}_{\mathrm{LM}} = sL\hat{i}_{\mathrm{L}}, \tag{54}$$

$$\hat{v}_{\mathrm{MS}} = \hat{v}_{\mathrm{LS}} - \hat{v}_{\mathrm{LM}}. \tag{55}$$

Then (53) can be rewritten as

$$\left(sL + \frac{1}{g_{\mathrm{MS}}}\right)\hat{i}_{\mathrm{L}} = \frac{k_{d_1}}{g_{\mathrm{MS}}}\hat{d}_1 + \hat{v}_{\mathrm{LS}} + \frac{g_{\mathrm{M}}}{g_{\mathrm{MS}}}\hat{v}_{\mathrm{SD}}, \tag{56}$$

and considering the capacitor, its current becomes

$$C\frac{d\hat{u}_{\mathrm{C}}}{dt} = \hat{i}_{\mathrm{o}} - \frac{\hat{u}_{\mathrm{C}}}{R}. \tag{57}$$

If $i_{\mathrm{o}} = i_{\mathrm{L}}$, (57) will become

$$C\frac{d\hat{u}_{\mathrm{C}}}{dt} = \hat{i}_{\mathrm{L}} - \frac{\hat{u}_{\mathrm{C}}}{R}. \tag{58}$$

Then, with $u_{\mathrm{c}} = v_{\mathrm{o}}$, we have

Table 3: Relevant factors of the circuit averaging (CA) method.

DC-DC converter	Buck	Boost	Buck-boost	KY
k_S	$(2M^2V_i)/(D_1R)$	$(2M(M-1)V_i)/(D_1R)$	$(2M^2V_i)/(D_1R)$	$(2M(M-1)V_i)/(D_1R)$
k_D	$((2M(1-M)V_i)/(D_1R))$	$(2MV_i)/(D_1R)$	$(2MV_i)/(D_1R)$	$(2M(2-M)V_i)/(D_1R)$
k_{d1}	$(2MV_i)/(D_1R)$	$(2M^2V_i)/(D_1R)$	$(2M(M+1)V_i)/(D_1R)$	$(2MV_i)/(D_1R)$
g_S	$(M^2)/((1-M)R)$	$(M^2-M)/(R)$	M^2/R	$(M(M-1))/((2-M)R)$
g_D	$(2M)/R$	$(2M)/R$	$(2M)/R$	$(2M)/R$
g_M	$(1-M)/R$	$M/((M-1)R)$	$1/R$	$(M(2-M))/((M-1)R)$
g_{MS}	$1/((1-M)R)$	$M^3/((M-1)R)$	$((M+1)^2)/R$	$M/((2-M)(M-1))$

$$\widehat{i}_L = \left(SC + \frac{1}{R}\right)\widehat{v}_o, \tag{59}$$

and with $i_o = i_D$, (57) yields

$$C\frac{d\widehat{u}_C}{dt} = k_D\widehat{d}_1 + g_D\widehat{v}_{MS} + g_M\widehat{v}_{MD} - \frac{\widehat{u}_C}{R}. \tag{60}$$

Finally, with (54)–(56), $u_c = v_o$, (60) can be rewritten as

$$\begin{aligned}\widehat{i}_L = {} & \frac{g_{MS}}{g_D + g_M}\left(SC + \frac{1}{R}\right)\widehat{v}_o \\ & + \left(k_{d1} - \frac{k_D \cdot g_{MS}}{g_D + g_M}\right)\widehat{d}_1 + \left(g_M - \frac{g_M \cdot g_{MS}}{g_D + g_M}\right)\widehat{v}_{SD}.\end{aligned} \tag{61}$$

Here, (56), (59), and (61) are the 3 general equations to deduce the DCM small signal models for the different DC-DC converters. By just input, the voltage drops V_{LS} and V_{SD} from Figure 5, plus the factors (Table 3) and the DC parameters (Table 2) into (56), (59) and (61), and the corresponding DCM small signal transfer functions can be calculated easily in the following.

5.2. Buck Converter Small Signal Transfer Function. For the buck converter, from Figure 5, $V_{LS} = V_i - V_o$, $V_{SD} = -V_i$, and $i_o = i_L$, and from Table 2, $I_L = (D_1^2T_sV_i(1-M))/(2LM)$ and $(D^2T_sR)/(2L) = M^2/(1-M)$. Then, with $\widehat{v}_i = 0$, (56) and (59) lead to

$$(sL + (1-M)R)\widehat{i}_L = \frac{2M(1-M)V_i}{D_1}\widehat{d}_1 - \widehat{v}_o, \tag{62}$$

$$\widehat{i}_L = \left(sC + \frac{1}{R}\right)\widehat{v}_o. \tag{63}$$

And from (62) and (63) simultaneously, the transfer function of the buck converter can be obtained as

$$\frac{\widehat{v}_o(s)}{\widehat{d}_1(s)} = \frac{M(1-M)\left((2V_i)/D_1\right)}{s^2LC + s((L/R) + RC(1-M)) + 2 - M}. \tag{64}$$

5.3. Boost Converter Small Signal Transfer Function. For the boost converter, from Figure 5, $V_{LS} = V_i$, $V_{SD} = -V_o$, $i_o = i_D$, and from Table 2, $I_L = (D_1^2T_sV_iM)/(2L(M-1))$ and $(D_1^2T_sR)/(2L) = M^2 - M$. Then, with $\widehat{v}_i = 0$, (56) and (61) imply,

$$\left(sL + \frac{(M-1)R}{M^3}\right)\widehat{i}_L = \frac{2(M-1)V_i}{D_1M}\widehat{d}_1 - \frac{1}{M^2}\widehat{v}_o, \tag{65}$$

$$\begin{aligned}\widehat{i}_L = {} & \frac{M^2}{2M-1}\left(sC + \frac{2M-1}{MR}\right)\widehat{v}_o \\ & + \frac{2(M-1)M^2V_i}{(2M-1)D_1R}\widehat{d}_1.\end{aligned} \tag{66}$$

Again, from (65) and (66) simultaneously, the transfer function of the boost converter will become,

$$\frac{\widehat{v}_o(s)}{\widehat{d}_1(s)} = \frac{\left((D_1T_sV_i)/M\right)\left(((2(M-1))/(D_1^2T_sM)) - s\right)}{s^2LC + s(((L(2M-1))/(RM)) + ((RC(M-1))/(M^3))) + ((2M-1)/M^3)}. \tag{67}$$

5.4. Buck-Boost Converter Small Signal Transfer Function. For the buck-boost converter, from Figure 5, $V_{LS} = V_i$, $V_{SD} = -(V_i + V_o)$, and $i_o = i_D$, and from Table 2, $I_L = (D_1^2T_sV_i(1+M))/(2LM)$ and $(D_1^2T_sR)/(2L) = M^2$. Then, with $\widehat{v}_i = 0$, (56) and (61) impose

$$\left(sL + \frac{R}{(M+1)^2}\right)\widehat{i}_L = \frac{2MV_i}{D_1(M+1)}\widehat{d}_1 - \frac{1}{(M+1)^2}\widehat{v}_o, \tag{68}$$

$$\begin{aligned}\widehat{i}_L = {} & \frac{(M+1)^2}{2M+1}\left(SC + \frac{2M^2+2M+1}{(M+1)^2R}\right)\widehat{v}_o \\ & + \frac{2\left(M^3+M^2\right)V_i}{(2M+1)D_1R}\widehat{d}_1.\end{aligned} \tag{69}$$

Similarly, with (68) and (69) considered simultaneously, the transfer function of the buck-boost converter will be

$$\frac{\widehat{v}_{\mathrm{o}}(s)}{\widehat{d}_1(s)} = \frac{\left((D_1 T_s V_{\mathrm{i}})/(M+1)\right)\left(((2M)/(D_1^2 T_s (M+1))) - s\right)}{s^2 LC + s\left(\left((L(2M^2+2M+1))/\left(R(M+1)^2\right)\right) + \left((RC)/\left((M+1)^2\right)\right)\right) + \left(2/\left((M+1)^2\right)\right)}. \tag{70}$$

6.5. KY Converter Small Signal Transfer Function. For the KY converter, from Figure 5, $V_{\mathrm{LS}} = 2V_{\mathrm{i}} - V_{\mathrm{o}}$, $V_{\mathrm{SD}} = -V_{\mathrm{i}}$, and $i_{\mathrm{o}} = i_{\mathrm{L}}$, and from Table 2, $I_{\mathrm{L}} = (D_1^2 T_s V_{\mathrm{i}}(2-M))/(2L(M-1))$ and $(D_1^2 T_s R)/(2L) = (M(M-1))/((2-M))$. Then, with $\widehat{v}_{\mathrm{i}} = 0$, (56) and (59) entail

$$\left(sL + \frac{(2-M)(M-1)R}{M}\right)\widehat{i}_{\mathrm{L}} = \frac{2(2-M)(M-1)V_{\mathrm{i}}}{D_1}\widehat{d}_1 - \widehat{v}_{\mathrm{o}}, \tag{71}$$

$$\widehat{i}_{\mathrm{L}} = \left(sC + \frac{1}{R}\right)\widehat{v}_{\mathrm{o}}. \tag{72}$$

Finally, from (71) and (72) simultaneously, the transfer function of the KY converter will become

$$\frac{\widehat{v}_{\mathrm{o}}(s)}{\widehat{d}_1(s)} = \frac{(2-M)(M-1)\left((2V_{\mathrm{i}})/D_1\right)}{s^2 LC + s\left((L/R) + ((RC(2-M)(M-1))/M)\right) + (((2-M)(M-1)+M)/M)}. \tag{73}$$

6. Simulation Results

We simulated the four DC-DC converters within a Cadence environment of a 65 nm CMOS process and also MATLAB to verify and compare the accuracy of the small signal transfer functions (30), (35), (40), (45), (64), (67), (70), and (73) deduced by the improved SSA and CA methods.

6.1. Buck Converter. The relevant parameters of the buck converter (Figure 2) are $V_{\mathrm{i}} = 1.2$ V, $f_{\mathrm{s}} = 100$ MHz, $C = 10$ nF, $L = 36$ nH, and $R = 40\,\Omega$. The Bode plot comparison between the transfer functions with the SSA and the CA methods ((30) and (64)), and the simulated circuit power stage (PS), is shown in Figure 6, for $d_1 = 0.3$, 0.5, and 0.7.

From Figure 6, we can conclude that in the buck converter, the CA method provides higher accuracy than the SSA method in any duty ratio range d_1, with clearer emphasis at larger d_1 values.

6.2. Boost Converter. The relevant parameters of the boost converter (Figure 2) are $V_{\mathrm{i}} = 1.2$ V, $f_{\mathrm{s}} = 100$ MHz, $C = 10$ nF, $L = 13.5$ nH, and $R = 60\,\Omega$. The Bode plot comparison between the transfer functions with the SSA and the CA methods ((35) and (67)), and the simulated circuit PS, is shown in Figure 7, for $d_1 = 0.3$, 0.5, and 0.7.

From Figure 7, we can conclude that in the boost converter with a small duty ratio value ($d_1 = 0.3$), the SSA method contains slightly better accuracy than the CA method. But, as the d_1 increases, the accuracy of the CA method will improve over the SSA method, again being more evident for larger d_1 values.

6.3. Buck-Boost Converter. The relevant parameters of the buck-boost converter (Figure 2) are $V_{\mathrm{i}} = 1.2$ V, $f_{\mathrm{s}} = 100$ MHz, $C = 40$ nF, $L = 15$ nH, and $R = 150\,\Omega$. The Bode plot comparison between the transfer functions with the SSA and the CA methods ((40) and (70)), and the simulated circuit PS, is shown in Figure 8, for $d_1 = 0.3$, 0.5, and 0.7.

From Figure 8, the analysis of the simulation results of the boost converter is similar to those of the buck-boost converter, leading exactly to the same conclusions.

6.4. KY Converter. Finally, for the KY converter (Figure 2), $V_{\mathrm{i}} = 1.2$ V, $f_{\mathrm{s}} = 100$ MHz, $C = 10$ nF, $C_{\mathrm{f}} = 10$ nF, $L = 3.6$ nH, and $R = 60\,\Omega$, and the Bode plot comparison between the transfer functions with the SSA and the CA methods ((45) and (73)), and the simulated circuit PS, is shown in Figure 9, for $d_1 = 0.3$, 0.5, and 0.7.

From Figure 9, the analysis of the simulation results of the KY converter are similar to those of the buck converter, leading exactly to the same conclusions.

7. High-Accuracy Modeling Method for Different DC-DC Converters in DCM—Selection Strategy

7.1. Derivation. By using the methods presented in [3] and [6], the approximate poles and zeros for different DC-DC converters in DCM with the SSA and CA methods can be calculated and summarized in Table 4. The previous Bode plot simulation results clearly demonstrate that the phase-frequency responses of the DC-DC converters power stages generally show a larger phase lag than the small signal models given by both the SSA and CA methods. Based on this, if the modeling method presents a smaller value of the second pole or zero (leading to a larger phase lag), it will exhibit a better accuracy of the system phase-frequency response. From Table 4, we propose a selection strategy of high-accuracy small signal modeling method for the DC-DC converters as in Table 5.

7.2. Verification. For verification of the proposed selection strategy, we simulated a buck converter and a boost

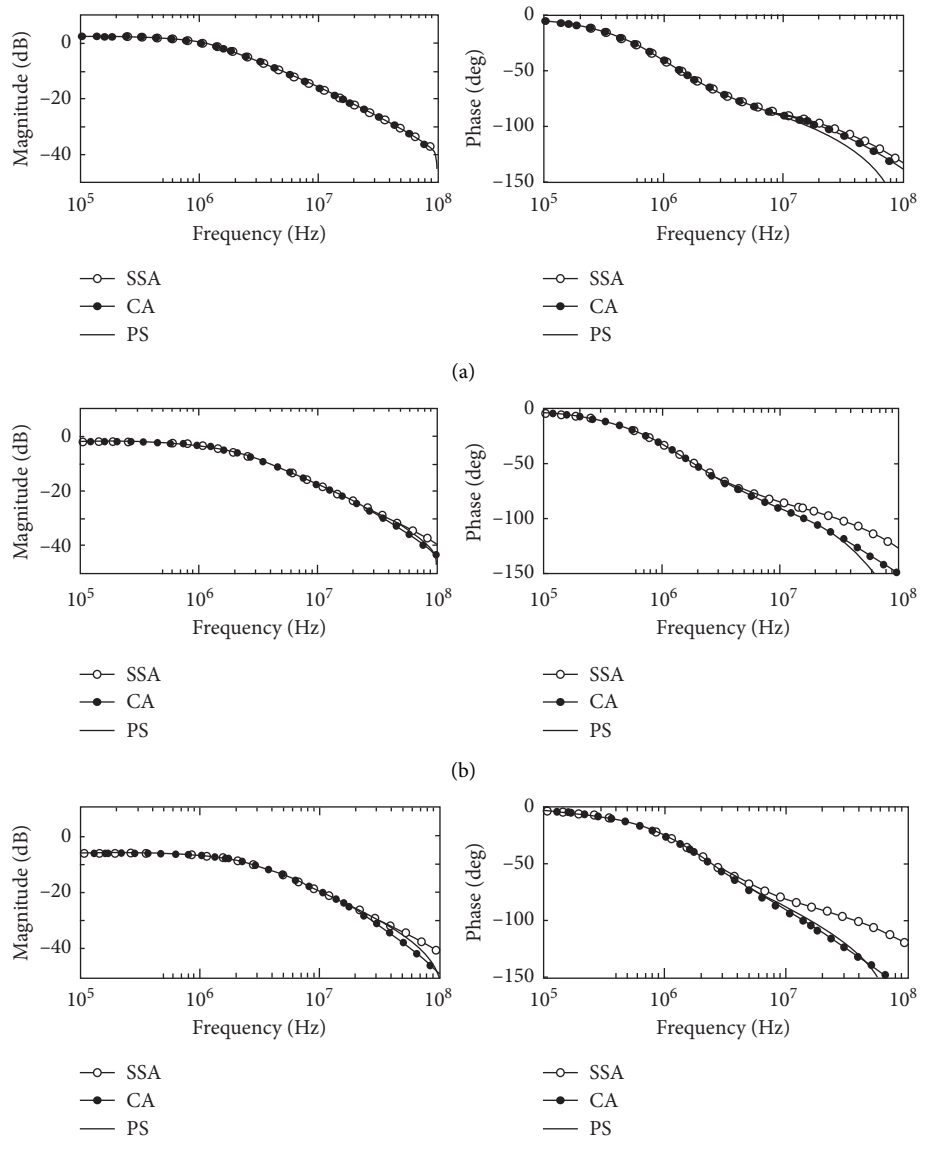


Figure 6: Small signal models comparison of the buck converter with SSA and CA methods: (a) $d_1 = 0.3$; (b) $d_1 = 0.5$; and (c) $d_1 = 0.7$.

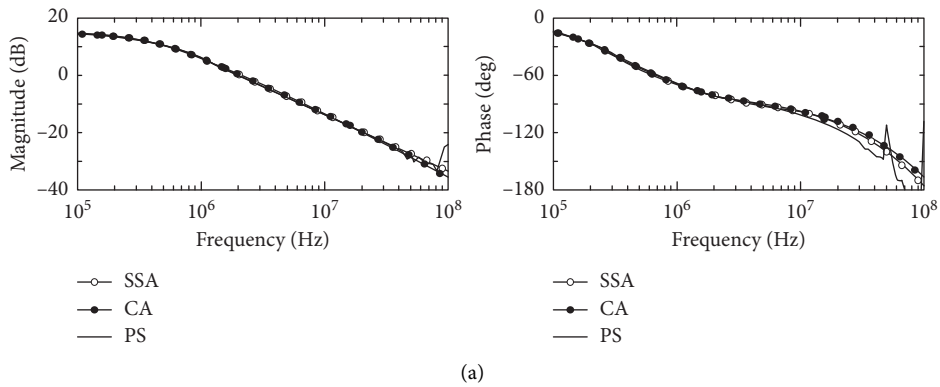


Figure 7: Continued.

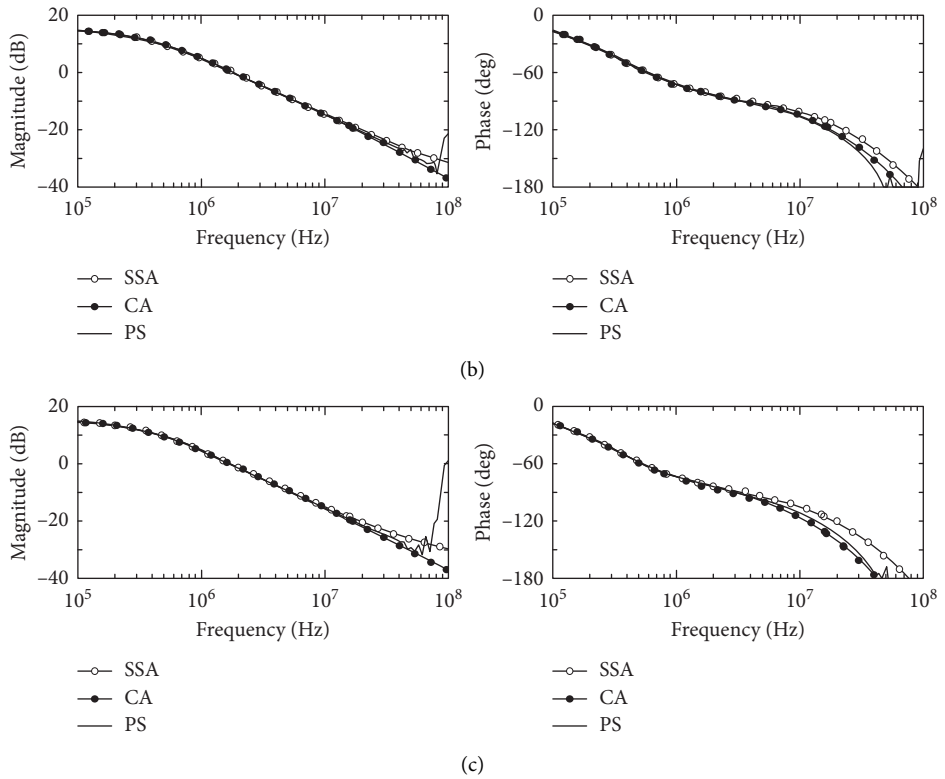


Figure 7: Small signal models comparison of the boost converter with SSA and CA methods: (a) $d_1 = 0.3$; (b) $d_1 = 0.5$; and (c) $d_1 = 0.7$.

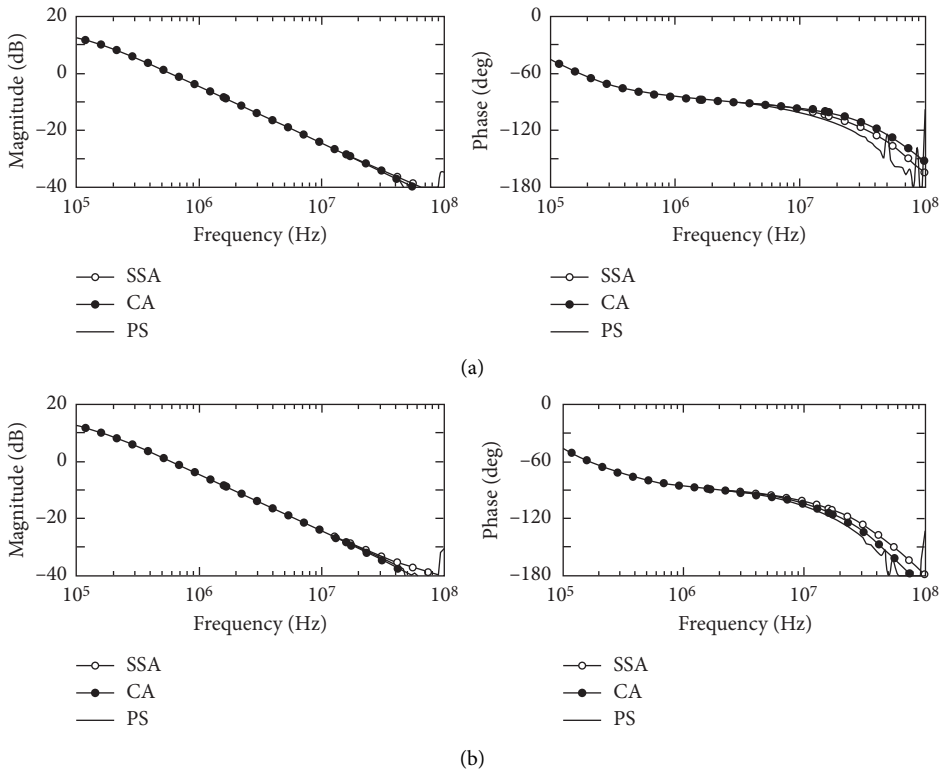
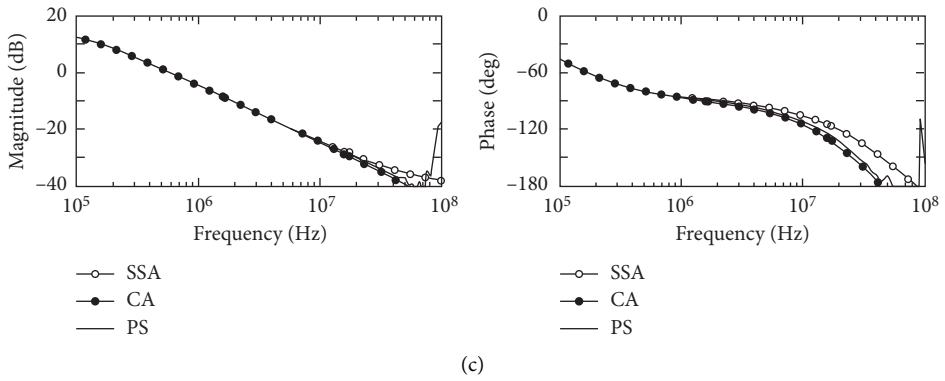
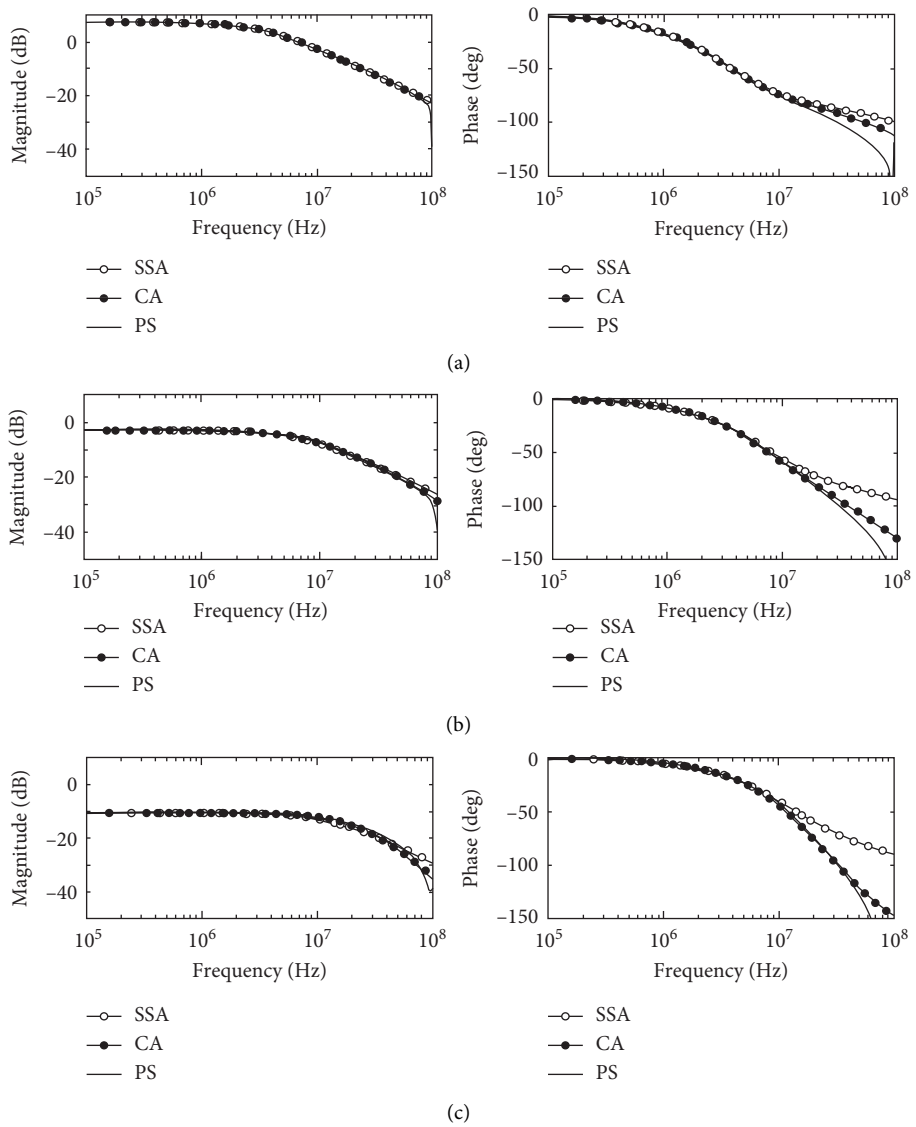


Figure 8: Continued.



(c)

Figure 8: Small signal models comparison of the buck-boost converter with SSA and CA methods: (a) $d_1 = 0.3$; (b) $d_1 = 0.5$; and (c) $d_1 = 0.7$.



(a)

(b)

(c)

Figure 9: Small signal models comparison of the KY converter with SSA and CA methods: (a) $d_1 = 0.3$; (b) $d_1 = 0.5$; and (c) $d_1 = 0.7$.

converter with the Cadence Spectre simulator to demonstrate that the converter operates with higher stability with a more accurate small signal modeling method used in the compensator design. The simulated results of the system phase-frequency response and the closed-loop controlled converters' load transient response are presented in

Table 4: Approximate poles and zeros for various DC-DC converters in DCM.

Name	Method	First pole	Second pole	Zero
Buck	SSA	$(2-M)/(RC(1-M))$	$(2M)/(d_1T_s(1-M))$	
	CA	$(2-M)/(RC(1-M))$	$(2M^2)/(d_1^2T_s)$	
Boost	SSA	$(2M-1)/(RC(M-1))$	$(2(M-1))/(d_1T_s)$	$2/(d_1T_s)$
	CA	$(2M-1)/(RC(M-1))$	$(2((M-1)/M)^2)/(d_1^2T_s)$	$(2((M-1)/M))/(d_1^2T_s)$
Buck-boost	SSA	$2/(RC)$	$(2M)/(d_1T_s)$	$2/(d_1T_s)$
	CA	$2/(RC)$	$2(M/(M+1))^2/d_1^2T_s$	$2(M/(M+1))/d_1^2T_s$
KY	SSA	$(M^2-4M+2)/(RC(M^2-3M+2))$	$(2(M-1))/(d_1T_s(2-M))$	
	CA	$(M^2-4M+2)/(RC(M^2-3M+2))$	$(2(M-1)^2)/(d_1^2T_s)$	

Table 5: Selection strategy between SSA and CA for high-accuracy small signal modeling.

Name	Criterion	Modeling selection
Buck	$(2M/(d_1T_s(1-M))) < ((2M^2)/(d_1^2T_s))$	SSA
	$(2M/(d_1T_s(1-M))) > ((2M^2)/(d_1^2T_s))$	CA
Boost	$\min(((2(M-1))/(d_1T_s)), (2/d_1T_s)) < (2((M-1)/M)^2/(d_1^2T_s))$	SSA
	$\min(((2(M-1))/(d_1T_s)), (2/d_1T_s)) > (2((M-1)/M)^2/(d_1^2T_s))$	CA
Buck-boost	$\min(((2M)/(d_1T_s)), (2/d_1T_s)) < (2(M/(M+1))^2/(d_1^2T_s))$	SSA
	$\min(((2M)/(d_1T_s)), (2/d_1T_s)) > (2(M/(M+1))^2/(d_1^2T_s))$	CA
KY	$(2(M-1))/(d_1T_s(2-M)) < ((2(M-1)^2)/(d_1^2T_s))$	SSA
	$(2(M-1))/(d_1T_s(2-M)) > ((2(M-1)^2)/(d_1^2T_s))$	CA

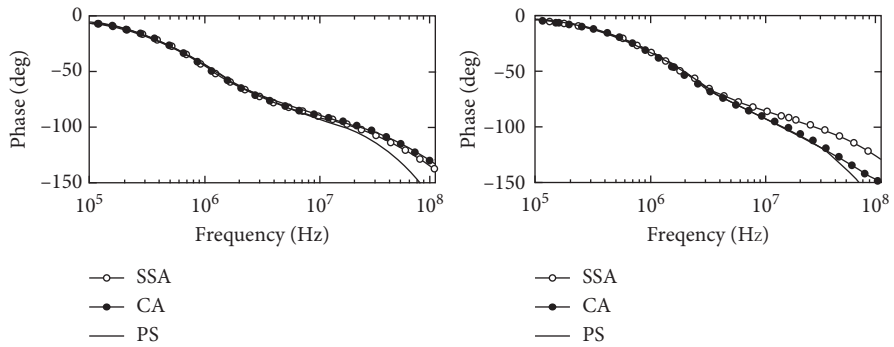


Figure 10: Simulation verification with the buck converter ($V_i = 1.2$ V, $f_s = 100$ MHz, $C = 10$ nF, $L = 40$ nH, and $R = 40\,\Omega$): (a) $d_1 = 0.2$, $(2M/(d_1T_s(1-M))) < ((2M^2)/(d_1^2T_s))$; and (b) $d_1 = 0.5$, $(2M/(d_1T_s(1-M))) > ((2M^2)/(d_1^2T_s))$.

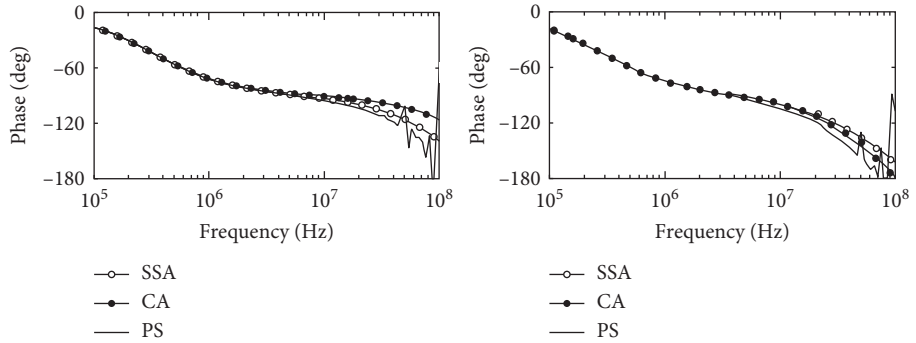


Figure 11: Simulation verification with the boost converter ($V_i = 1.2$ V, $f_s = 100$ MHz, $C = 20$ nF, $L = 2$ nH, and $R = 15\,\Omega$): (a) $d_1 = 0.2$, $\min(((2(M-1))/(d_1T_s)), (2/d_1T_s)) < (2((M-1)/M)^2/(d_1^2T_s))$; and (b) $d_1 = 0.5$, $\min(((2(M-1))/(d_1T_s)), (2/d_1T_s)) > (2((M-1)/M)^2/(d_1^2T_s))$.

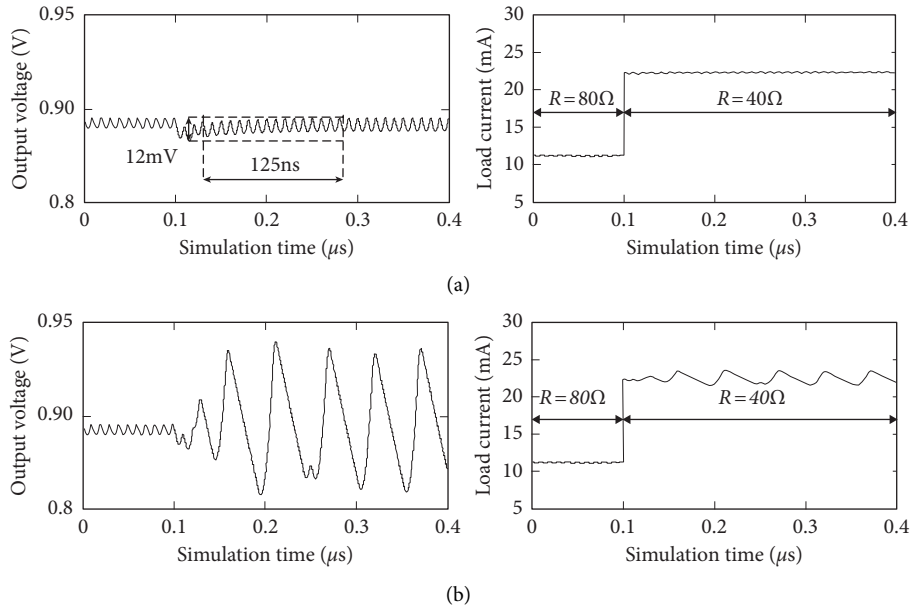


FIGURE 12: V_o and i_o of the designed buck converter with $((2M)/(d_1T_s(1-M))) > (2M^2/d_1^2T_s)$ ($V_i = 1.2\,V$, $f_s = 100\,MHz$, $C = 10\,nF$, $L = 40\,nH$, and $R = 80/40\,\Omega$) and PM = 45°. (a) Compensator based on CA. (b) Compensator based on SSA.

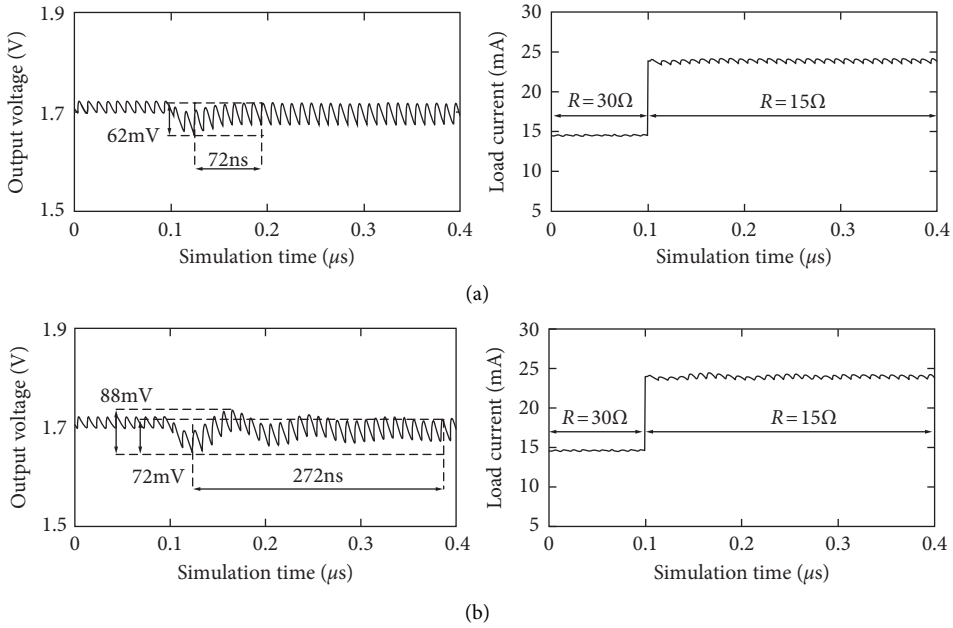


FIGURE 13: V_o and i_o of the designed boost converter with $\min(((2(M-1))/(d_1T_s)), (2/d_1T_s)) < (2((M-1)/M)^2/(d_1^2T_s))$ ($V_i = 1.2\,V$, $f_s = 100\,MHz$, $C = 20\,nF$, $L = 2\,nH$, and $R = 30/15\,\Omega$) and PM = 45°. (a) Compensator based on SSA. (b) Compensator based on CA.

Figures 10–13. These figures confirm the correctness of the proposed selection strategy in Table 5.

Figure 12 presents the simulated output voltage V_o and load current i_o of the designed closed-loop controlled buck converter during a load transient, applying a Type II compensator. As indicated in Table 5, the CA method is more accurate with the condition $((2M)/(d_1T_s(1-M))) > ((2M^2)/(d_1^2T_s))$, and the simulated result (Figure 12) also confirms that the closed-loop controller designed with the CA method exhibits better stability and transient response than the SSA method, even though both cases have the same phase margin (PM) of 45°. On the other hand, Figure 13 shows the simulated V_o and the i_o of the closed-loop controlled boost converter during a load transient, applying also a Type II compensator. In this case, as indicated in Table 5, the SSA modeling method is more accurate with the condition $(\min((2(M-1))/(d_1T_s)), (2/d_1T_s)) < ((2((M-1)/M)^2)/(d_1^2T_s))$ and the simulated result

(Figure 13) also confirms that the closed-loop controller designed with SSA method obtain a better stability and transient response. When there is a sudden change of the i_o, the boost converter with the SSA method responds faster than that with the CA method.

Unlike the conclusion made in [6], this paper shows that, in some cases, the CA method exhibits better accuracy than the SSA method. Figures 12 and 13 confirm that an accurate modeling method is critical to design the appropriate closed-loop controller of the DC-DC converter, demonstrating that the selection strategy given in Table 5 is essential and necessary in the design. The general and streamlined small signal deduction process for both modeling methods can be further applied conveniently to similar DC-DC converter topologies.

8. Conclusions

This paper presented the review, study, DCM small signal modeling deduction and simulation verification by using the improved SSA and CA methods for four DC-DC converters. This paper first proposed a general and intuitive deriving process for the improved SSA and CA modeling methods, such that the corresponding DCM small signal models for DC-DC converters can be easily determined. Then, this paper discovers that the CA can obtain higher accuracy than the improved SSA at some operating conditions, as some research studies claimed that the improved SSA can obtain the highest accuracy among all the modeling methods. Finally, this paper provided a selection strategy for a high-accuracy modeling method for various DC-DC converters operating in DCM, verified by simulations, which is necessary and beneficial in the design of a more accurate DCM closed-loop controller for DC-DC converters, achieving better stability and transient response.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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Research Article

Shunt Active Power Filter Based on Proportional Integral and Multi Vector Resonant Controllers for Compensating Nonlinear Loads

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The current tracking control strategy determines the compensation performance of shunt active power filter (SAPF). Due to inadequate compensation of the main harmonic by traditional proportional integral (PI) control, a control algorithm based on PI and multi vector resonant (VR) controllers is proposed to control SAPF. The mathematical model of SAPF is built, and basic principle of VR controller is introduced. Under the synchronous reference frame, the proposed control method based on pole zero cancellation is designed, which narrows the order of the control system and improves the system dynamic response and the control accuracy. Then the feasibility of the method is demonstrated by analyzing the closed loop frequency characteristics of the system. Finally, the simulation and experimental results are carried out to verify the performance of the proposed method.

1. Introduction

In recent years, with the intensification of the global energy crisis, the renewable energy and power electric technology have been integrated, which has promoted the development of distributed generators (DGs) [1, 2]. The speed driver of small motor, voltage source converter, and a large number of nonlinear loads including electric arc furnace, high-power rectifier, transducer, and fluorescent are connected to the grid, which will cause harmonic pollution unavoidably [3–5]. The power grid operates in this state for a long run, which will bring great harm to power system and power consumers, mainly manifested in the following respects: (1) The line loss of the system is increasing greatly, and the operating efficiency of the grid is reduced. A lot of 3rd harmonics will also increase the neutral current, leading to the damage of the custom power devices. (2) It makes the motor vibrate and produce noise, which affects the safety operation in production. (3) It makes the relay protection device act by mistake, which interrupts the power supply and makes the extent loss to production. (4) It interferes with measuring instruments and communication systems [6–8]. Therefore, it is urgent to control the power harmonic pollution to improve the power quality.

As a new type of power electronic device that can suppress harmonics dynamically, a three-phase three-wire SAPF with excellent performance has been widely used in the field of power quality. The real-time and accurate compensation for the fast changing harmonic currents is an important guarantee for the operation of SAPF safely and reliably. In the past years, a lot of research and analysis have been done on the detection and tracking control strategy of the harmonic currents. In [9, 10], it transforms the harmonic component to the DC component through multisynchronous rotating coordinate transformation; thus, traditional PI controller can be utilized to track the harmonics with zero steady-state error; however, it is too complicated. The hysteresis current control method presented in [11, 12] with quickly dynamic respond performance is simple and easy to realize without carrier modulation, but the control accuracy is inversely proportional to switching frequency. In addition, the switching frequency is not fixed, which sets a higher request to switching device. In [13, 14], the repetitive control theory was developed to solve harmonic problems, which has the advantages of good

robustness, simple structure, and easy implementation. However, dynamic performance is limited if the load changes suddenly. In order to overcome the effect of computational delay and control delay on compensation performance, the dead-beat control in [15, 16] is used to track the reference current, which plays a certain effect, but it highly depends on the system parameters. When the system parameters change, the compensation performance will be greatly affected. In [17, 18], vector resonant(VR) control method is proposed, where proportional controller is to adjust the control bandwidth to improve the dynamic response speed, while the resonant controller is to select frequency for specific frequency signal to improve the control accuracy of current. However, it can not compensate the phase delay of controlled object.

Viewing of the shortcomings of above methods, a current control method based on PI and VR controller is proposed to compensate the selected harmonics accurately. The proportional control can improve the dynamic performance of the current loop and the fundamental current. The VR controller can control a group of positive and negative sequence harmonic currents with zero steady-state error by the idea of zero pole cancellation. Finally, the feasibility and validity of the proposed strategy are confirmed by simulation based on Matlab/Simulink and a prototype of the SAPF using TMS320F28335 as control core.

2. Modeling of SAPF

The structure of two-level three-phase three-wire SAPF used in this paper is shown in Figure 1 [19]. The mathematical model can be described in three-phase ABC static coordinate system as follows:

$$L\frac{di_{\mathrm{Fa}}}{dt} + Ri_{\mathrm{Fa}} = u_{\mathrm{a}} - e_{\mathrm{Sa}},$$
$$L\frac{di_{\mathrm{Fb}}}{dt} + Ri_{\mathrm{Fb}} = u_{\mathrm{b}} - e_{\mathrm{Sb}}, \quad (1)$$
$$L\frac{di_{\mathrm{Fc}}}{dt} + Ri_{\mathrm{Fc}} = u_{\mathrm{c}} - e_{\mathrm{Sc}},$$

where e_{a}, e_{b}, and e_{c} are the 3-phase source voltage; u_{a}, u_{b}, and u_{c} are the 3-phase output voltage of SAPF; i_{sa}, i_{sb}, and i_{sc} are source current; i_{Fa}, i_{Fb}, and i_{Fc} are the compensation currents of SAPF; $S_{\mathrm{a}} - S_{\mathrm{c}}^{*}$ are fully controlled switch devices; L is AC-link inductance; C is DC-link capacitance; u_{dc} is DC-link voltage; and R is the equivalent loss of the AC-link inductance and switch device.

By means of Clarke transform and Park transform, the mathematical model under the synchronous reference frame is given as follows:

$$L\frac{di_{\mathrm{Fd}}}{dt} + Ri_{\mathrm{Fd}} = u_{\mathrm{d}} + \omega_{\mathrm{s}}Li_{\mathrm{Fq}} - e_{\mathrm{Sd}},$$
$$L\frac{di_{\mathrm{Fq}}}{dt} + Ri_{\mathrm{Fq}} = u_{\mathrm{q}} - \omega_{\mathrm{s}}Li_{\mathrm{Fd}} - e_{\mathrm{Sq}}. \quad (2)$$

$e_{\mathrm{d}}, e_{\mathrm{q}} u_{\mathrm{d}}, u_{\mathrm{q}}$ and $i_{\mathrm{Fd}}, i_{\mathrm{Fq}}$ are d-axis components and q-axis components of the three-phase source voltage, AC-link output voltage, and compensation current of the SAPF under synchronous reference frame, respectively. ω_{s} represents the voltage angle frequency detected by a software phase-locked loop.

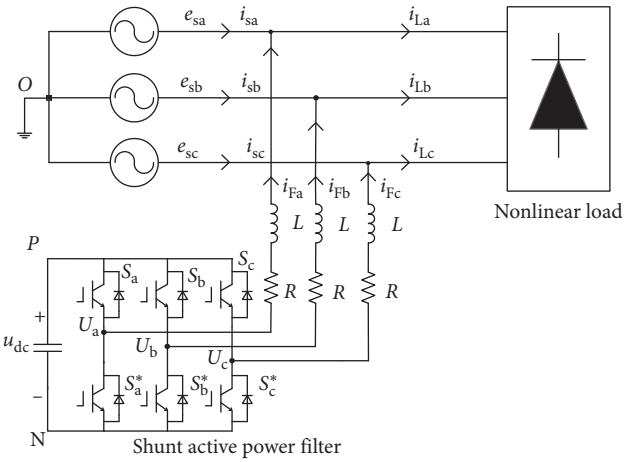


Figure 1: Structure of three-phase three-wire SAPF.

3. Basic Principle of VR Controller

The current controller based on VR control has a higher gain at its resonant frequency, which can control the AC current at the resonant frequency with high precision. The transfer function of the VR controller can be derived as [20]

$$G_{\mathrm{VR}h}(s) = \frac{K_{\mathrm{p}h}s^2 + K_{\mathrm{i}h}s}{s^2 + (h\omega_{\mathrm{s}})^2}, \quad (3)$$

where $K_{\mathrm{p}h}$ and $K_{\mathrm{i}h}$ are proportional coefficient and the integral coefficient, respectively, and $h\omega_{\mathrm{s}}$ is the resonant angle frequency. The absolute value of h represents the order of the harmonic currents, the sign of which represents the rotation direction in sequence component diagram. When h is positive, it represents that harmonic currents are in positive sequence. Otherwise, it represents that harmonic currents are in negative sequence.

The bode diagram of VR controller is shown in Figure 2 for $K_{\mathrm{p}h} = 1, K_{\mathrm{i}h} = 50, h = 6, \omega_{\mathrm{s}} = 100\pi$. On one hand, the open loop gain of VR controller is infinity at its two resonant points $\pm h\omega_{\mathrm{s}}$, but for other frequencies, the gain is rapidly attenuated. On the contrary, the VR controller is phase-leading about 180° at the frequency of $0 \sim h\omega_{\mathrm{s}}$. Once the angular frequency exceeds the resonant frequency, the phase jumps from 180° to 0°. But at negative frequency, it appears on the opposite performance. On the basis of the analysis above, it shows that VR controller has a good control precision for the signal at the resonant frequency.

4. Current Control Strategy of SAPF

4.1. VR Controller for Compensating Harmonic Currents. For the three-phase uncontrollable rectifier, the main harmonic currents consist of 5th of negative sequence, 7th of positive sequence, 11th of negative sequence, 13th of positive

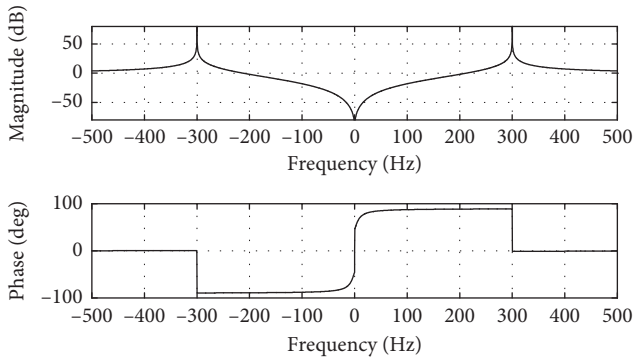


Figure 2: Bode diagram of VR controller.

harmonic, and so on, such that $h = \pm 6n + 1, n$ is $1, 2, \ldots$. Since the synchronous reference frame provides a frequency shift of −50 Hz, the main harmonic current in fundamental frame transforms to 6th of positive and negative sequence harmonic, 12th of positive and negative sequence harmonic, and so on. The harmonic orders become $h = \pm 6n$. Thus the multi-VR controller can compensate the selected harmonic based on formula (3). The equivalent gain of the SAPF K_{PWM} is set to 1. The current control block diagram is shown in Figure 3, where $P(s) = 1/(Ls + R)$ is the transfer function of the controlled object.

Taking the d-axis current as an example, current open loop transfer function of the multi-VR controller is

$$\begin{aligned} G_{\mathrm{o}}(s) &= \sum_{h=6n,n=1,2}^{5} G_{\mathrm{VR}h}(s) P(s) \\ &= \sum_{h=6n,n=1,2}^{5} \frac{K_{\mathrm{p}h} s^2 + K_{\mathrm{i}h} s}{\left(s^2 + (h\omega_s)^2\right)(Ls + R)}. \end{aligned} \tag{4}$$

The basic idea of VR control is to adopt the zero point of the control to offset the poles of the controlled object, so as to compensate for the phase lag of the controlled object, thus improve the control accuracy of the harmonic currents. The zero of the controller can effectively cancel the poles of the controlled object on condition that $K_{\mathrm{p}h} = K_{\mathrm{i}h} * L/R$, and the simplified open loop transfer function is given as

$$G_{\mathrm{o}}(s) = \sum_{h=6n,n=1,2}^{5} \frac{K_{\mathrm{p}h} s}{L\left(s^2 + (h\omega_s)^2\right)}. \tag{5}$$

The closed loop transfer function is

$$G_{\mathrm{c}}(s) = \frac{G_{\mathrm{o}}(s)}{1 + G_{\mathrm{o}}(s)} = \frac{\sum_{h=6n,n=1,2}^{5} \left(K_{\mathrm{p}h} s / L\left(s^2 + (h\omega_s)^2\right)\right)}{1 + \sum_{h=6n,n=1,2}^{5} \left(K_{\mathrm{p}h} s / L\left(s^2 + (h\omega_s)^2\right)\right)}. \tag{6}$$

The values of $K_{\mathrm{p}h}, K_{\mathrm{i}h}, L,$ and R in formulae (4)–(6) are both greater than 0. The bode diagram of harmonic current close loop control is depicted in Figure 4, at the resonant frequency, the amplitude gain of the transfer function is 1 without phase delay, which indicates that the VR controller has frequency selection function on a pair of harmonic currents and can be controlled with zero steady-state error.

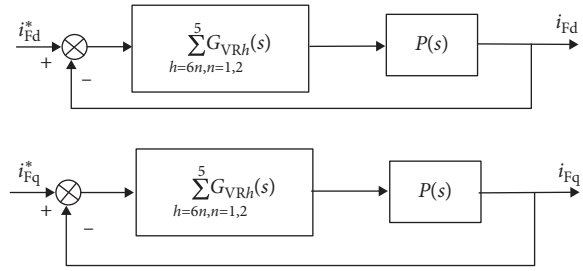


Figure 3: Current control block diagram based on multi-VR controller.

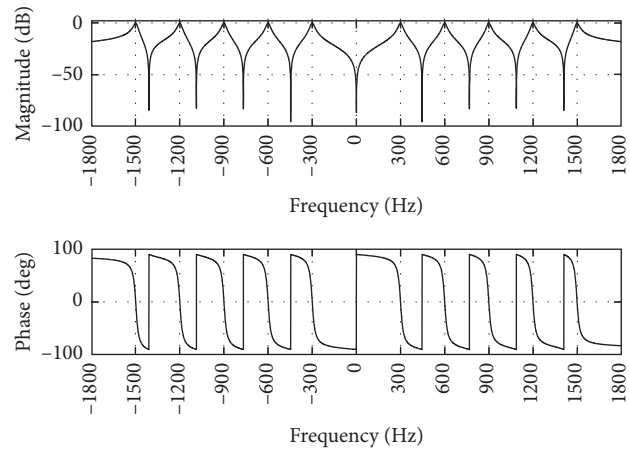


Figure 4: Bode diagram of harmonic current close loop control.

Therefore, the system is stable even when the circuit parameters and VR parameters change.

Whether SAPF can operate stably is affected not only by its own system parameters, but also by external disturbances, and the grid voltage is the most important factor for SAPF. Next, the tracking performance of compensation current is analyzed, when the grid voltage is disturbed. The current control block is shown in Figure 5.

When controlling any order of harmonic, the transfer function of compensation current caused by grid voltage disturbance is

$$\Phi_{\mathrm{en}}(s) = \frac{P(s)}{1 + G_0(s)} = \frac{1}{(Ls + R)\left(1 + \left(K_{\mathrm{p}h} s / L\left(s^2 + (h\omega_s)^2\right)\right)\right)}. \tag{7}$$

At the resonant frequency, the amplitude gain caused by the grid voltage disturbance tends to 0, that is, the steady-state error is 0, which indicates that the compensation current is affected by the voltage disturbance very little by using the VR controller.

4.2. PI Controller for Compensating Fundamental Current. The previous section demonstrates that the VR controller with double resonant frequency can compensate the harmonic with zero steady-state error, but from bode diagram of harmonic close loop control, the amplitude gain of the current near 0 Hz is very small, which means that the VR

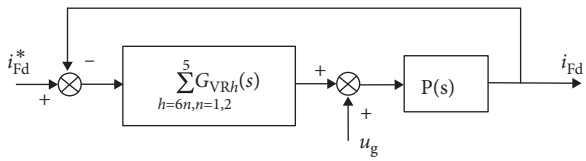


Figure 5: Current control block diagram when the system is disturbed by the grid voltage.

controller is not ideal for the low frequency signal including DC current signal and has the problem of slow dynamic response. However, in addition to controlling the harmonic currents, the SAPF needs to control the fundamental current from voltage controller to compensate for its loss. The DC current obtained fundamental current by the synchronous reference frame. So, it is necessary to ameliorate the VR controller to improve the gain of the low frequency signals. For $h = 0$ in formula (3), the VR controller can be transformed to PI controller, as shown in the following formula:

$$G_{PI}(s) = \frac{K_{p0}s + K_{i0}}{s}. \tag{8}$$

The fundamental current control block diagram based on PI controller is given in Figure 6.

The fundamental current closed loop transfer function based on the PI controller is

$$\Phi_c(s) = \frac{K_{p0}s + K_{i0}}{Ls^2 + \left(R + K_{p0}\right)s + K_{i0}}. \tag{9}$$

For $K_{p0}/K_{i0} = L/R$, the zero point of the PI controller is used to offset the pole of the controlled object; thus, the phase delay of the controlled object is compensated. That is,

$$\Phi_c(s) = \frac{K_{p0}}{Ls + K_{p0}}. \tag{10}$$

The closed loop transfer function shown in formula (10) is a typical first-order inertia link, and its control bandwidth is $\omega = K_{p0}/L$; that is, the cut-off frequency of the transfer function is $f_c = K_{p0}/2\pi L$. When L is constant, the bigger K_{p0} is, the bigger bandwidth ω is, which represents that the response speed of current loop is faster; when K_{p0} is constant, the bigger L is, the bigger bandwidth ω is, which represents that the response speed of current loop is slower.

The bode diagram of fundamental close loop control is given in Figure 7 for $L = 3$ mH and $K_{p0} = 1$, 10, 20. At the frequency of 0 Hz, the amplitude gain of the fundamental current is 1 without phase delay. However, the gain is rapidly attenuated outside 0 Hz. It indicates that the PI controller has the function of frequency selection for the DC current under the synchronous reference frame, which can achieve high precision control.

4.3. The Influence of Digital Control Delay. Digital control delay, including computation delay and PWM update link delay, will affect tracking performance of the current loop and even cause instability of the system. Thus, it is necessary to study the effect of control delay on the tracking performance of the current loop. The delay of the digital control is

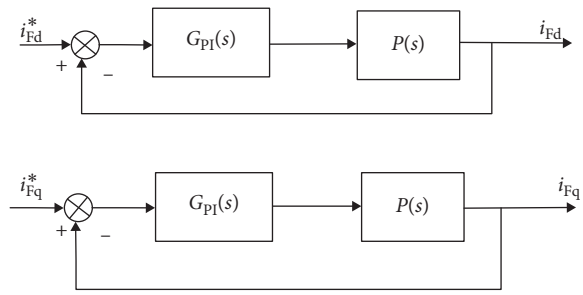


Figure 6: Fundamental current control block diagram based on PI controller.

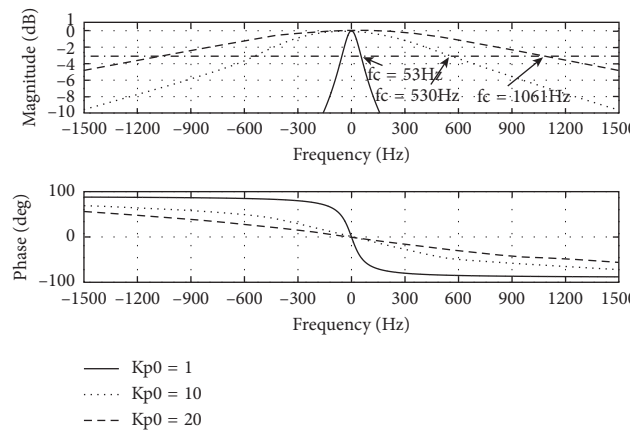


Figure 7: Bode diagram of fundamental close loop control.

generally 1.5 times of the sample period Ts [21], and the transfer function can be expressed as

$$G_d(s) = \frac{1}{1.5T_s * s + 1},$$

$$G_c(s) = \frac{\sum_{h=6n,n=1,2}^{5}\left(K_{ph}s/L\left(s^2 + \left(h\omega_s\right)^2\right)\left(1.5T_s s + 1\right)\right)}{1 + \sum_{h=6n,n=1,2}^{5}\left(K_{ph}s/L\left(s^2 + \left(h\omega_s\right)^2\right)\left(1.5T_s s + 1\right)\right)}. \tag{11}$$

Bode diagram of closed loop current considering digital control delay is shown in Figure 8 for $L = 3$mH, $T_s = 10^{-4}$ s, $K_{ph} = 0.4$. Even if affected by the digital control delay, the current loop has 35° of phase margin, which is still stable. In addition, the phase shift is still 0 at every positive and negative sequence harmonic frequency, which indicates that the digital control delay has less influence on the system and the current loop still has high static control accuracy.

4.4. Design of Control System. The control block diagram of the three-phase three-wire SAPF for the proposed method is shown in Figure 9. The PI control is used to maintain DC-link voltage stability in the external voltage loop. The difference between the reference voltage u_{dc}^* and the actual voltage u_{dc} is input to the PI controller and the output of PI controller as a part of active power loss is added to the active source current component. PI and VR control is used in the internal current loop. The harmonic currents i_{hd}^* and i_{hq}^*

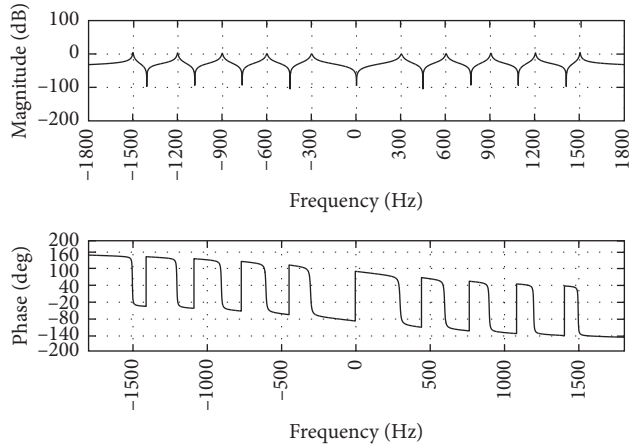


Figure 8: Bode diagram of closed loop current considering digital control delay.

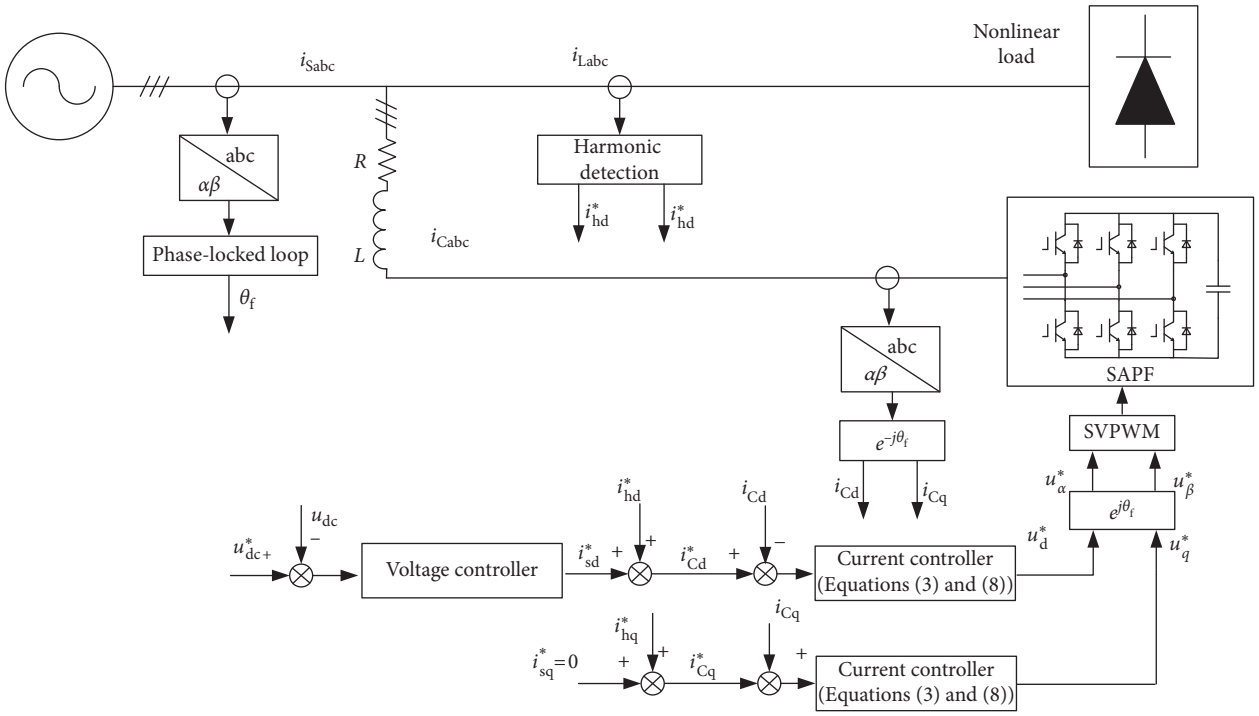


Figure 9: Control block diagram of three-phase three-wire SAPF.

extracted from the load current i_{Labc} by instantaneous reactive power theory is added to the output of the PI controller i^*_{sd} and i^*_{sq}. Compensation current i_{Cabc} is turned to i_{cd} and i_{cq} based on synchronous coordinate transformation; then the difference between i_{cd}, i_{cq} and i^*_{cd}, i^*_{cq} is input to the current controller; besides, the control pulse signal required by SAPF is obtained by the space vector pulse width modulation (SVPWM) to compensate the harmonic currents [22].

5. Simulation and Experimental Results

In order to verify the correctness and effectiveness of the proposed current control method based on PI and multi-VR control in this paper, both classical PI controller and PI + multi-VR controller are designed according to the above-mentioned method in Matlab/Simulink. The simulation model parameters are shown in Table 1.

Table 1: Simulation model parameters.

Parameter	Value
Source voltage V_{snom}	220 V, 50 Hz
DC-link voltage V_{dcref}	750 V
DC-link capacitance C	1000 μF
Filter inductance L_f	3 mH
Equivalent loss resistance R_f	0.3 Ω
Nonlinear load	Three-phase diode bridge rectifier with a 10 Ω DC resistor

Since both of the power supply and the nonlinear load are three-phase symmetry, the A phase is only analyzed in

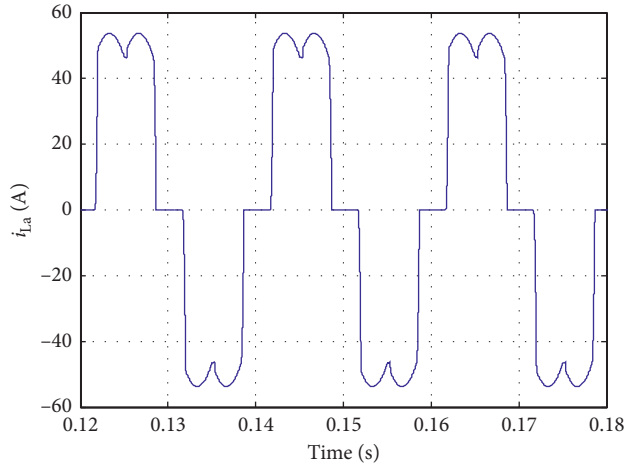


Figure 10: Waveform of nonlinear load current.

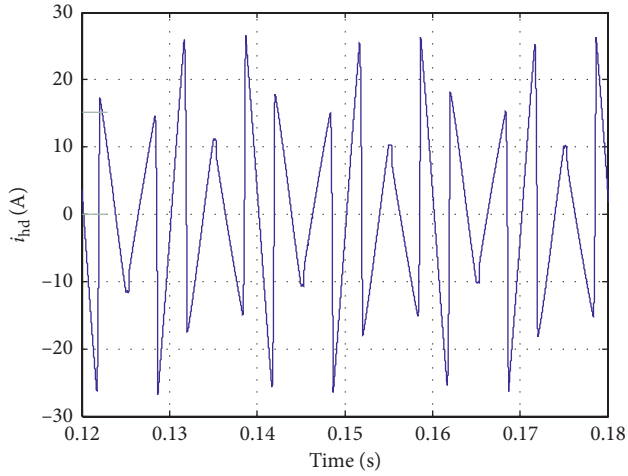


Figure 11: Waveform of harmonic currents.

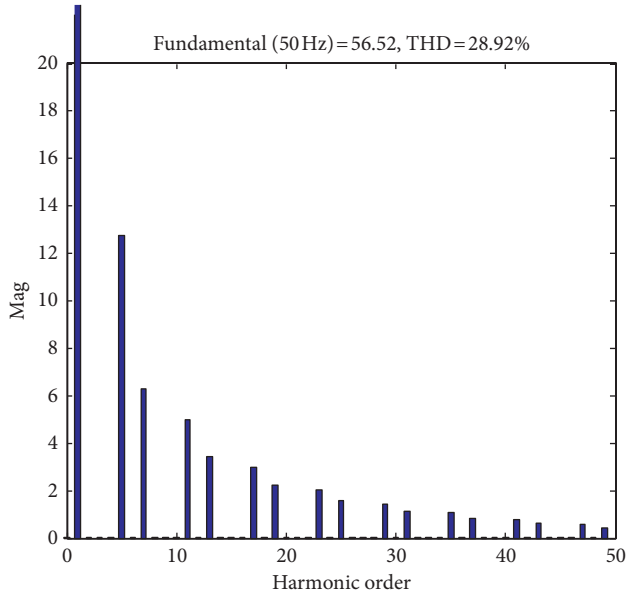


Figure 12: FFT analysis of nonlinear load current.

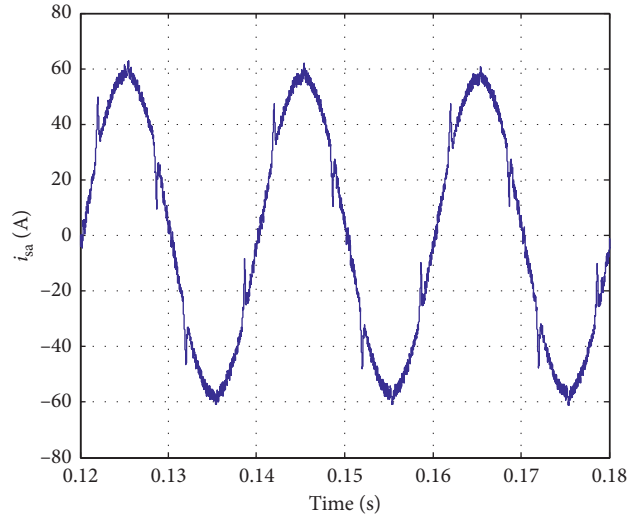


Figure 13: Waveform of source current using PI controller.

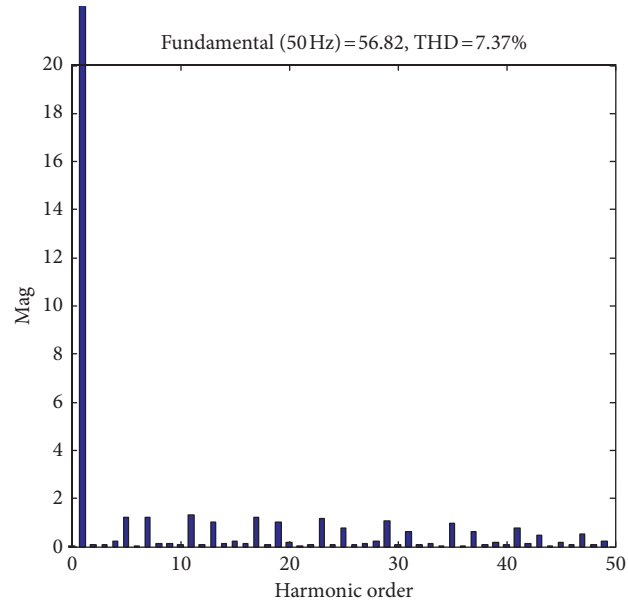


Figure 14: FFT analysis of source current using PI controller.

the simulation waveform. The waveform of the load current and harmonic currents are depicted in Figures 10 and 11, and the FFT analysis of the nonlinear load current are shown in Figure 12. From Figure 11, the total harmonic distortion (THD) before compensation is up to 28.92%, and the load current's harmonic spectrum contains harmonics of the order $h = 6n \pm 1, n = 1, 2, \ldots$.

The compensation performance using PI controller is shown in Figures 13 and 14, respectively. The compensation results of the proposed control strategy based on PI and 6th VR controller are shown in Figures 15 and 16, respectively. Comparing the four figures, PI controller can compensate a part of harmonic, which is not too fruitful. After adopting the 6th of the VR controller, the 5th harmonic and 7th harmonic can be compensated effectively. 5th harmonic is reduced to 0.28% from 2.08%. 7th harmonic is reduced to

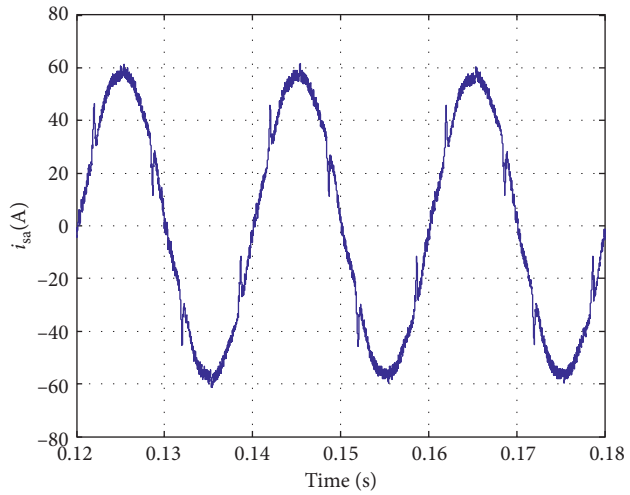


Figure 15: Waveform of source current using PI controller and 6th VR controller.

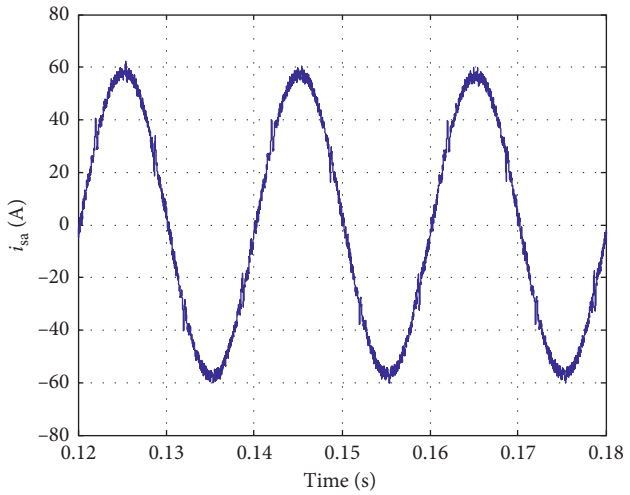


Figure 17: Waveform of source current using PI controller and multi-VR controllers.

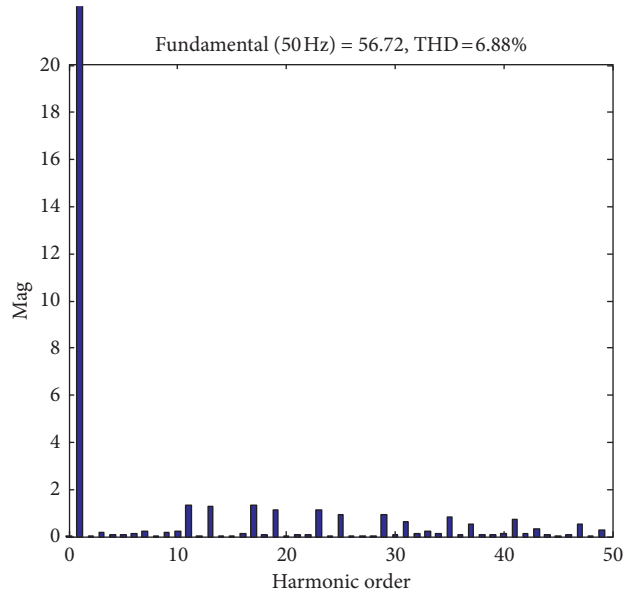


Figure 16: FFT analysis of nonlinear load current using PI controller and 6th VR controller.

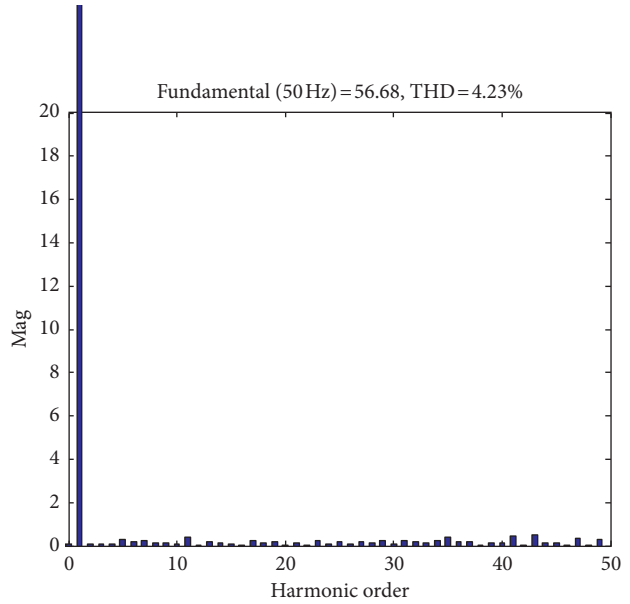


Figure 18: FFT analysis of nonlinear load current using PI controller and multi-VR controllers.

0.11% from 2.16%, but distortion rate of other harmonics remains the same. The simulation results show that the 6th resonant controller has good inhibitory effects on 5th harmonic and 7th harmonic, which can further improve the compensation performance for some specific harmonics.

The compensation results using PI controller and multi-VR controller are shown in Figures 17 and 18. When the PI and multi-VR controllers are introduced in the control system, distortion rate of each harmonic decreases remarkably.

The experimental waveforms based on PI + multi-VR controllers proposed in the case of abrupt loading is shown in Figure 19. It is known from Figure 19 that at 0.3 s, a three-phase diode rectifier of 20 kW is added to the system, and the SAPF can still track the abrupt load current quickly. After about one fundamental period, the system reaches stability. It shows that the proposed control strategy has good dynamic performance.

In order to further verify the effectiveness of the proposed strategy, a SAPF prototype of 15 kVA is built. The main control chip is TMS320F28335 of TI company. PM50RL1B120 produced by Mitsubshi is used as power devices of the main circuit. In the process of prototype testing, the experimental waveform is recorded by the DPO3014 digital fluorescence oscilloscope produced by the Tektronix Inc in the United States, and the harmonic data are recorded by PM3000A Power Quality Analyzer produced by Voltech Inc. Experimental setups of SAPF are shown as Figure 20. The experimental parameters are as follows:

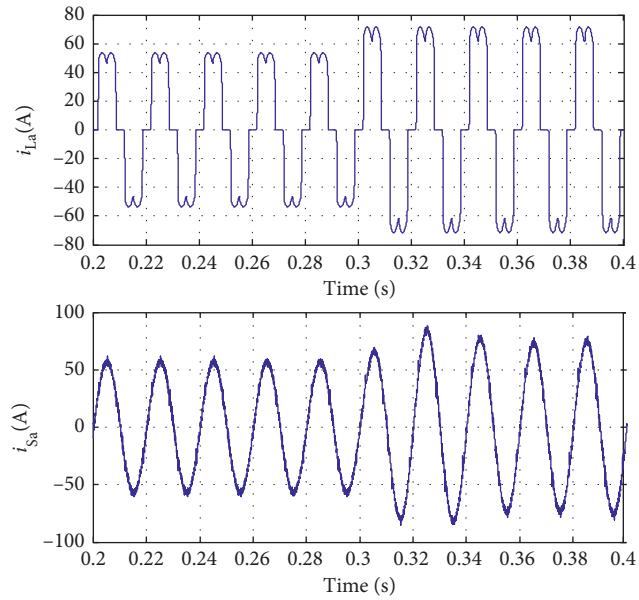
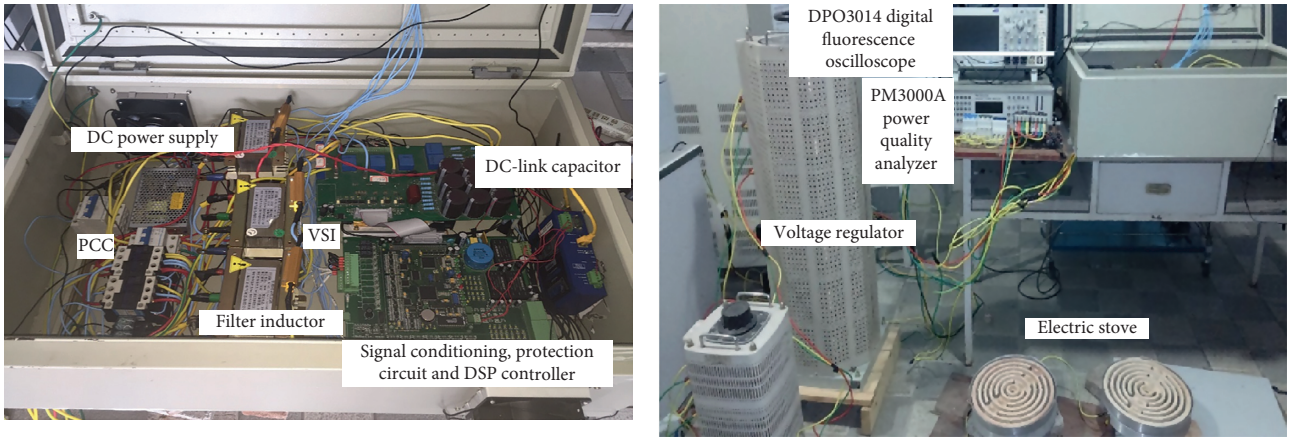


Figure 19: Waveforms of load current and source current in the case of abrupt loading.



(a) (b)

Figure 20: Experimental setups of SAPF.

(i) Three-phase source voltage: $U_N = 380$ V and $f = 50$ Hz

(ii) Nonlinear load: two-way three-phase diode rectifier with two series two parallel(2S2P) electric stoves of 5 kW in DC link and a three-phase voltage regulator with a rated power of 15 kVA, rated voltage p of 380 V, and output voltage of 220 V in AC link

(iii) Switching frequency of IGBT: 10 kHz

(iv) Voltage controller parameters: ratio coefficient $Kp = 0.1$ and integral coefficient $Ki = 10$

(v) Current controller parameters: $K_{p0} = 0.5$, $K_i = 160$, $K_{p6} = 0.2$, $K_{i6} = 200$, $K_{p12} = 0.2$, $K_{i12} = 200$, $K_{p18} = 0.5$, $K_{i18} = 200$, and so on

(vi) Other experimental parameters: the parameters including DC-link voltage, DC link capacitance, and filter inductance are consistent to the simulation parameters

Experimental steady waves using PI controller and PI + multi-VR controllers are shown in Figures 21 and 22. Waveform 2 represents load current, THD of which is 26.1%. Waveform 4 in Figures 21 and 22 represent source current after compensation based on PI controller and PI + multi-VR controllers. Evidently, both of source currents approach nearly sinusoidal by SAPF. However from Table 2, the THD of the source current reduces from 7.34% to 2.86% by using the proposed control strategy. The above results show that the proposed control strategy has good steady performance and control accuracy.

Experimental dynamic results are shown in Figure 23. Before the time of 0.04 s, the SAPF has been invested in the system to finish the harmonic current detection. Besides, voltage controller has been working steadily and DC-link

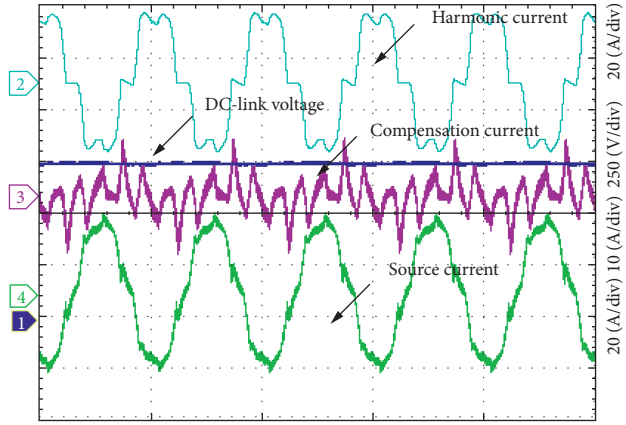


Figure 21: Experimental steady waves using PI controller.

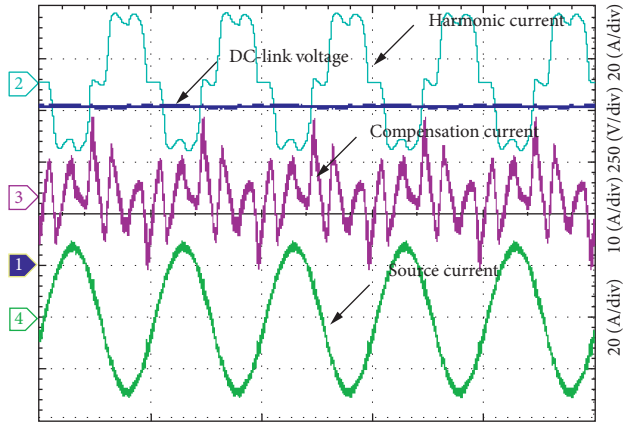


Figure 22: Experimental steady waves for proposed scheme.

Table 2: Compensation results with two control algorithms.

Order of harmonic		5	7	11	13	17	19	THD (%)
Harmonic distortion before compensation (%)		21.3	9.87	5.60	3.36	1.80	0.92	26.1
Harmonic distortion after compensation (%)	With PI controller	2.16	1.86	1.76	1.80	1.74	1.82	7.34
	With the proposed method	0.72	0.48	0.35	0.2	0.18	0.10	2.86

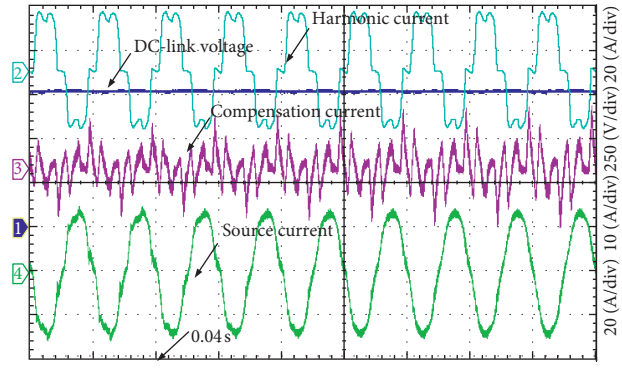


Figure 23: Experimental dynamic waveform after adding VR controller.

voltage has been stabilized at 750 V. Moreover, the basic control loop of current controller or PI control has also been run. At the time of 0.04 s, the multi-VR controllers start running. After about 3 fundamental periods, the system enters the new steady state. Experimental results show that the proposed strategy also has good dynamic performance.

6. Conclusion

With development of power electronic technology, a large number of power electronic devices are integrated into the power grid, which causes the harmonic pollution. Through the study on SAPF mathematical model and the principle of VR controller, a current control strategy based on PI and multi-VR controller is proposed in this paper. Through detailed analysis on frequency response characteristic of current closed loop, in that the PI and VR controller can compensate the harmonic currents with zero steady-state error, little phase delay and good dynamic performance are proved. In addition, under the synchronous reference frame, the proposed method is simple enough to compensate the harmonic, which reduces the computation and is better adapted to frequency fluctuation. The simulation and experimental results show that the proposed control strategy is correct and effective, which improves the power quality.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

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Research Article

A Double Update PWM Method to Improve Robustness for the Deadbeat Current Controller in Three-Phase Grid-Connected System

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In the grid-connected inverter based on the deadbeat current control, the filter inductance variation and single update PWM affect the distortion of the grid current, stability, and dynamic of the system. For this, a double update PWM method for the deadbeat current controller in three-phase grid-connected system is proposed, which not only effectively decreases the grid current distortion and control delay, but also improves the system stability and dynamic response speed due to reducing the characteristic root equation order of the closed-loop transfer function. The influence of the filter inductance deviation coefficient on the system performance is analyzed. As a conclusion, the corresponding filter inductance deviation coefficient in the system critical stability increases with increase in the parasitic resistance of the filter inductance and line equivalent resistance and decreases with increase in the sampling frequency. Considering the system stability and dynamic response, the optimal range of the control parameters is acquired. Simulation and experimental results verify the effectiveness of the proposed method.

1. Introduction

With the increasingly serious energy crisis and environmental pollution, renewable energy distributed generation technology has been widely concerned and researched in [1–4]. The grid-connected inverter is the core of the distributed generation system in [5–8]. Its role is to convert the DC power generated by renewable energy to the AC power accepted by the grid. The deadbeat current control is based on the mathematical model of the grid-connected inverter and depends on the actual electrical parameters of the main circuit. Theoretically, no static-state error can be achieved in [9–12]. Because of its fast current transient response, accurate current tracking characteristic, and all digital control, the deadbeat current control has been applied more often.

However, reliance on the accurate electrical model and control delay are the main constraints in the deadbeat control. On the one hand, the filter inductance value cannot be accurately detected. Even with the increasing of the grid current, the magnetic flux of the filter inductance tends to be saturated, resulting in the decrease of the filter inductance. This will lead to a certain deviation between the model filter inductance and actual filter inductance, affect the control accuracy of the deadbeat control, and cause the grid current distortion in [13, 14]. On the other hand, the inherent delay of the sampling and calculation limits the maximum duty cycle of the grid-connected inverter. For this, the delay caused by the proposed single update PWM in [15] may increase poles of the open-loop pulse transfer function, which affects the stability and dynamic response speed of the system. Therefore, how to improve the stability and dynamic response speed of the system and decrease the distortion of the grid current has become the research focus and goal of the grid-connected inverter.

In [16], a current prediction control method for the inductance online identification is proposed, which can accurately identify the inductance value in static and dynamic processes. An online estimation method of the filter inductance parameter is proposed in [17], which can prevent the current phase difference and system instability when the filter inductance parameter is not matched by the traditional prediction deadbeat current control method. However, the delay caused by the single update PWM has not been considered in the above methods.

The predictive current control technology is proposed to compensate the delay in [15, 18–20]. A supply current predictive controller that adopts the variable step-size adaptive algorithm is proposed in [15], which solves the problem that the maximum duty is limited by the delay caused by the sampling and calculation. Because the weighted coefficient is regulated by the error calculated in each sampling period, this algorithm shows well predictive accuracy. But a single voltage vector is only used in a control cycle, so it needs very high sampling frequency to get good performance [18]. In [19, 20], the linear prediction method is proposed, which can estimate the information of the next beat based on the control object model and the information of the current and past period. Although it eliminates the control delay, this method depends on the accuracy of the model, which may exist a certain estimation error.

At the same time, the current observer is used to predict the next beat current in [10, 21, 22], and the current reference is predicted in advance to compensate for the delay. In [10, 21], the current predictive algorithm based on repetitive control observer is proposed, which solves the problem of the current instability caused by the control delay and improves the current predictive precision. However, this method does not involve the dynamic analysis. In [22], an improved deadbeat current control scheme with a novel adaptive self-tuning load model is proposed. An improved deadbeat current controller with delay compensation is used to achieve high bandwidth current control characteristic, which compensates for the delay of the total system. However, a single prediction algorithm is adopted in the current reference variation, which may cause a large current overshoot or phase lag and deteriorate the system performance.

Digital PWM in double update mode is used to reduce the modulation delays and achieve performance. In [23], the effects of the measurement sampling and PWM updating methods on PI-based current control performance have been studied for a converter system. Reference [24] proposed proportional resonant controller implementation with double update mode digital PWM for single-phase grid-connected inverter. Digitally controlled grid-connected inverters with converter current control scheme and converter current plus grid current control scheme have been studied in [25]. A combination of two samples' time displacement and the line current PWM ripple was proposed to cancel that error and boost the performance of such drives in [26]. Reference [27] demonstrated the improved performance of a three-phase voltage source inverter when digital multi-sampled space vector modulation was used. The bandwidth expansion strategy was proposed to achieve the stator current double sampling and PWM duty cycle double update in a carrier period in [28]. However, the deadbeat current control has not been considered in the above methods. A fast robust PWM method for photovoltaic grid-connected inverter is proposed in [29], which effectively solves the delay of the one-step-delay control and improves the system stability.

In this paper, the double update PWM method to improve robustness for the deadbeat current controller in three-phase grid-connected system is proposed. The paper is organized as follows. Section 2 presents the structure and control method for three-phase grid-connected system. The double update PWM method for the deadbeat current controller is proposed in Section 3. Finally, simulations and experiments are illustrated and discussed in Sections 4 and 5. Some conclusions are given in Section 6.

2. Control Method for Three-Phase Grid-Connected System

Structure of photovoltaic grid-connected system is shown in Figure 1, including the photovoltaic array, inverter circuit, and LC filter. C_{dc} is the DC side storage capacitance, which is used to stabilize the DC voltage U_{dc}. The power transistors Q_1-Q_6 constitute a three-phase full bridge inverter circuit that converts the DC voltage U_{dc} into the AC output voltage, which is the same as the amplitude and phase of the grid voltage. LC filter is formed by the inductance L and capacitance C. In the grid-connected mode, LC filter is equivalent to a single filter inductance. The resistance r is the sum of the parasitic resistance of the filter inductance L and line equivalent resistance. I_{dc} is the DC current. $i_{inv\,j}$ (j=a,b,c) is the inverter output current. i_{gj} is the grid current. Since the current flowing through the filter capacitance C is small, $i_{inv\,j}$ is approximately equal to i_{gj}.

Diagram of the double update PWM method for the deadbeat current controller is shown in Figure 2, including the double closed-loop control and double update PWM. The outer voltage loop adopts the PI control to stabilize U_{dc}. The inner current loop adopts the deadbeat control, which decreases the distortion of the grid current caused by the filter inductance variation. The double update PWM effectively solves the delay caused by the single update PWM and improves the stability and dynamic response speed of the system. U_{dcr} is the DC voltage command, u_{gj} is the grid voltage, ω_1 is the fundamental angular frequency of the grid, I_{gr} is the input amplitude command of the inner current loop, i_{gjr} is the grid current command, and D_j is the equivalent duty cycle.

3. The Double Update PWM Method for the Deadbeat Current Controller

3.1. The Single Update PWM Method. In digital control, the single update PWM is shown in Figure 3, where u_{ms} is the single update PWM wave. The sampling is carried out at the peak of the (k-1)th triangular carrier. The calculation is based on the sampling value. At the peak of the kth triangular carrier, the single update PWM wave $u_{ms}(k\text{-}1)$ of the (k-1)th

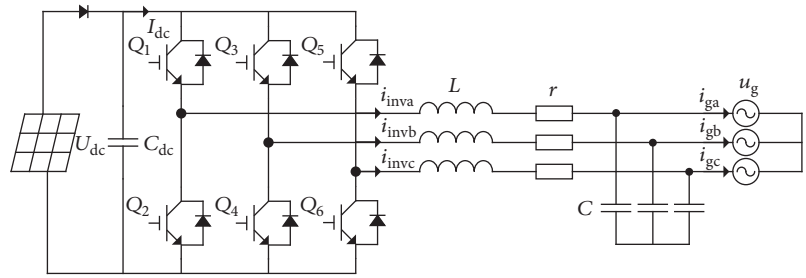


Figure 1: Structure of photovoltaic grid-connected system.

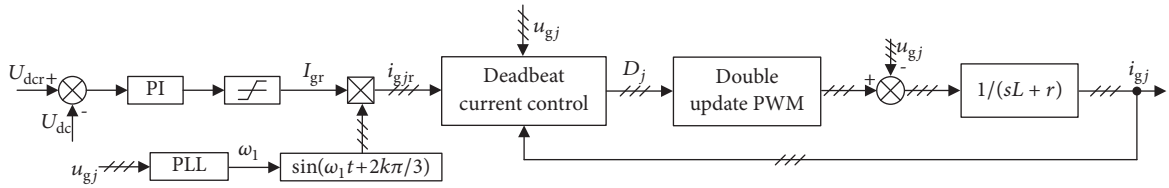


Figure 2: Diagram of the double update PWM method for photovoltaic grid-connected inverter based on the deadbeat control.

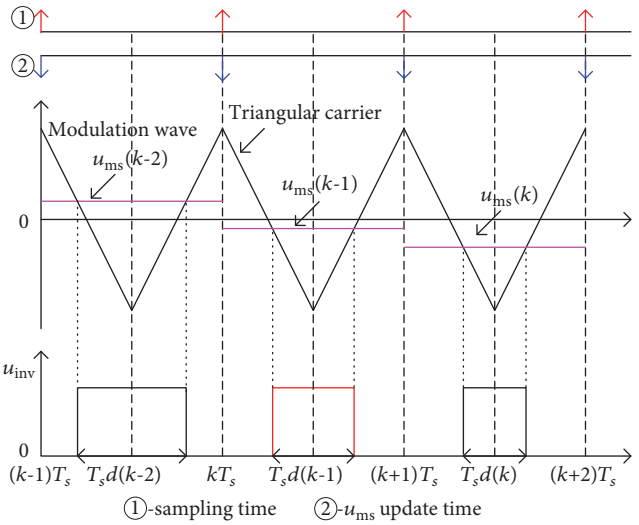


Figure 3: The single update PWM.

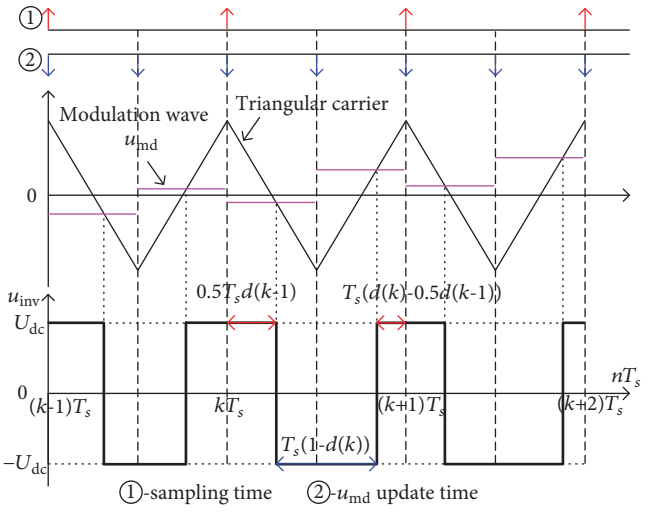


Figure 4: The double update PWM method.

carrier cycle is loaded. So the equivalent duty cycle $D(k)$ of the kth carrier cycle can be expressed as

$$D(k) = d(k-1) \tag{1}$$

where $d(k\text{-}1)$ is the duty cycle calculated by the sampling values at the peak of the $(k\text{-}1)$th triangular carrier.

Obviously, the loading time of the single update PWM wave is lagged behind a sampling period at the beginning of the sampling. So the one-step delay is caused by the single update PWM.

3.2. The Double Update PWM Method. The double update PWM method is shown in Figure 4, where u_{md} is the double update PWM wave. The sampling is carried out at the peak of the triangular carrier. The loading is carried out at the peak and valley of the triangular carrier. That is to say, one sampling and double loading are taken in each carrier cycle. The modulation process is as follows: the sampling is carried out at the peak of the kth triangular carrier. Meanwhile, the double update PWM wave corresponding to the $d(k\text{-}1)$ is loaded, so that the conduction time of the first half of the carrier cycle is $0.5T_s d(k\text{-}1)$. At the valley of the kth triangular carrier, the double update PWM wave corresponding to the difference calculated by subtracting the $d(k\text{-}1)$ from the $2d(k)$ is loaded, so that the conduction time of the second half of the carrier cycle is $T_s(d(k)\text{-}0.5d(k\text{-}1))$. So the equivalent duty cycle $D(k)$ of the kth carrier cycle can be expressed as

$$\begin{aligned} D(k) &= \frac{0.5T_s d(k-1) + T_s(d(k) - 0.5d(k-1))}{T_s} \\ &= d(k) \end{aligned} \tag{2}$$

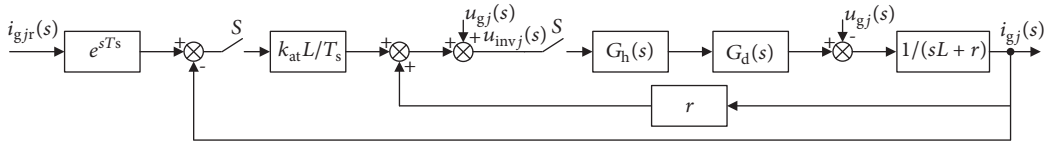


Figure 5: Diagram of the deadbeat current control for the grid-connected inverter.

Table 1: The delay comparison between the single update PWM and proposed method.

Serial number	$G_d(s)$	Method
Case 1	e^{-sTs}	Single update PWM
Case 2	1	Proposed(double update PWM)

where $d(k)$ is the duty cycle calculated by the sampling values at the peak of the kth triangular carrier.

Therefore, the proposed double update PWM method eliminates the control delay. Meanwhile, the time margin of the sampling and calculation decreases from T_s to $T_s/2$.

Diagram of the deadbeat current control for the grid-connected inverter is shown in Figure 5, where $i_{gjr}(s)$ is the input quantity, $u_{gj}(s)$ is the disturbance input quantity, $i_{gj}(s)$ is the output quantity, T_s is the sampling cycle, and S is the synchronous sampling switch. With the increasing of the grid current, the magnetic flux of the filter inductance tends to be saturated, resulting in the decrease of the filter inductance. There is the deviation between the filter inductance L_1 and actual filter inductance L. k_{at} is the filter inductance deviation coefficient. $k_{at}=L_1/L$. $G_h(s)$ is the continuous domain transfer function of the zero order holder (ZOH).

$$G_h(s) = \frac{\left(1 - e^{-sT_s}\right)}{s} \tag{3}$$

$G_d(s)$ is the continuous domain transfer function of the single update PWM, which can be expressed as

$$G_d(s) = e^{-sT_s} \tag{4}$$

The delay comparison between the single update PWM and proposed method is shown in Table 1. Considering the parasitic resistance of the filter inductance and line equivalent resistance, the influence of the control delay on the stability and dynamic of the system is analyzed, and the appropriate control parameter range is given.

3.3. Control System Stability Analysis. In Figure 5, using the single update PWM, $G_d(s)=e^{-sTs}$. $i^*_{gj}(s)$ is Laplace transform of $i_{gj}(s)$, which can be expressed as

$$i^*_{gj}(s) = \frac{k_{at}\left(L/T_s\right)\cdot G_h G_d G^*_L(s)}{1 + \left(k_{at}L/T_s - r\right)\cdot G_h G_d G^*_L(s)} \cdot e^{sT_s} \cdot i^*_{gjr}(s) \tag{5}$$

where $G_L(s)$ is the transfer function of the filter, $G_L(s)=sL+r$, $G_h G_d G_L{}^*(s)$ is Laplace transform of $G_h(s)G_d(s)G_L(s)$, and $i^*{}_{gjr}(s)$ is Laplace transform of the input quantity $i_{gjr}(s)$. By substituting $z=e^{-sTs}$ into (5), the closed-loop pulse transfer function in the z domain is obtained using the single update PWM.

$$\Phi(z) = \frac{k_{at}\left(L/T_s\right)\left(1 - e^{-T_s r/L}\right)\cdot z}{r\left(z - e^{-T_s r/L}\right)z + \left(k_{at}L/T_s - r\right)\left(1 - e^{-T_s r/L}\right)} \tag{6}$$

By substituting $z=(\omega+1)/(\omega-1)$ into (6), the characteristic root equation of the closed-loop transfer function of the system can be obtained as

$$\begin{aligned} &A\omega^2 + B\omega + C = 0 \\ &A = k_{at}\left(\frac{L}{T_s}\right)\left(1 - e^{-T_s r/L}\right) \\ &B = 2r - 2\left(k_{at}\frac{L}{T_s} - r\right)\left(1 - e^{-T_s r/L}\right) \\ &C = r\left(1 + e^{-T_s r/L}\right) \\ &\quad + \left(k_{at}\frac{L}{T_s} - r\right)\left(1 - e^{-T_s r/L}\right) \end{aligned} \tag{7}$$

where ω is transform operator from the z domain to the ω domain.

Based on the Routh criterion [30], the range of the filter inductance deviation coefficient k_{at} can be expressed as

$$0 < k_{at} < \frac{r\left(2 - e^{-T_s r/L}\right)}{1 - e^{-T_s r/L}}\frac{T_s}{L} \tag{8}$$

In Figure 5, using the proposed method, $G_d(s)=1$. The closed-loop pulse transfer function in the z domain can be expressed as

$$\Phi(z) = \frac{k_{at}\left(L/T_s\right)\left(1 - e^{-T_s r/L}\right)\cdot z}{r\left(z - e^{-T_s r/L}\right) + \left(k_{at}L/T_s - r\right)\left(1 - e^{-T_s r/L}\right)} \tag{9}$$

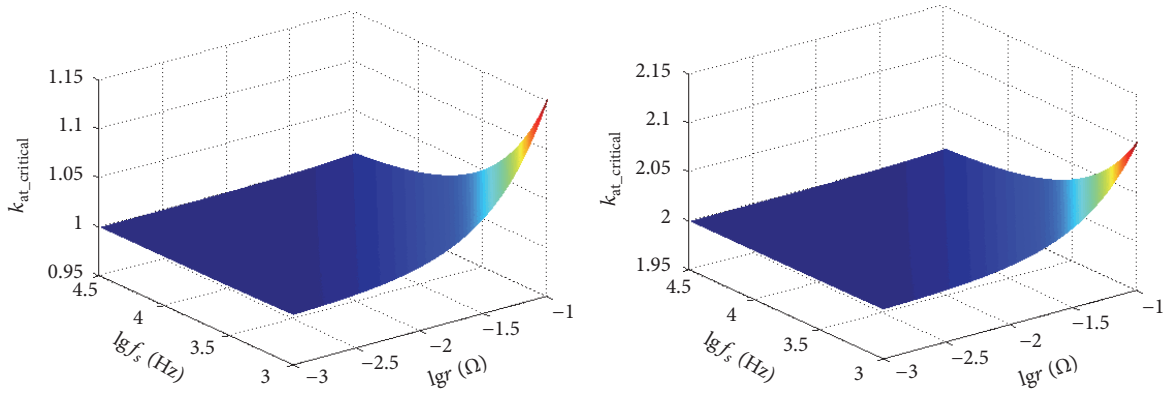
In (6) and (9), compared to the single update PWM, the characteristic root equation order of the closed-loop transfer function of the system is reduced when the proposed method is used.

When $|z| < 1$, the system is stable and the range of the filter inductance deviation coefficient k_{at} can be expressed as

$$0 < k_{at} < \frac{2r}{1 - e^{-T_s r/L}}\frac{T_s}{L} \tag{10}$$

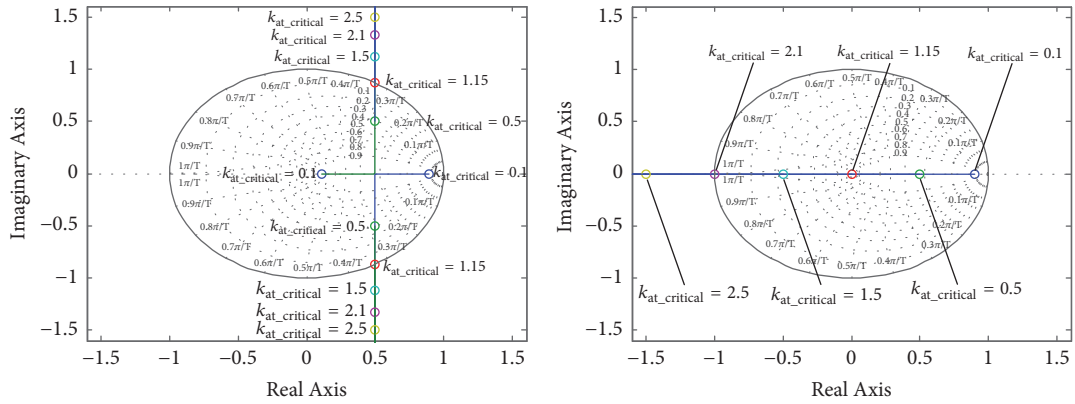
The corresponding filter inductance deviation coefficient in the system critical stability $k_{at\_critical}$ can be expressed as

$$k_{at\_critical} = \frac{2r}{1 - e^{-T_s r/L}}\frac{T_s}{L} \tag{11}$$



(a) Single update PWM (b) Double update PWM

FIGURE 6: Relationship among the resistance r, sampling frequency f_s, and $k_{at\_critical}$.



(a) Single update PWM (b) Double update PWM

FIGURE 7: The contrast analysis of root locus with different $k_{at\_critical}$.

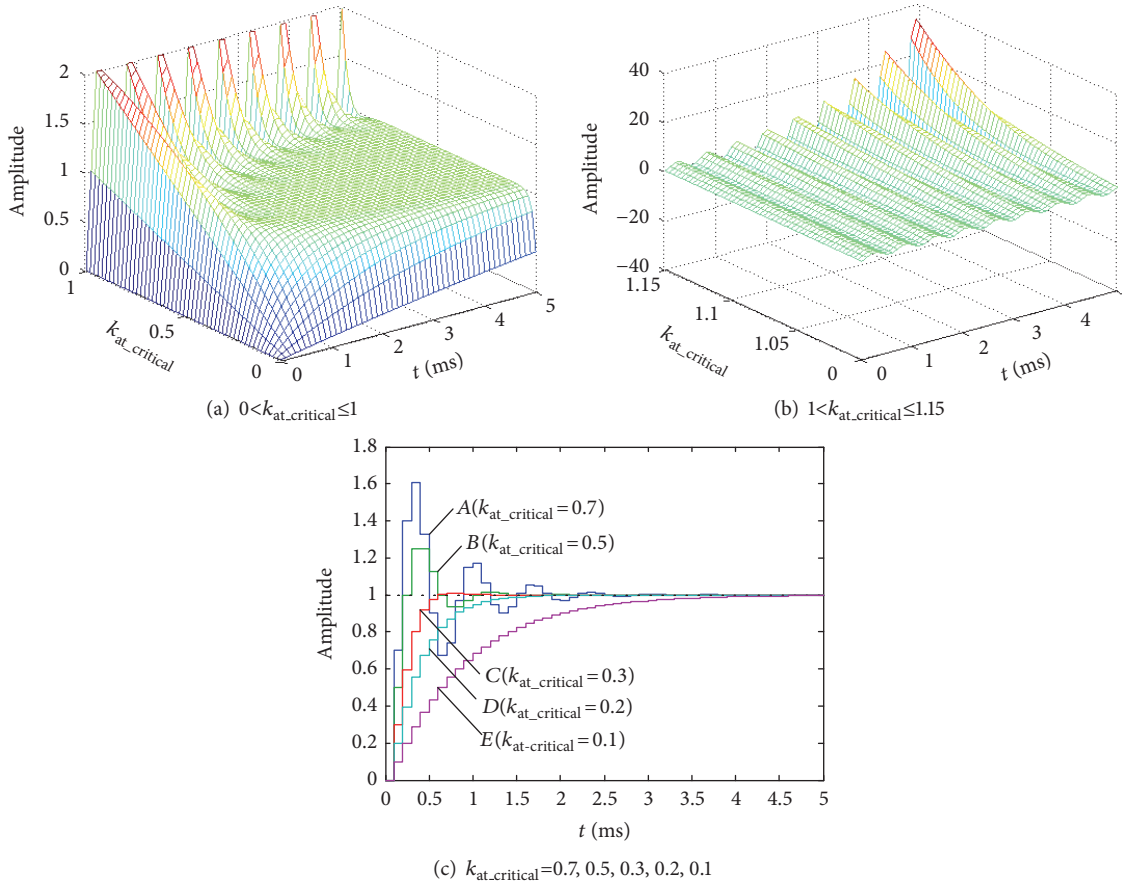
Relationship among the resistance r, sampling frequency f_s, and $k_{at\_critical}$ by the single update PWM and proposed method is shown in Figure 6. Figures 6(a) and 6(b) correspond to the single update PWM and proposed method, respectively. When f_s is constant, $k_{at\_critical}$ increases with increase in r. When r is constant, $k_{at\_critical}$ decreases with increase in f_s. When the proposed method is used, the range of $k_{at\_critical}$ is $0< k_{at\_critical} \leq 2.1$, while the range of $k_{at\_critical}$ is $0< k_{at\_critical} \leq 1.15$ by using the single update PWM. So the range of $k_{at\_critical}$ by using the proposed method is obviously larger than the range of $k_{at\_critical}$ by using the single update PWM.

When $k_{at\_critical}$=0.1, 0.5, 1.15, 1.5, 2.1, and 2.5, the root locus analysis with the single update PWM and proposed method is shown in Figure 7. Figures 7(a) and 7(b) correspond to the single update PWM and proposed method, respectively. In Figure 7(a), when $k_{at\_critical}$=0.1 and 0.5, the pole is inside the unit circle, and the system is in a stable state. When $k_{at\_critical}$=1.15, the pole is on the unit circle, and the system is in a critical stable state. When $k_{at\_critical}$=2.1 and 2.5, the pole is outside the unit circle, and the system is in an unstable state.

In Figure 7(b), when $k_{at\_critical}$=0.1, 0.5, 1.15, and 1.5, the pole is inside the unit circle, and the system is in a stable state. When $k_{at\_critical}$=2.1, the pole is on the unit circle, and the system is in a critical stable state. When $k_{at\_critical}$=2.5, the pole is outside the unit circle, and the system is in an unstable state. So the range of $k_{at\_critical}$ by using the proposed method is obviously larger than the range of $k_{at\_critical}$ by using the single update PWM.

3.4. Control System Dynamic Analysis. When the single update PWM is used, system response to unit step change with $k_{at\_critical}$ changing is shown in Figure 8, while the sampling frequency f_s=10kHz and resistance r=0.01Ω are constant. Figures 8(a) and 8(b) correspond to $0< k_{at\_critical} \leq 1$ and $1< k_{at\_critical} \leq 1.15$, respectively. When $0< k_{at\_critical} \leq 1$, the dynamic response of the system is convergent. When $1< k_{at\_critical} \leq 1.15$, the dynamic response of the system is divergent. Therefore, the range of $k_{at\_critical}$ is $0< k_{at\_critical} \leq 1$.

In Figure 8(c), the curves A, B, C, D, E correspond to $k_{at\_critical}$=0.7, 0.5, 0.3, 0.2, 0.1, respectively. In curve C, the system has the best dynamic response and no overshoot when $k_{at\_critical}$ is equal to $k_{at\_critical0}$ ($k_{at\_critical}$=$k_{at\_critical0}$=0.3). In



(a) $0<k_{at\_critical}\leq 1$ (b) $1<k_{at\_critical}\leq 1.15$

(c) $k_{at\_critical}$=0.7, 0.5, 0.3, 0.2, 0.1

FIGURE 8: Single update PWM system response to unit step change with the constant sampling frequency f_s=10kHz and resistance r=0.01 when $k_{at\_critical}$ changes.

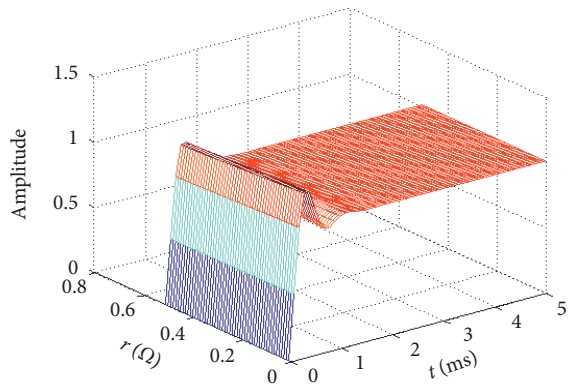


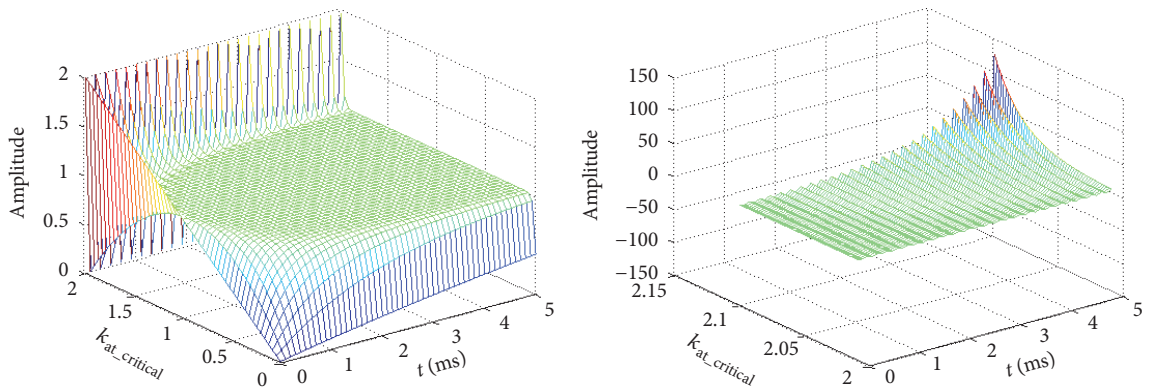
FIGURE 9: Single update PWM system response to unit step change with the constant sampling frequency f_s=10kHz and $k_{at\_critical}$=0.5 when the resistance r changes.

curves A and B, when $k_{at\_critical} > k_{at\_critical0}$, the closed-loop poles are conjugate complex poles located in the right half unit circle of the z plane, and the dynamic response of the system is the oscillation convergence pulse sequence. The smaller $k_{at\_critical}$ is, the closer poles are to the coordinate origin, the smaller the overshoot is, and the faster the response speed is. In curves D and E, when $k_{at\_critical} < k_{at\_critical0}$, the closed-loop poles are located in the real axis of the right half unit circle of the z plane. The dynamic response of the system is unidirectional positive convergence pulse sequence and has no overshoot. The larger $k_{at\_critical}$ is, the closer poles are to the coordinate origin, and the faster the response speed is.

When the single update PWM is used, system response to unit step change with the resistance r changing is shown in Figure 9, while the sampling frequency f_s=10kHz and $k_{at\_critical}$=0.5 are constant. When the resistance r changes, the peak time and the adjustment time of the system do not change much.

When the proposed method is used, system response to unit step change with $k_{at\_critical}$ changing is shown in Figure 10, while the sampling frequency f_s=10kHz and resistance r=0.01Ω are constant. Figures 10(a) and 10(b) correspond to $0< k_{at\_critical} \leq 2$ and $2< k_{at\_critical} \leq 2.1$, respectively. When $0< k_{at\_critical} \leq 2$, the dynamic response of the system is convergent. When $2< k_{at\_critical} \leq 2.1$, the dynamic response of the system is divergent. Therefore, the range of $k_{at\_critical}$ is $0< k_{at\_critical} \leq 2$.

Contrast analysis of system response to unit step change between the single update PWM and proposed method is shown in Figure 11. Curves A and B correspond to



(a) $0<k_{at\_critical}\leq 2$ (b) $2<k_{at\_critical}\leq 2.1$

FIGURE 10: Proposed control system response to unit step change with the constant sampling frequency f_s=10kHz and resistance r=0.01 when $k_{at\_critical}$ changes.

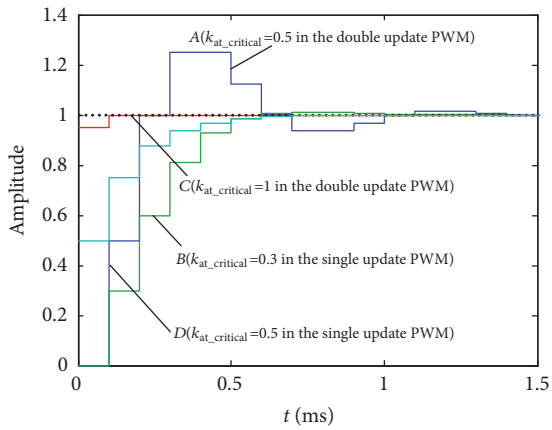


FIGURE 11: Contrast analysis of system response to unit step change between the single update PWM and proposed method.

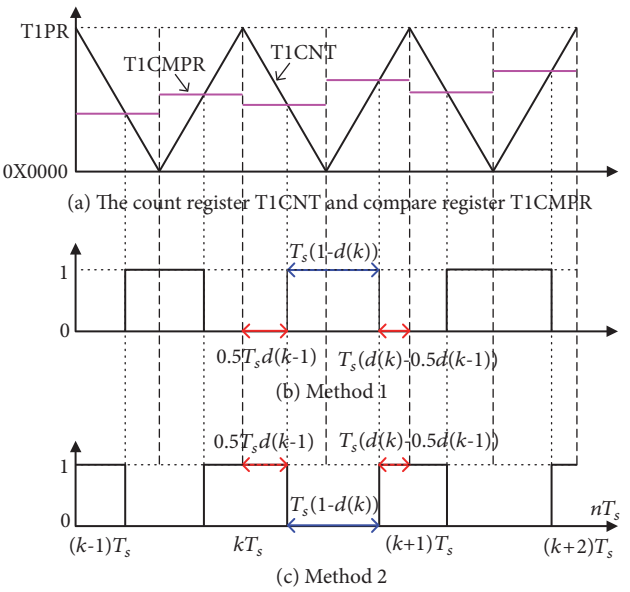
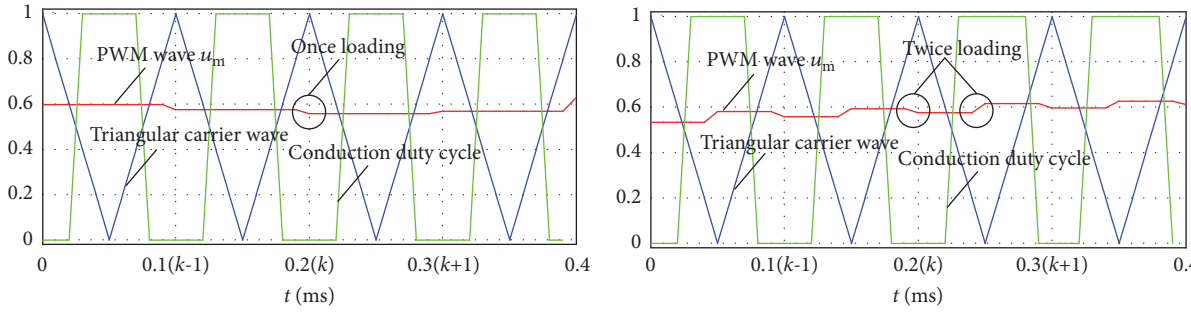


FIGURE 12: The implementation principle of the proposed modulation method based on the DSP2812 controller.

$k_{at\_critical}$=0.5 and 0.3 in the single update PWM, and curves C and D correspond to $k_{at\_critical}$=1 and 0.5 in the proposed method. Compared to curve D, the system has optimal response to unit step change, fast response speed, and no overshoot in curve C. Comparing curve C with curve B, the optimal response to unit step change of the system in curve C using the proposed method is superior. Comparing curve D with curve A, in curve A using the single update PWM, the unit step response of the system has overshoot, and the oscillation and adjustment time become longer, resulting in the poor dynamic of the system. In curve D using the proposed method, the unit step response of the system has no overshoot and the dynamic becomes better.

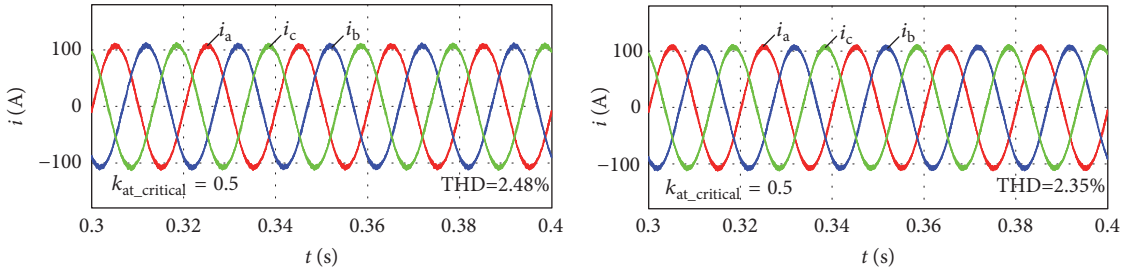
3.5. Project Implementation Design Method. The implementation principle of the proposed modulation method based on the DSP2812 controller is shown in Figure 12. DSP adopts TI's TMS320F2812 chip, which is a 32-bit fixed point micro control unit (MCU) with a main frequency of up to 150MHz. And the selected switching frequency is up to 10kHz. The general-purpose timer T1 is set to operate in continuous up/down counting mode. When the value of the count register T1CNT is equal to the period register T1PR, the timer T1 has a cycle interrupt, which starts the AD sampling unit, and (1-$d(k$-1))T1PR is assigned to the compare register T1CMPR. When the value of the count register T1CNT is 0x0000, the timer T1 has an underflow interrupt. The time margin from the start of the sampling to the end of the calculation is $0.5T_s$. The duty cycle $d(k)$ is obtained, and (1-2$d(k)$+$d(k$-1))T1PR is assigned to the compare register T1CMPR. When the value of the count register T1CNT is equal to the compare register T1CMPR, the compare match event occurs, and the level of the pin T1PWM will jump.

Method 1. The compare output pin T1PWM of the timer is set to active high in the DSP2812 controller. The DSP pin output driver signal is shown in Figure 12(b). The drive signal is sent



(a) Single update PWM (b) Double update PWM

Figure 13: The simulation waveforms of the modulation wave and triangular carrier wave.



(a) Single update PWM (b) Double update PWM

Figure 14: Steady state simulation waveforms of grid currents with $k_{at\_critical}$=0.5.

to the buffer for isolation and transformation. And then its level is reversed by the phase inverter. The final voltage signal is assigned to the corresponding IPM module.

Method 2. The compare output pin T1PWM of the timer is set to active low in the DSP2812 controller. The DSP pin output driver signal is shown in Figure 12(c). The drive signal is sent to the buffer for isolation and transformation. The final voltage signal is assigned to the corresponding IPM module.

4. Simulation Verification

In order to verify the effectiveness of proposed method, the simulation model of three-phase grid-connected inverter is built by using PSIM 9.0 based on Figure 1. The maximum output power of photovoltaic array is 50kW. System parameters are shown in Table 2.

In order to verify the implementation process of the proposed method, the simulation waveforms of the modulation wave and triangular carrier wave are shown in Figure 13. When the single update PWM and proposed method are used, the modulation processes are similar to the description of Figures 3 and 4. The correctness of the theoretical analysis is verified.

Steady state simulation waveforms of grid currents with $k_{at\_critical}$=0.5 and $k_{at\_critical}$=2 are shown in Figures 14 and 15, respectively. And the steady state simulation results of grid currents are shown in Table 3. In Figure 14(a), when the single update PWM is used with $k_{at\_critical}$=0.5, THD of the grid current is 2.48%. Meanwhile, in Figure 14(b), when the proposed method is used with $k_{at\_critical}$=0.5, THD of the grid current is 2.35%. Under the two modulation methods, the system is in a stable state.

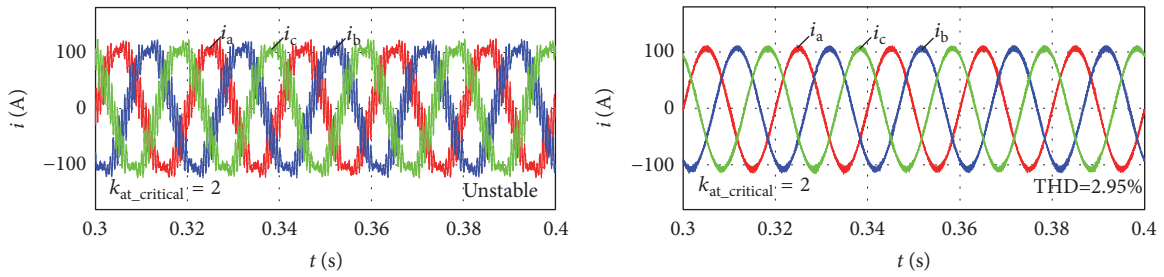
In Figure 15(a), when the single update PWM is used with $k_{at\_critical}$=2, the system is in an unstable state. However, in Figure 15(b), when the proposed method is used with $k_{at\_critical}$=2, THD of the grid current is 2.95%, and the system

Table 2: System parameters.

Parameters and units	Values
DC Voltage U_{dc} [V]	700
DC side storage capacitance C_{dc} [μF]	6000
Filter inductance L [mH]	1.0
Resistance r [Ω]	0.01
Outer voltage loop k_p, k_i	1.5, 0.3
Fundamental frequency f_1 [Hz]	50
Sampling frequency f_s [kHz]	10
Switching frequency f_{sw} [kHz]	10
Carrier frequency f_{tri} [kHz]	10

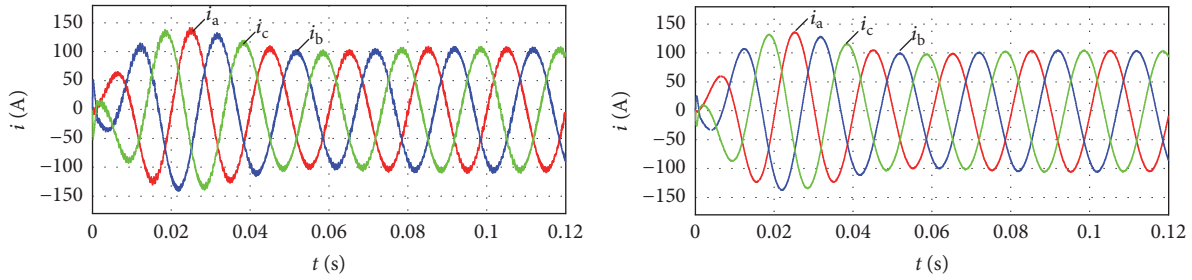
Table 3: The steady state simulation results of grid currents.

Method	$k_{at\_critical}$	THD
Single update PWM	0.5	2.48%
Proposed method	0.5	2.35%
Single update PWM	2	unstable
Proposed method	2	2.95%



(a) Single update PWM (b) Double update PWM

Figure 15: Steady state simulation waveforms of grid currents with $k_{at\_critical}$=2.



(a) Single update PWM (b) Double update PWM

Figure 16: The dynamic simulation waveforms of grid currents.

Table 4: The dynamic simulation results of grid currents.

Method	Grid inrush current	THD
Single update PWM	50A	2.7%
Proposed method	25A	1.8%

is in a stable state. Therefore, if the value of $k_{at\_critical}$ exceeds its critical range with using the single update PWM, the instability will occur. But when this parameter is applied to the proposed method, the system is still in a stable state. So the range of $k_{at\_critical}$ by using the proposed method is obviously larger than the range of $k_{at\_critical}$ by using the single update PWM.

The dynamic simulation waveforms of grid currents using the single update PWM and proposed method are shown in Figure 16. And the dynamic simulation results of grid currents are shown in Table 4. In Figure 16(a), the grid inrush current is 50A and THD is 2.7% during the start-up process when the single update PWM is used. However, the grid inrush current can be decreased to 25A and THD can be reduced to 1.8% during the start-up process by using the proposed method, as shown in Figure 16(b).

5. Experimentation Verification

In order to verify the validity of simulation results, the experimental platform of three-phase grid-connected system is built shown in Figure 17, which includes the main circuit, the control board, and the LC filter circuit. DSP adopts TI's TMS320F2812 chip, and IGBT selects Infineon

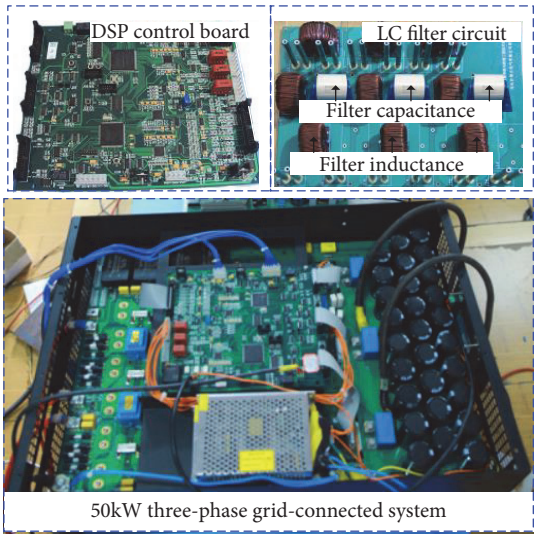
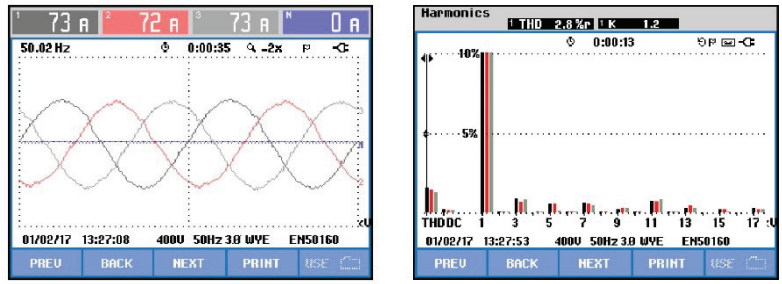


Figure 17: Experimental platform of three-phase grid-connected system.

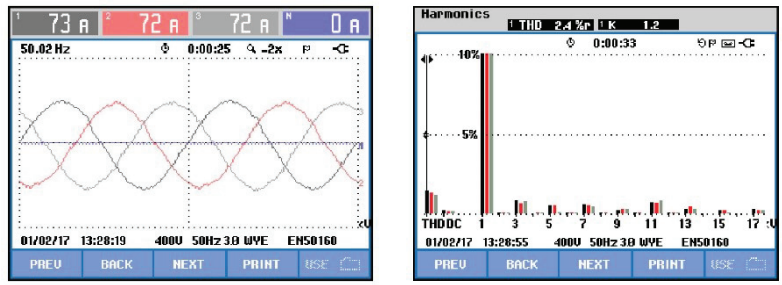
FF300R12ME4 module. The system parameters are shown as in Table 2.

By real-time debugging and setting breakpoints for the proposed method in CCStudio V3.3, the time spent on the sampling is 11.30μs, the time consumed by the outer voltage loop is 11.80μs, and the time required for the inner current loop is 7.60μs. The total time spent is 30.70μs. The selected switching frequency is up to 10kHz, and the switching period is 100.00μs. Therefore, the time consumed by the sampling



(a) (b)

Figure 18: The experimental waveforms and THD of grid currents using the single update PWM ($k_{at\_critical}$=0.5).



(a) (b)

Figure 19: The experimental waveforms and THD of grid currents using the proposed method ($k_{at\_critical}$=0.5).

Table 5: The steady state experimental results of grid currents.

Method	$k_{at\_critical}$	THD
Single update PWM	0.5	2.8%
Proposed method	0.5	2.4%
Proposed method	1	2.1%
Proposed method	1.5	2.2%

Table 6: The dynamic experimental results of grid currents.

Method	$k_{at\_critical}$	Adjustment time	Overshoot
Single update PWM	0.5	75ms	yes
Single update PWM	0.3	55ms	yes
Proposed method	1	15ms	no
Proposed method	0.5	35ms	no

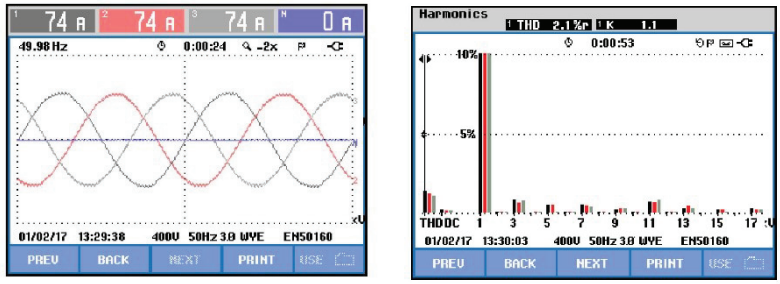
and calculation is only 30.70% of the switching period, which is less than 0.5 times the switching period. The sampling and calculation can be completed within 0.5 times the switching period.

The steady state experimental results of grid currents are shown in Table 5. And the experimental waveforms and THD of grid currents using the single update PWM and proposed method are shown in Figures 18 and 19, respectively. The theoretical root mean square (RMS) values of the grid currents are 50kW/(3×220V)≈75.76A. Considering some losses, the actual RMS values of grid currents are less than 75.76A. There is a measurement error among three current clamps of FLUKE, so three display values are not equal. Under the same $k_{at\_critical}$=0.5 and control parameters, THD of the grid current using the single update PWM is 2.8%, while THD of the grid current using the proposed method is only 2.4%.

The experimental waveforms and THD of grid currents using the proposed method with $k_{at\_critical}$=1, 1.5 are shown in Figures 20 and 21, respectively. In Figures 19, 20, and 21, THD of the grid current changes from 2.4% to 2.1%, and the next is from 2.1% to 2.2%, showing a tendency to increase firstly and then decrease with the inductance deviation coefficient $k_{at\_critical}$ increasing. Therefore, THD of the grid current is the lowest at $k_{at\_critical}$=1.

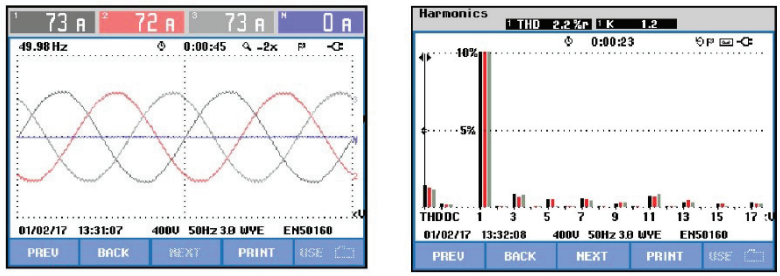
Steady state experimental waveforms of grid currents with the single update PWM and proposed method are depicted in Figure 22. In Figure 22(a), when $k_{at\_critical}$ changes from 0.5 to 2 with the single update PWM, the system becomes unstable. However, when $k_{at\_critical}$ changes from 0.5 to 2 with the proposed method, the system can still be in a stable state, as shown in Figure 22(b).

Dynamic experimental waveforms between the single update PWM and proposed method are compared as shown in Figure 23. Figures 23(a) and 23(b) correspond to $k_{at\_critical}$=0.5 and 0.3 in the single update PWM. Figures 23(c) and 23(d) correspond to $k_{at\_critical}$=1 and 0.5 in the proposed method. And the dynamic experimental results of grid currents are as shown in Table 6. The adjustment time is 75ms, 55ms, 15ms, and 35ms, respectively. When the above two individual methods are adopted with $k_{at\_critical}$=0.5, in



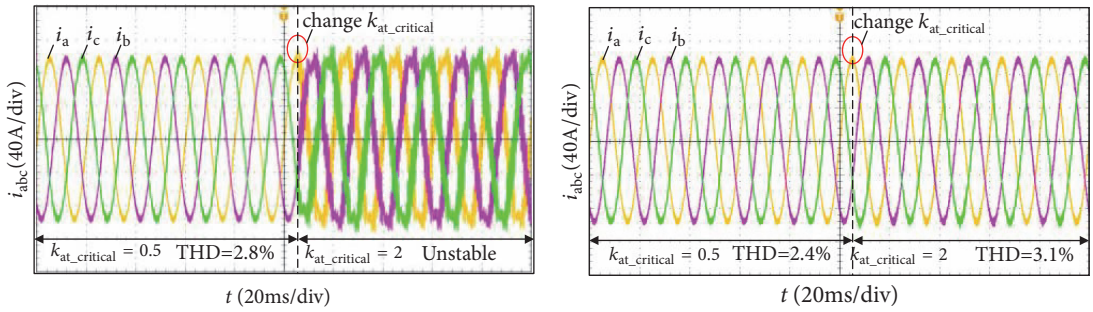
(a) (b)

Figure 20: The experimental waveforms and THD of grid currents using the proposed method ($k_{at\_critical}$=1).



(a) (b)

Figure 21: The experimental waveforms and THD of grid currents using the proposed method ($k_{at\_critical}$=1.5).



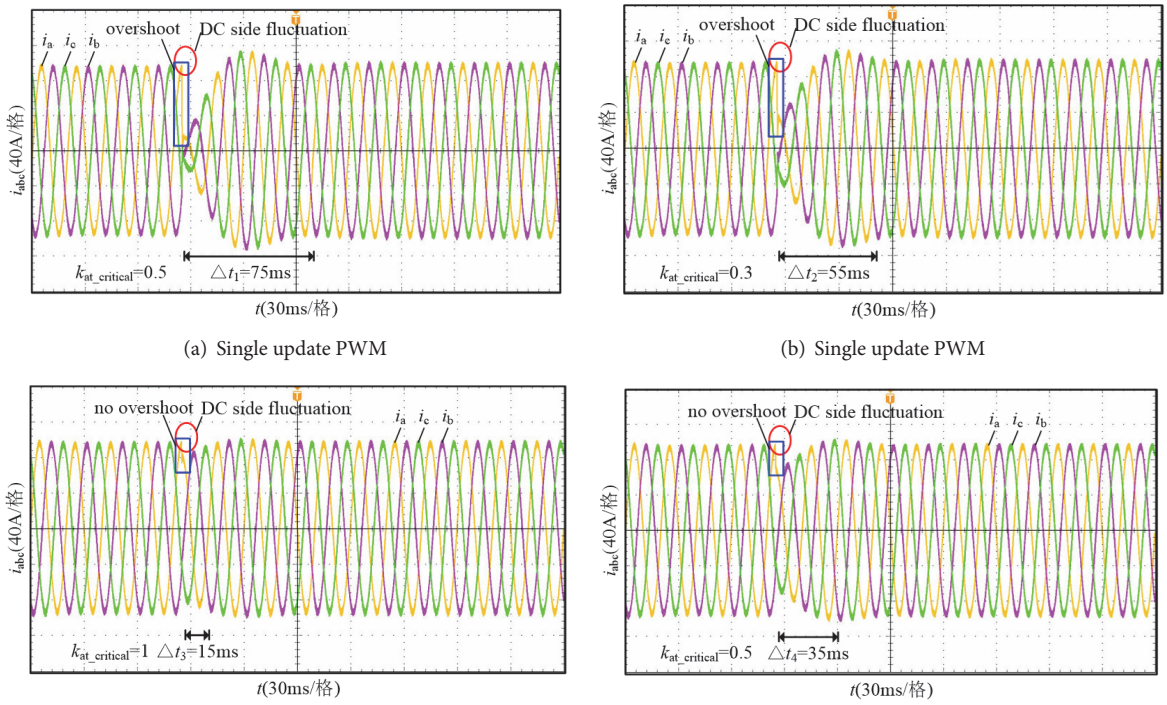
(a) Single update PWM (b) Double update PWM

Figure 22: Steady state experimental waveforms of grid currents with the single update PWM and proposed method.

Figure 23(a), the system has overshoot, and the adjustment time becomes longer, resulting in the poor dynamic. However, in Figure 23(d), the system has no overshoot and the dynamic becomes better with using the proposed method. Comparing Figure 23(c) with Figure 23(d), the adjustment time of the former is only 15ms, while the latter is 35ms. Thus, the system has faster response speed when the proposed method is used with $k_{at\_critical}$=1. Comparing Figure 23(a) with Figure 23(b), the system has the better dynamic with $k_{at\_critical}$=0.3 rather than $k_{at\_critical}$=0.5 when the single update PWM is used. From Figures 23(c) and 23(b), it can be obtained that the optimal dynamic of the system is superior by using the proposed method. The experimental results prove the correctness of theoretical analysis for Figure 11.

6. Conclusion

In this paper, the proposed double update PWM method for the deadbeat current controller not only effectively decreases the grid current distortion and control delay, but also improves the system stability and dynamic response speed due to reducing the characteristic root equation order of the closed-loop transfer function. The influence of the filter inductance deviation coefficient on the system performance is analyzed. As a conclusion, the corresponding filter inductance deviation coefficient in the system critical stability increases with increase in the parasitic resistance of the filter inductance and line equivalent resistance and decreases with increase in the sampling frequency.



(a) Single update PWM (b) Single update PWM

(c) Double update PWM (d) Double update PWM

Figure 23: Contrast analysis of dynamic experimental waveforms between the single update PWM and proposed method.

Data Availability

Some data are included within the article. No additional data are available.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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Research Article

Analysis of Transient Voltage Stability in a Low Voltage Distribution Network Using SST for the Integration of Distributed Generations

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Models of a low voltage distribution network using a typical tertiary-structure solid state transformer (SST) for the integration of distributed generations (DGs) and a conventional low voltage distribution network integrated with DGs were established to study the transient voltage stability issue, using the power system simulation software PSCAD. Effects on the transient voltage stability of the load bus and DC bus in the SST system are analyzed when grid-side cable line faults (such as short circuit and line disconnection) occur or the total output of DGs drops greatly. The results show that, comparing with the conventional system, the SST has apparent advantages on enhancing the transient voltage stability of load bus while facing different disturbances, even though SST has to regulate the voltage passively. Short circuit faults at different location of the grid-side line have different effects on the transient voltage stability, while the effect of disconnection fault is not related to fault location. Moreover, the DC bus voltage is easy to keep climbing continually when short circuit fault of the line occurs that is close to the SST input stage or disconnection fault occurs at any location of the line. If a battery energy storage station is installed, the transient voltage stability of DC bus and load bus will be improved effectively because of the regulation function of battery storage.

1. Introduction

With the technologies related to new energy generation being maturing day by day and the construction of the energy internet being pushed forward constantly [1–3], penetrations of distributed generations (DGs) in the distribution network are increasing gradually [4, 5]. Before the electric power grid and other energy networks connecting with each other and forming an energy internet, building a green smart grid with the core of energy routers to accept large-scale renewable energy sources widely is one way to construct the energy internet [6]. The intelligent dispatching and controlling center of the energy internet is the energy router [7], whose core is a high-frequency coupled device called solid state transformer (SST) based on the advanced power electronic technology [8].

The output of DG is random and the configuration of the distribution network integrated with DGs is complex, which can influence the stability of the distribution network [9, 10]. Reference [11] pointed out that the voltage stability issue does exist in distribution networks integrated with photovoltaic cell power, and the voltage instability phenomenon can be solved effectively by photovoltaic inverter reactive power support [2, 11]. A typical simulation model that a distributed photovoltaic power station is directly integrated into a low voltage distribution network was established in [12], and the effects were analyzed on the transient voltage stability of load bus when the faults such as short circuit and line disconnection occur or the output of distributed photovoltaic power plant drops greatly. In [13], the impacts of large-scale photovoltaic generation on the steady state voltage stability of distribution system were studied, and the conclusion that the photovoltaic modules have to operate in the reactive power support mode to improve the system voltage stability was obtained. In [14], a DC microgrid containing photovoltaic cell, wind turbine, and fuel cell was proposed and connected to the low voltage distribution network under variable load demands, and the simulation results showed that the voltage

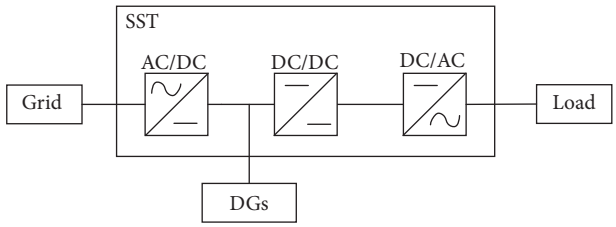


Figure 1: A typical tertiary-structure solid state transformer.

stability of DC bus can be maintained at different operating modes. In [15], a method that can enhance the transient voltage stability of a real distribution network with wind power was proposed, by means of optimal rating and location of the static synchronous compensator (STATCOM).

When using a SST for the integration of DGs and the distribution network, on the part of the grid, the ability of adopting the DGs will be enhanced and the situation of voltage oscillation and instability will be avoided. In this paper, a simulation model of a 0.38 kV low voltage distribution network which uses a typical SST for the integration of DGs was established using the power system simulation software PSCAD/EMTDC, and effects on the transient voltage stability of the system while facing various disturbances are studied. The advantages of the transient voltage stability using a SST for the integration of DGs are analyzed, and the differences between whether there is a battery energy storage station are discussed.

2. Modeling and Control Strategy of SST

As shown in Figure 1, a typical tertiary-structure SST is chosen for discussion, which consisted by a AC/DC unit, a DC/DC unit, and a DC/AC unit. The three units are input stage, isolation stage, and output stage, respectively. To realize the bidirectional power flow, the full-controlled device, IGBT, is used for building the SST [16].

In this paper, a voltage-source PMW rectifier is chosen as the input stage of SST, which can rectify the 0.38 kV AC of the low voltage distribution network to 0.78 kV DC.

The dual-loop decoupled control strategy is chosen for the input stage [17]. The voltage orientation control strategy based on d-q rotating coordinate system is selected for the voltage loop, and the direct current control is adopted for the current loop. The grid-side power factor can be corrected according to the control goal. The control equations of the SST input stage are

$$\begin{aligned} i_{1d}^{*} &= \left(K_{\mathrm{P1}} + \frac{K_{\mathrm{I1}}}{s}\right)\left(U_{\mathrm{dc}}' - U_{\mathrm{dc}}\right) \\ i_{1q}^{*} &= 0 \\ u_{1d}^{*} &= u_{1d} + \omega L i_{1q} - \left(K_{\mathrm{P2}} + \frac{K_{\mathrm{I2}}}{s}\right)\left(i_{1d}^{*} - i_{1d}\right) \\ u_{1q}^{*} &= u_{1q} - \omega L i_{1d} - \left(K_{\mathrm{P2}} + \frac{K_{\mathrm{I2}}}{s}\right)\left(i_{1q}^{*} - i_{1q}\right), \end{aligned} \tag{1}$$

where i_{1d}^{*} and i_{1q}^{*} are the grid-side current command values in d-q coordinate system and i_{1d} and i_{1q} are the actual values; u_{1d}^{*} and u_{1q}^{*} are the grid-side voltage command values in d-q coordinate system and u_{1d} and u_{1q} are the actual values; U_{dc}', U_{dc} are the reference voltage and actual voltage of DC bus, respectively; K_{P1}, K_{I1}, K_{P2}, and K_{I2} are the parameters of PI controllers; L is the filter inductance of SST input stage.

In isolation stage, the 0.78 kV DC is converted to a high-frequency AC square wave and coupled to the secondary side of a high-frequency isolated transformer which is used to isolate the original side and subside. Then, the high-frequency AC will be rectified to 0.78 kV DC.

In the output stage, the 0.78 kV DC is inverted to 0.38 kV AC for power supplies. The dual-loop decupled control strategy with the voltage and current feedforward is adopted for the control [18]. The control equations of the SST output stage are

$$\begin{aligned} i_{2d}^{*} &= i_{2d} - \omega C_f u_{2q} + \left(K_{\mathrm{P3}} + \frac{K_{\mathrm{I3}}}{s}\right)\left(u_{2d}' - u_{2d}\right) \\ i_{2q}^{*} &= i_{2q} + \omega C_f u_{2d} + \left(K_{\mathrm{P3}} + \frac{K_{\mathrm{I3}}}{s}\right)\left(u_{2q}' - u_{2q}\right) \\ u_{2d}^{*} &= u_{2d} - \omega L_f i_{2q} + \left(K_{\mathrm{P4}} + \frac{K_{\mathrm{I4}}}{s}\right)\left(i_{2d}^{*} - i_{2d}\right) \\ u_{2q}^{*} &= u_{2q} + \omega L_f i_{2d} + \left(K_{\mathrm{P4}} + \frac{K_{\mathrm{I4}}}{s}\right)\left(i_{2q}^{*} - i_{2q}\right), \end{aligned} \tag{2}$$

where i_{2d}^{*} and i_{2q}^{*} are the load current command values in d-q coordinate system and i_{2d} and i_{2q} are the actual values; u_{2d}^{*} and u_{2q}^{*} are the load bus voltage command values in d-q coordinate system, u_{2d}' and u_{2q}' are the reference values, and u_{2d} and u_{2q} are the actual values; K_{P3}, K_{I3}, K_{P4}, and K_{I4} are the parameters of PI controllers; L_f, C_f are the filter inductance and capacitance of SST output stage, respectively.

3. Model of Low Voltage Distribution Network Integrated with DGs

A conventional system model of a low voltage distribution network integrated with DGs (including distributed photovoltaic and wind power) is established using the power system simulation software PSCAD, as shown in Figure 2. $\dot{U}_1$ and $\dot{U}_2$ are the voltage of Bus 1 and Bus 2, respectively. The impedance of the cable is $R + jX$ and the value is $0.096 + j0.015\ \Omega$. The power from the low voltage distribution network is noted as $P_1 + jQ_1$, the power flow from the network to Bus 2 is noted as $P_2 + jQ_2$. The outputs of photovoltaic power plant and wind power farm are $P_{\mathrm{pv}} + jQ_{\mathrm{pv}}$ and $P_{\mathrm{wind}} + jQ_{\mathrm{wind}}$, respectively; the absorbed power of the three-phase induction motor and the static load are $P_M + jQ_M$ and $P_s + jQ_s$, respectively.

Some ancillary facilities such as reactive power compensation devices and inverters of photovoltaic or wind power systems can be left out because of the structure and flexible control characteristics of SST, and the DGs can be directly connected to the DC bus. The model of a low voltage distribution network using a SST for the integration of DGs is shown in Figure 3.

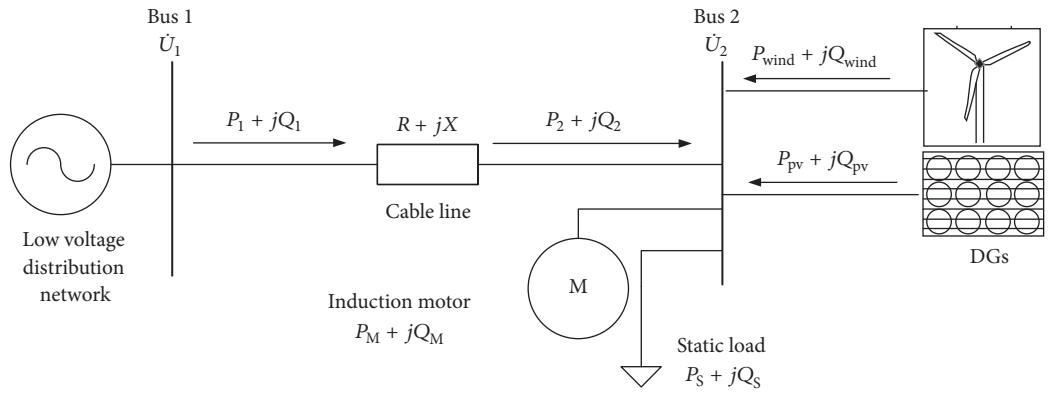


Figure 2: Model of conventional low voltage distribution network integrated with DGs.

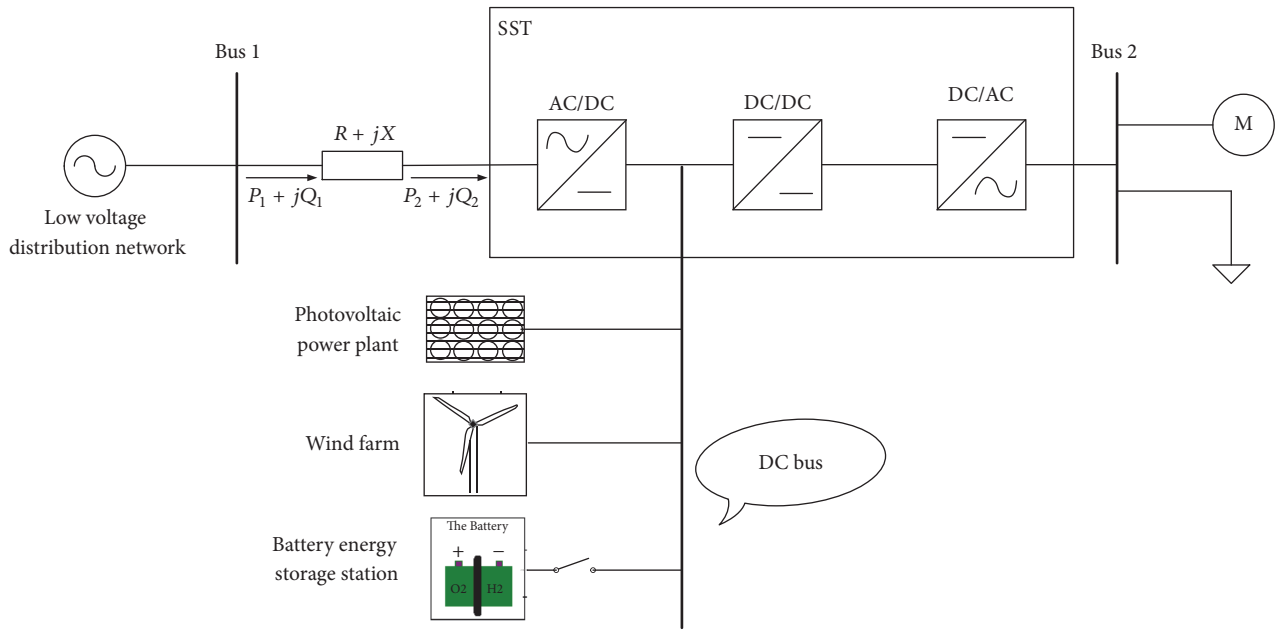


Figure 3: Model of low voltage distribution network integrated with DGs using SST.

In Figures 2 and 3, the rated capacities of the photovoltaic power station and the wind power plant both are 260 kW. The loads are composed of two parts of static load (including a constant resistance load and a constant impedance load) and a three-phase induction motor. The rated power of the constant resistance R_{s1} is 90 kW; the rated power of the constant impedance $R_{s2} + jX_{s2}$ is 60 kVA; the rated capacity of the three-phase induction motor is 49.5 kVA.

During the simulation analyses, the environmental temperature is 298.15 K, the light intensity is 1000 W/m^2, the wind speed is 11 m/s, and these values will vary in a certain rage. When the system operates normally, the absorbed active and reactive power of the induction motor are about 46 kW and 23 kvar, respectively; the absorbed active and reactive power of the constant impedance load are about 48 kW and 35 kvar, respectively. The grid-side unity power factor is realized due to the control strategy of the SST input stage.

4. Effects on Transient Voltage Stability of Grid-Side Line Faults

The research results show that short circuit fault of grid-side cable line at different location has different effect on the system transient voltage stability because of the control function of the SST input stage, while line disconnection fault is not associated with the fault location.

The schematic diagram of fault position is shown in Figure 4. The grid-side cable line is divided into Line 1 and Line 2 equivalently, by the signal collection device which monitors the distribution network. Line 1 contains only a small part of lines connecting the signal collection device and the SST input stage in practice, and its fault possibility is much lower. Line 2 contains the whole external distribution network lines which are so complex that their fault possibility is very high.

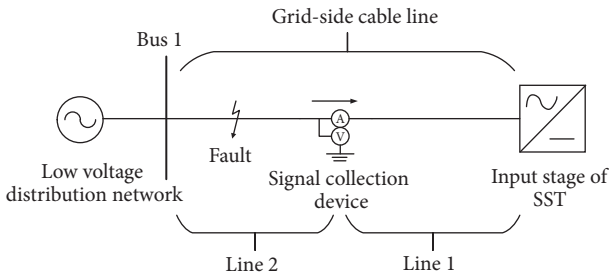


Figure 4: Schematic diagram of line fault location.

To save space and take the aesthetics into consideration, most urban low voltage distribution networks use cable lines. Insulation aging or damage is the main cause of cable faults.

4.1. Short Circuit Fault Occurs at Line 1. Line 1 may have short circuit faults though there are fewer lines in it. Once the fault occurs, each stage of the SST has to regulate the voltage passively. Therefore, we focus on the influence on the system transient voltage stability when different short circuit faults occur at Line 1.

Take the typical single-phase grounding short circuit fault as an example. Now set the simulation time as 2 s. After time $t = 0.4$ s, the system enters stable operation. When $t = 0.6$ s, single-phase grounding short circuit fault occurs at the midpoint of Line 1, and the fault duration is 0.1 s. The relay protection acts and removes the fault line when $t = 0.65$ s. We focus on the system transient voltage stability when the cut line is no longer reinput because 0.38 kV low voltage cable line has generally no reclosing device.

After the line is cut off, the grid loses power and the DGs enter the state of isolation island operation. We do this research on the condition that the outputs of DGs are rich and can meet the need of local loads. When the single-phase grounding short circuit fault occurs, the response curves of load bus voltage and absorbed powers of induction motor in the conventional DGs grid-connected system (shown in Figure 2), the response curves of load bus (Bus 2) voltage, absorbed powers of induction motor, and DC bus voltage are shown in Figure 5.

In general, if a 0.38 kV AC bus voltage in low voltage distribution network is lower than 0.9 pu or higher than 1.1 pu after a large disturbance for more than the specified limit time (e.g., 1 s or above), it can be considered that the low voltage AC bus is transient voltage instability [12]. In this paper, the transient voltage stability of low voltage DC bus obeys the same rules, too.

As can be seen from Figures 5(a) and 5(b), for the conventional system, after the single-phase grounding short circuit fault occurs and the relay protection acts, the load bus voltage drops rapidly to 0.8 pu or less, and the load bus is considered to be unstable, thus causing the active and reactive power absorbed by induction motor to have oscillations and finally to be below rated values (rated active power is 1 pu and rated reactive power is 0.5 pu). The limitation of the conventional system is that the inverter control function of DGs is simple, and the transient voltage stability of load bus cannot be guaranteed while facing disturbances.

In this paper, the DGs' inverters adopt outlet voltage control strategy; simulation results show that the transient voltage stability of load bus cannot be maintained by the inverters without the support of power grid.

If the inverters adopt constant power control strategy, the outputs of DGs will remain constant under the normal environment after the disturbances. After the relay protection acts, the load bus has the equation according to the power balance:

$$P_{\text{pv}} + P_{\text{wind}} = P_M + P_S = P_M + \left(\frac{1}{R_{s1}} + \frac{R_{s2}}{R_{s2}^2 + X_{s2}^2}\right) U_2^2 \quad (3)$$

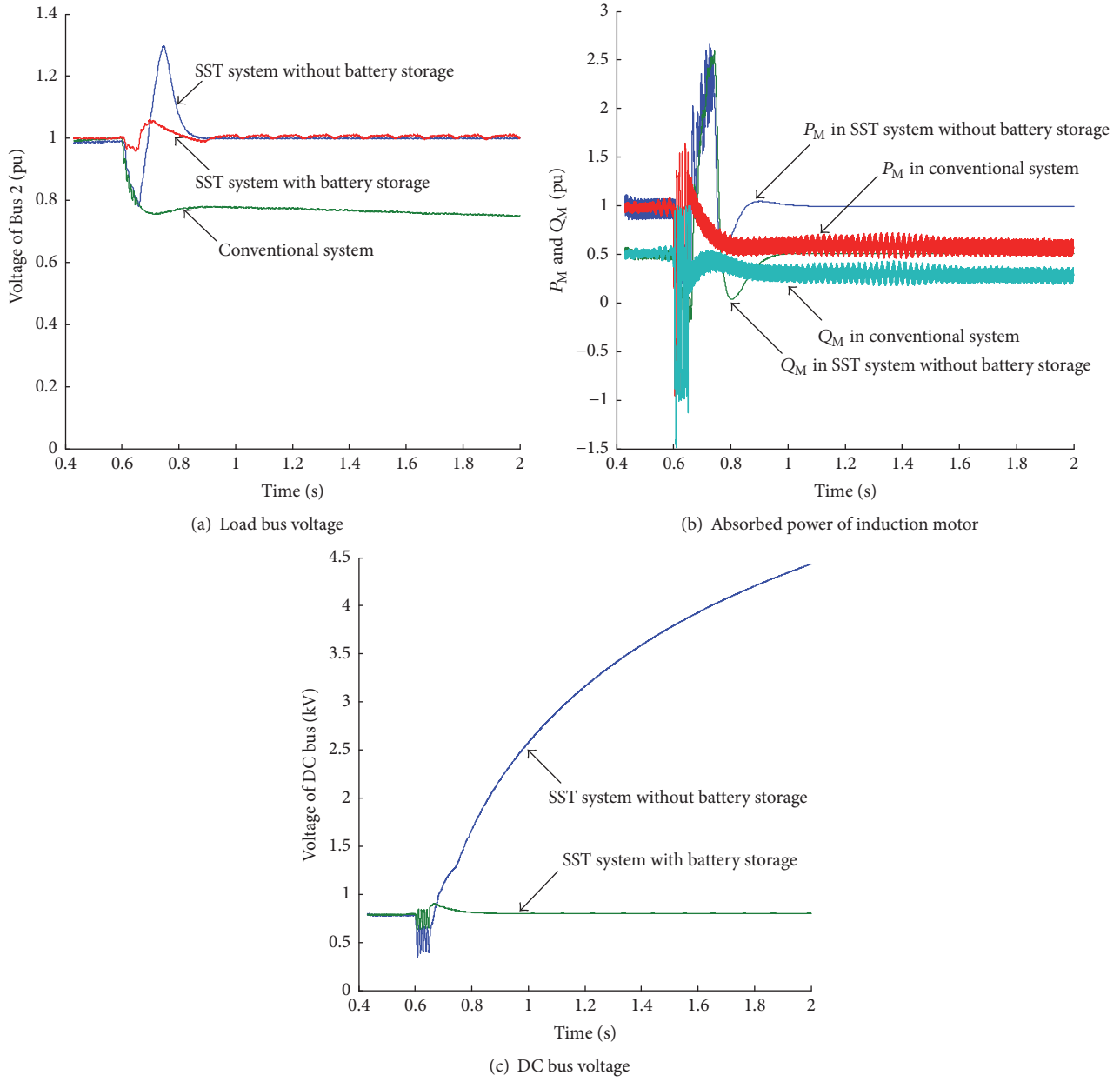
It can be seen from Formula (3), in the case of rich outputs of DGs, the load demand can be met, so the load bus voltage recovers quickly. Accordingly, the absorbed active power of induction motor begins to fall down after the oscillation. From Formula (3), we can find that U_2 will be lifted once P_M starts to decrease, eventually causing the load bus voltage to climb continually. And at this time, the load bus is still considered to be transient voltage instability. It is necessary to abandon the photovoltaic and wind power to protect the motor in time.

The effectiveness of the control strategy of SST on the transient voltage stability can be seen from Figures 5(a) and 5(b), which reflects the SST's better ability of maintaining transient voltage stability while facing disturbances. Though the fault is close to the SST input stage, active control cannot be taken by the SST to stabilize the grid-side surge current and the current has to be regulated passively and the load bus voltage can recover to the original rated value and maintain the stability after experiencing rapid sag. Therefore, the absorbed powers of induction motor can recover to the original rated values too.

As shown in Figure 5(c), although the SST can maintain the voltage stability of load bus by passive regulation, if there is no a battery energy storage station installed in the DC bus, the DC bus voltage will keep climbing because the outputs of DGs cannot be transmitted to the grid. At this time, we can consider that the DC bus loses its transient voltage stability. It is harmful to the security and stability of the system and the photovoltaic and wind power will have to be abandoned.

The battery energy storage station plays an important role in stabilizing the load bus voltage and DC bus voltage. As shown in Figure 5, in the DGs grid-connected system based on SST, the battery energy storage station can stabilize the load bus voltage and DC bus voltage greatly after the shot circuit fault occurs, and there is merely a slight oscillation. After the relay protection acts, the DC bus voltage is regulated to the original rated value because of the function of energy storage station, avoiding the voltage climbing phenomenon.

Simulation results show there are similar conclusions when other short circuit faults occur at Line 1; for instance, the response curves of three-phase short circuit occurring at midpoint of Line 1 are shown in Figure 6.



(a) Load bus voltage

(b) Absorbed power of induction motor

(c) DC bus voltage

FIGURE 5: Response curves when single-phase grounding short circuit fault occurs at the midpoint of Line 1.

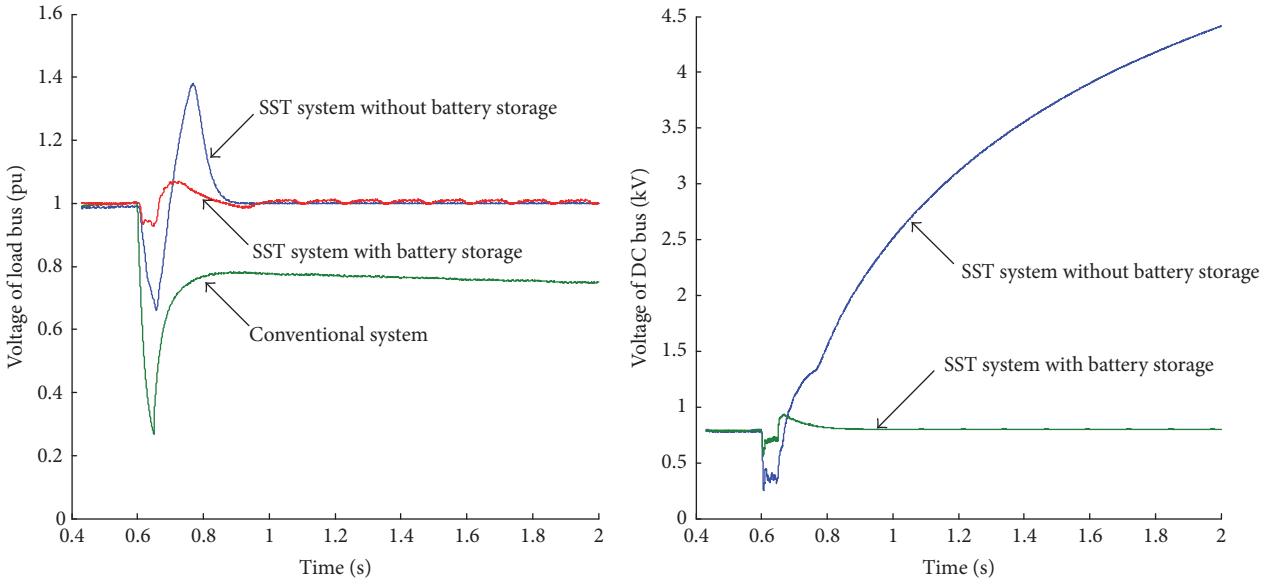
4.2. Short Circuit Fault Occurs at Line 2. If short circuit fault occurs at Line 2, the information can be picked up and the surge current can be steadied by the active control of the SST input stage, and it merely has little effect on the load bus voltage and DC bus voltage even if the most serious three-phase short circuit fault occurs, as shown in Figure 7.

4.3. Disconnection Fault Occurs at Any Location of Gird-Side Line. When the line disconnection fault occurs at any location of the gird-side line (including Line 1 and Line 2), we can draw similar conclusions with the condition that short circuit faults occurs at Line 1. Taking the disconnection occurring at the midpoint of Line 1, for example, the response curves are shown in Figure 8.

5. Impact of Great Drop of DGs' Total Output on Transient Voltage Stability

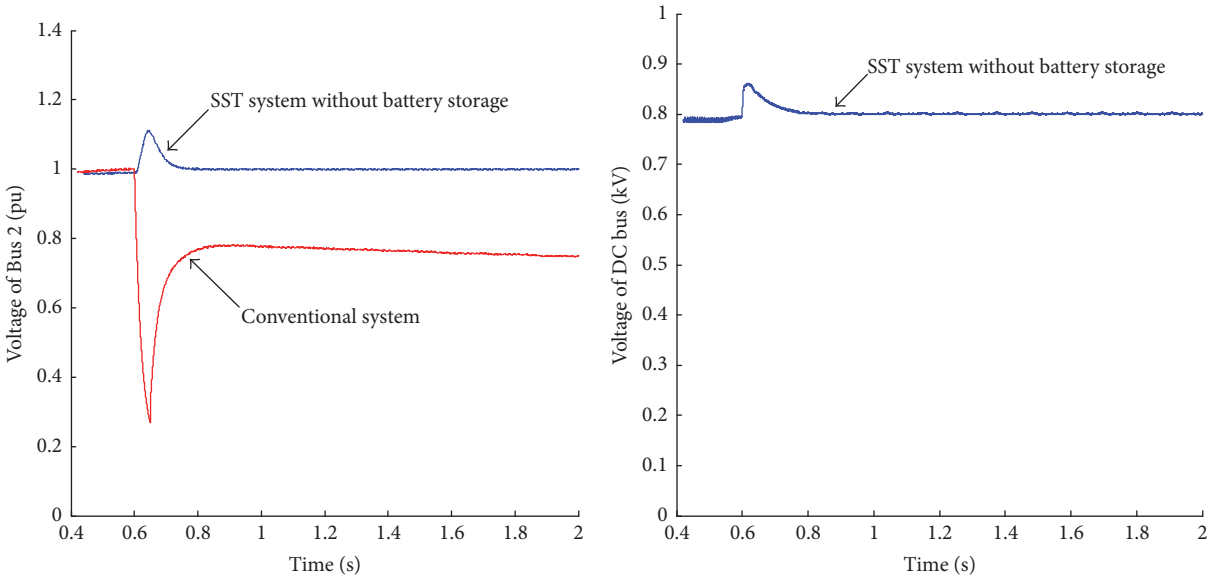
The output of DG is affected by the weather greatly. The sudden changes in light intensity and wind speed will cause sudden changes in the outputs of photovoltaic power plant and wind farm, respectively, which will affect the transient voltage stability of the system.

Considering the most adverse weather condition, when the light intensity drops greatly and the wind turbine drops out because wind speed is too large, the sudden great drop of DGs' total output can cause the load bus voltage to be instability. For the conventional system shown in Figure 2, supposing that the total load power is $P_L + jQ_L$ and the total



(a) Load bus voltage (b) DC bus voltage

Figure 6: Response curves when three-phase short circuit fault occurs at the midpoint of Line 1.



(a) Load bus voltage (b) DC bus voltage

Figure 7: Response curves when three-phase short circuit fault occurs at the midpoint of Line 2.

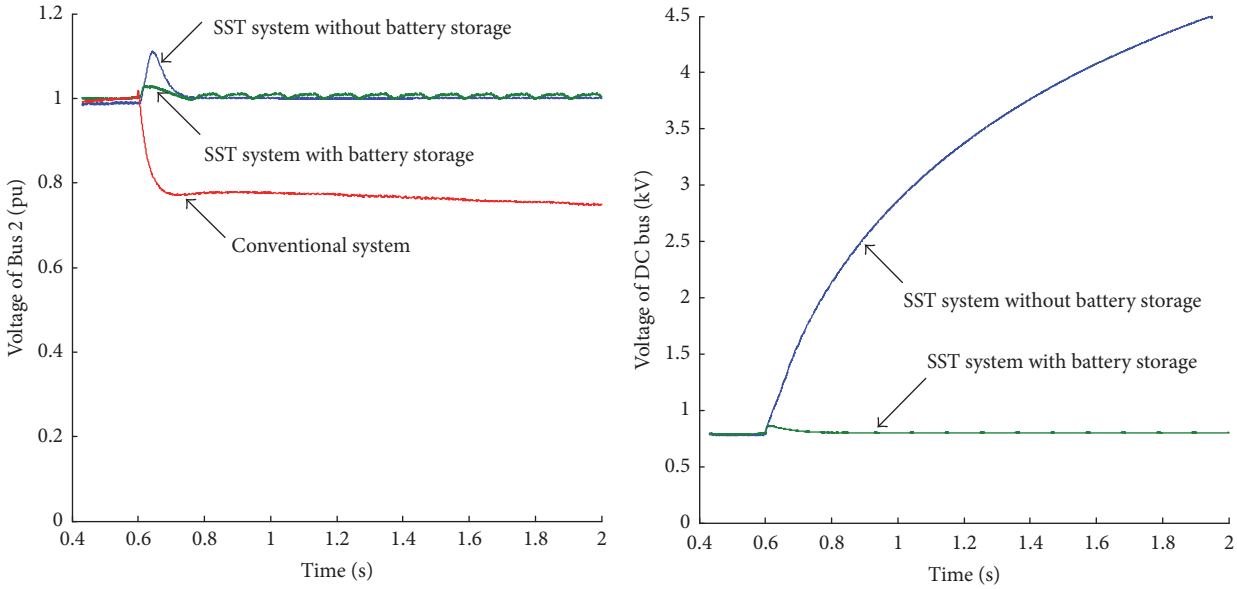
output of DGs is $P_\Sigma + jQ_\Sigma$, the load bus voltage drops to U_2' when the DGs' total output drops to 0 suddenly; there will be [12]

$$U_2 - U_2' = \frac{P_\Sigma R + Q_\Sigma X}{U_2} + \left(P_L R + Q_L X\right)\left(\frac{1}{U_2'} - \frac{1}{U_2}\right) \quad (4)$$

Since both photovoltaic and wind power have maximum power control, Q_Σ is almost 0. Suppose the voltage drop ratio is a; that is, $U_2' = aU_2$. Put $Q_\Sigma = 0$ and $U_2' = aU_2$ into Formula (4), we can get the following:

$$P_\Sigma = \frac{(1-a)U_2^2 - (1/a - 1)\left(P_L R + Q_L X\right)}{R} \quad (5)$$

In Formula (5), if U_2 is the rated value (1 pu), then a takes 0.9. And we can get the upper limit approximate value of total output active power of DGs that is just right for maintaining the system transient voltage stability when the total output



(a) Load bus voltage

(b) DC bus voltage

Figure 8: Response curves when disconnection fault occurs at the midpoint of Line 1.

drops to 0. When the DGs' total output is equal or greater than the upper limited approximate value in the actual operation of the system and drops to 0 suddenly, the load bus will lose its transient voltage stability in general.

Using the parameters in the conventional system to calculate according to Formula (5), it will figure out that the upper limit approximate value of DGs' total output is 150 kW as a takes 0.9 (because U_2 is very close to 1 pu). Now, the total output of DGs in the conventional system and the SST system is set to be 150 kW, respectively. The simulation time is set to be 2 s, and the photovoltaic and wind power suddenly drop to 0 at $t = 0.6$ s. The response curves are shown in Figure 9.

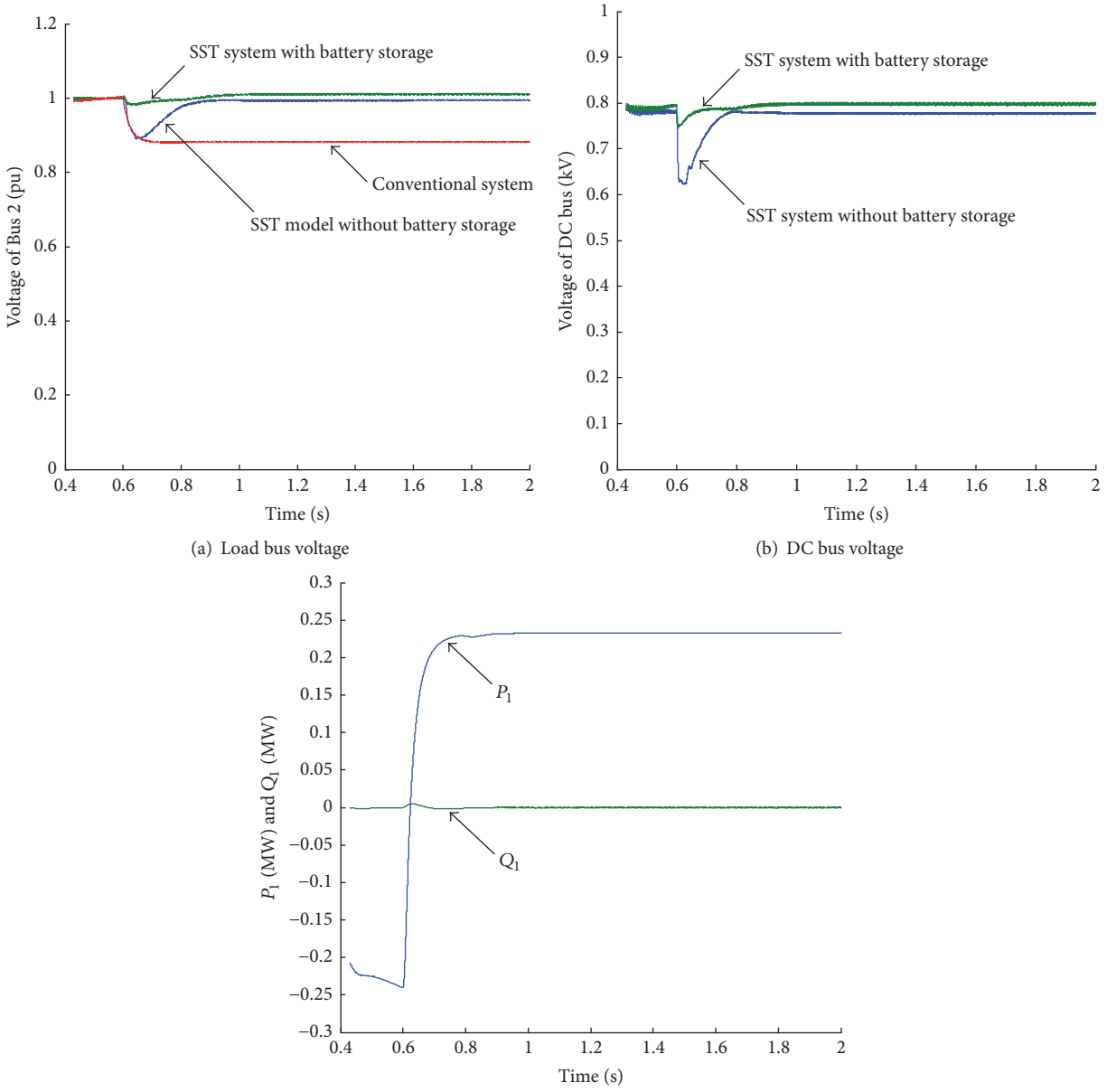
It can be known from Figures 9(a) and 9(b) that the load bus voltage in the conventional system is unstable after the great drop of DGs' total output occurs, and the voltage drops to about 0.88 pu which is almost matching with the theoretical value (0.9 pu), while in the SST system, the load bus and DC bus recover transient voltage stability quickly. When it comes to the SST system with a battery energy storage station, the voltages of load bus and DC bus are almost not affected by the disturbance. As can be seen from Figure 9(c), for the SST system without a battery energy storage station, before the great drop of DGs' total output occurs, the reactive power transmitted from the grid is 0 because of the control of the SST input stage, while the active power is −0.2 MW because of the plenty outputs of DGs. After the total output of DGs drops to 0, the low voltage distribution network supplies a certain amount of powers to help to maintain the bus voltage at this moment.

6. Conclusions

The development of the technology of DGs has realized the effective integration and efficient utilization of renewable energies distributed around the world. It has practical significance to study on the transient voltage stability of the DGs grid-connected system and it is meaningful for realizing the change from a traditional fossil-fuel grid to a future green smart grid. In this paper, we use PSCAD software to study the transient voltage stability of the low voltage distributed network integrated with DGs based on SST under the condition of cable line fault and sudden drop of DGs' total output and concluded as follows:

(1) Using a SST for the integration of DGs and the distribution network has advantages on the system transient voltage stability while facing different faults. The influence of grid-side line short circuit fault on the transient voltage stability is related to fault location, and the line disconnection fault is not the case. Even if SST has to regulate the voltage passively when the fault occurs at the line close to the SST input stage, the regulation function of SST still can maintain the voltage transient stability of load bus. This avoids load bus in the conventional DGs gird-connected system losing its transient voltage stability effectively while facing such faults and improves utilization of DGs and reliability of power supply.

(2) Although the SST control makes the load bus have better transient voltage stability, the DC bus voltage is easy to keep climbing continually when the short circuit occurs at the line side that is close to the SST input stage or the line disconnection occurs at any location of the line. At this moment, the DC bus can be considered to be transient voltage instability, and this is a new transient voltage stability phenomenon in the DGs gird-connected system using SST. It is harmful to the security and stability of the system



(a) Load bus voltage

(b) DC bus voltage

(c) Power supplies of distribution network without battery storage

Figure 9: Response curves when total output of DGs drops to 0.

operation. The DC bus voltage can be stabilized by the DGs equipped with a certain amount of batteries or a battery energy storage station installed in the DC bus when faults occur, which can effectively avoid the transient voltage instability of DC bus and guarantee the system safety.

(3) When the total output of DGs drops greatly under the adverse weather condition, the SST can ensure the transient voltage stability thus avoiding the biggest voltage drop of load bus in the conventional system. If a battery energy storage station is installed, the load bus voltage and DC bus voltage will be almost unaffected while facing the great drop of the DGs' total output. It is of great significance to the stable operation of low voltage distribution network that the battery storage is installed.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

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Research Article

A Novel Hybrid T-Type Three-Level Inverter Based on SVPWM for PV Application

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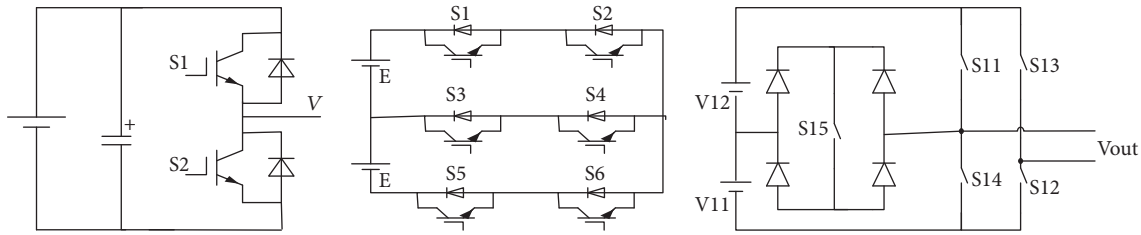
We describe several, recently reported, new topologies and compare them with each other, in order to find out the optimal multilevel grid-connected inverter topology. Then, we classify these topologies according to the basic unit which predecessors proposed. Eventually, we propose the hybrid T-type inverter topology structure, which is composed of two best basic units. This structure takes full advantage of the two components, to reduce the harmonic content and the power loss of the converter and improve the conversion efficiency of the system. At the same time, the space vector pulse width modulation (SVPWM) method is used to simulate the proposed topology in the MATLAB/SIMULINK platform, while the loss of each semiconductor switch is calculated using MELCOSIM software. The results show that the proposed structure is superior to the most widely used topology, i.e., the diode clamped and the T-type three-level circuits.

1. Introduction

Nowadays, the contradictions between the consumption pattern of the traditional petrochemical energy and the economic development and environmental protection are becoming more and more prominent. People gradually realize the importance of taking sustainable development road, vigorous developing, and utilizing of the renewable energies. Among the renewable energies, the solar energy represents the largest and the most commonly distributed resource. The photovoltaic power generation technology using the solar cells effectively absorbs the solar energy and changes it into electricity. The grid-connected inverter is the key component and important equipment in a photovoltaic grid-connected system.

In the design of general inverters, synthetically considering the cost-effective factors, insulated-gate bipolar transistor (IGBT) represents the most employed device. However, due to the nonlinearity of the IGBT's conduction voltage drop, it does not significantly increase with the increase of current, thus ensuring that the inverter still presents a relatively low loss and high efficiency at the maximum load condition. However, since the European efficiency is mainly related to the efficiency of the inverter at different light-load, the aforementioned characteristics of the IGBT represent the disadvantage of the photovoltaic grid-connected inverter. For light loads, the turn-on voltage drop of the IGBT does not significantly reduce, which in turn reduces the European efficiency of the inverter. In contrast, due to linear conduction voltage drop of the MOSFET, it provides lower turn-on voltage drop for light loads. Considering the excellent dynamic characteristics and high frequency work ability, MOSFET becomes the first choice for photovoltaic inverting [1].

Three-level inverter has been widely used in the middle and high voltage large capacity AC speed regulating fields, since its output has higher power quality, lower harmonic contents, better electromagnetic compatibility, lower switching losses, and other advantages. However, it still suffers from some key problems, including the simplification of the three-level algorithm, neutral point voltage control in the overmodulation region, and the stability of the system at high voltage. In view of the above problems, this paper studies



(a) Basic unit A (b) Basic unit B (c) Basic unit C

Figure 1: Basic unit of the inverter.

the structure and principle of the three-level inverter, the control of the neutral point voltage of the capacitor, and the realization of the SVPWM algorithm.

In this paper, we study novel T-type inverter topology in PV system using SVPWM control algorithm. The structure is organized as follows: Section 2.1 introduces basic cells of the new multilevel PV inverters and classifies them. Section 2.2 presents and compares new types of multilevel inverters. Section 2.3 analyzes and compares switch losses and conversion efficiency of diode clamped T-type and proposed hybrid T-type. Section 2.4 details SVPWM control algorithm. Section 3 gives simulation results. Finally, Section 4 concludes the paper.

2. Materials and Methods

2.1. Basic Unit. Inverter basic unit refers to the minimum component that meets the demands of the topological multilevel grid-connected inverter. Odeh [2] proposed one basic concept of the basic unit of multilevel grid-connected inverter.

As shown in Figure 1(a), after achieving the basic unit, it may be extended in form of series-parallel and parallel-series connections to present higher voltage levels. Odeh [3] analyzes the connection between the topologies of the multilevel grid-connected inverters and proposes a regular pattern that is followed when general multilevel grid-connected inverter topology simplifies to other multilevel grid-connected inverter topology. For example, the main switches must be all maintained, all switching devices must be deleted symmetrically, diodes and capacitors must be distributed symmetrically, and so on. With the development of power electronic devices, in order to unify the pressure drop of the power electronic switch transistors, a more practical basic unit is put forward.

Figure 1(b) shows the stacked commutation cells or three-pole cells. As the employed conduction strategy, one of the two transistors in the outer leg is in a frequent switching state only during half-cycle, while the other transistor is switched only once during the fundamental wave period, which greatly reduces the switching loss. This conduction strategy also avoids the voltage-equalization problem caused by the simultaneous turn-on and turn-off of the series devices. Figure 1(c) shows the structure of a multilevel inverter basic unit reported by Draxe et al. [4]. This inverter is formed using five switches with antiparallel diodes, where S11 to S14 are arranged as the traditional CHB inverter, while, however, S15 is added to increase the output voltage levels by selecting the appropriate voltage source. This structure produces higher voltage levels with minimum number of switches by optimizing the circuit layout and reducing the gate drive circuitry.

Recently reported inverter topologies aim to reduce the number of the power electronic devices to improve the conversion efficiency. Figure 2 shows the classification of the inverters based on their topologies. As we see from this figure, the largest portion of the proposed inverter topologies formed by the basic unit A, due to its relatively simple construction. The topologies composed of basic units B and C have not yet appeared because of their complex basic constitution unit.

The basic unit of the inverter consists of a DC power supply and a pair of switches. By using the same basic unit, taking Figure 1(a), for example, in the form of series-parallel combinations a new circuit topology, as shown in Figure 3, called single phase H-bridge topology, is obtained. Or by series-parallel combinations between different basic units also a new one is got. For instance, three parallel basic units A and one basic unit B constitute the three-level T-type inverter topology, as shown in Figure 4. Different multilevel inverters can be obtained by multiseries and multiparallel connections of multiple basic units. And the construction of the other topologies in Figure 2 can be deduced by the same analogy.

2.2. New Type Inverter Topology. The work in [5] proposed the split capacitor H-bridge (SC-HB) inverter topology. Adding a simple DC-DC converter, this topology overcomes the capacitance-voltage balance problem, while reducing the leakage current, with improved efficiency. The work in [2] presented the improved cascaded H-bridge topology which consists of a half-bridge level latching circuit and a main inverter H-bridge. Thus, it reduces the number of the devices, switching loss, and harmonic content. An asymmetric cascaded H-bridge topology, with different, and proportional, DC voltage source values is reported in [4]. This reduces the capacity and number of the devices, as well as the costs. A sine-wave pulse width modulation (SPWM) three-phase multilevel inverter topology may be achieved by inserting two auxiliary switches in each phase bridge to change the basic two-level to three-level inverter to synthesize higher levels [3]. In comparison with traditional diode clamps, flying

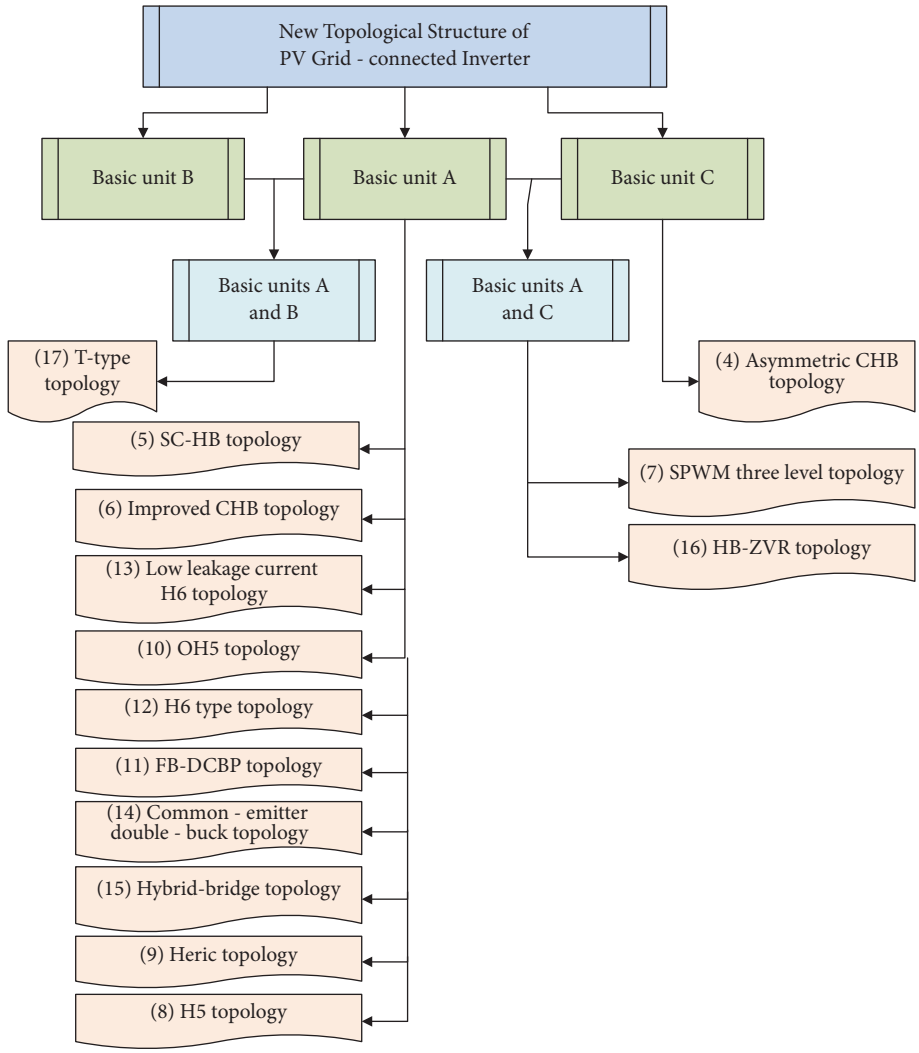
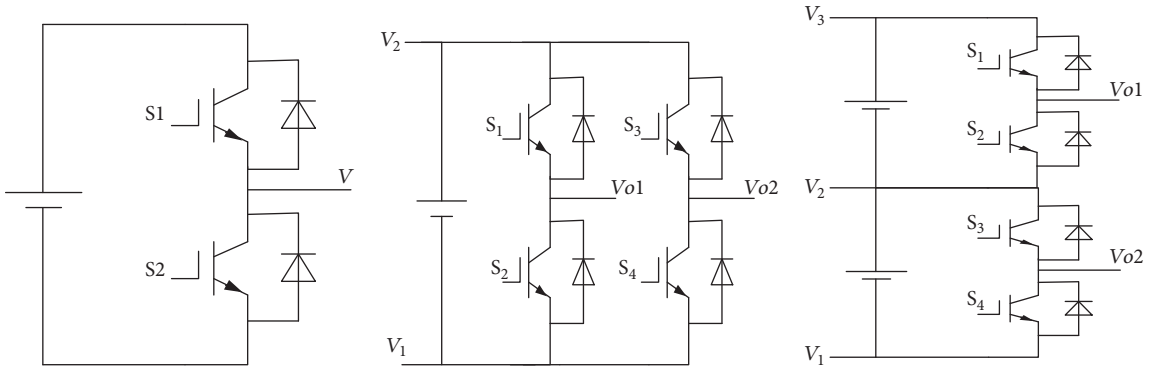


Figure 2: Per-phase circuit configuration of the conventional multilevel inverter.



(a) Basic unit A (b) Parallel-connection (c) Series-connection

Figure 3: Parallel-series-connection topology of the same basic units.

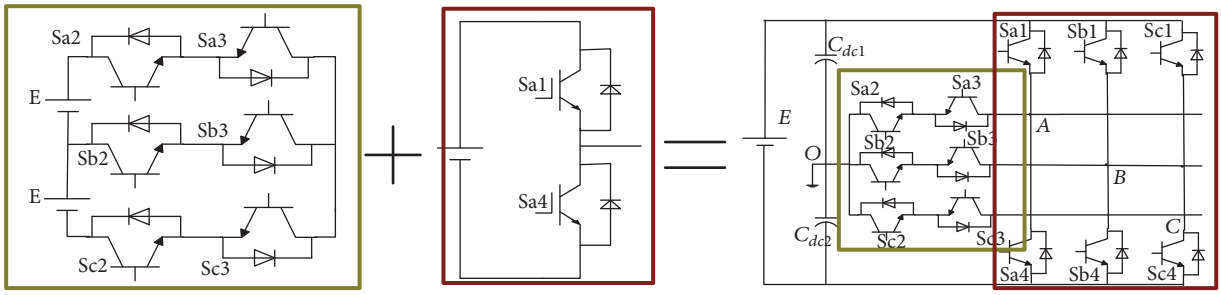


Figure 4: Parallel-series-connection topology of the different basic units.

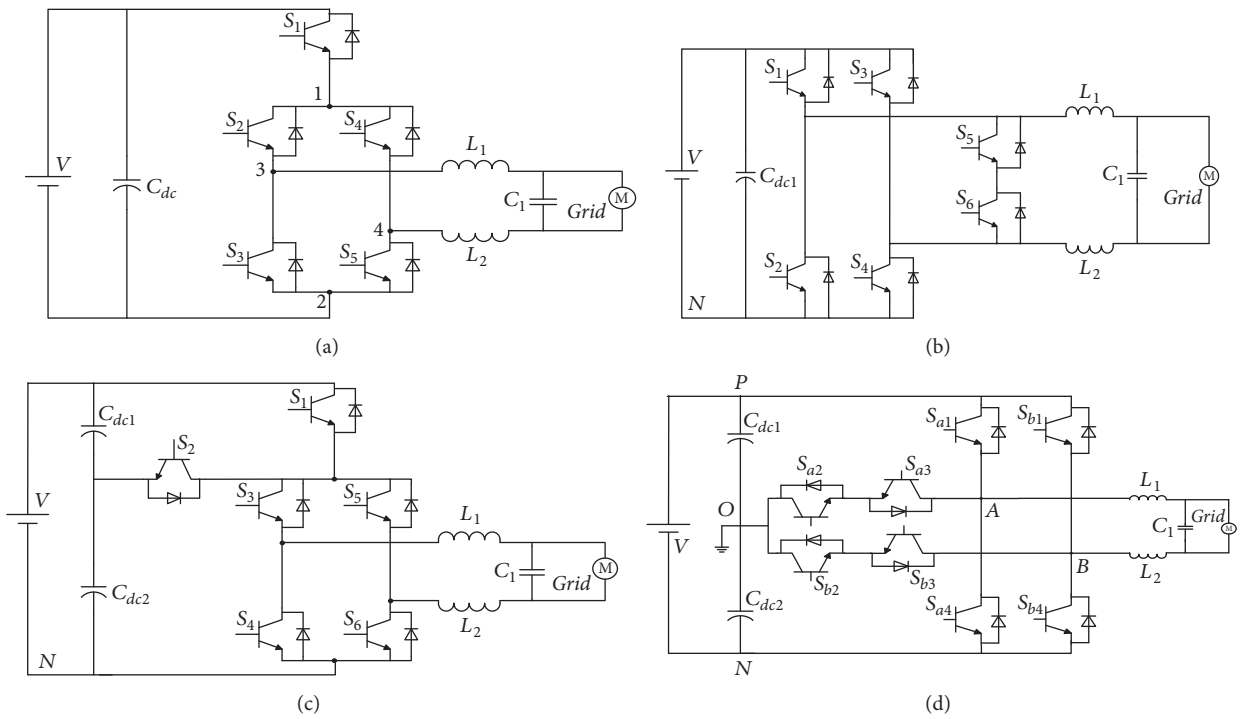


Figure 5: Some new topology structure. (a) H5 topology, (b) Heric topology, (c) OH5 topology, and (d) T-type topology.

capacitors, and cascaded H-bridge inverters, this topology uses only a DC power supply and lower power electronics providing the same number of the levels.

Figure 5(a) shows the H5 topology [6], composed of a freewheeling circuit by adding a high frequency switch in the positive end of the DC input side, where the efficiency may reach up to 98.1%. However, it suffers from big loss and heat and unbalanced thermal stress. Figure 5(b) shows the structure of the Heric topology [7], where a new freewheeling circuit is added, which itself is composed of a set of bidirectional switch branches on the AC side, based on the traditional full-bridge inverter topology. The efficiency of this topology may reach more than 98%. The OH5 topology is shown in Figure 5(c) [8], which uses a switch and capacitor to form the bidirectional clamping circuit on the basis of the H5 topology, which greatly inhibits the leakage current, and improves the conversion efficiency. However, in such a structure, the clamping circuit is constrained by the dead time of the switch, and a large on-state loss is presented. The work in [9] proposes the FB-DCBP topology, which achieves the complete elimination of the leakage current by adding two controllable switch and clamp diodes in the DC side to format the clamping circuit. The leakage current suppression capability of this topology is stronger than that of the H5 and Heric topologies but suffers from large on-state loss and high number of devices, providing the maximum efficiency of 97.4%.

H6-type topology is proposed in [10], and it is a variant of the Heric topology. It does not require setting dead time between the switches of the same bridge arm and does not pass through the body diode of the switch. Therefore, all switches may be formed by MOSFET, but the topology requires extra two freewheeling diodes, so the cost is increased. Moreover, the efficiency is lower than the Heric topology, and the efficiency is up to 97.6%. The low-leakage current H6 topology is reported in [11], which is a compromise between the H5 and Heric topologies. A new freewheeling circuit is formed based on the H5 topology by adding a switch to make the number of switches through two

half-frequency cycles of the network current at power transfer mode not the same, yielding reduced on-state loss. The efficiency of the H6 topology is lower than that of the Heric topology and higher than that of H5 topology. The common mode is inferior to H5 topology and superior to Heric topology. A common emitter double BUCK topology may be considered [12], composed of four controllable switches and two diodes. The leakage current of this structure is basically zero, and there is no high frequency dead zone between the switches. In addition, this structure presents no breakthrough phenomenon, high reliability, and small switching loss, where the efficiency may reach more than 98.5%. However, the topological magnetic component utilization is low and cannot output reactive current.

The hybrid bridge topology proposed in [13] consists of six controllable switches and two freewheeling diodes. This topology moved the switch on the AC side of the Heric topology to the middle of the bridge arm A, similar to H6-type topology. HB-ZVR (H-bridge zero-voltage state rectifier) topology is proposed in [14], introducing an AC bypass circuit, which itself is composed of a IGBT and a group of diode rectifiers, which is clamped to the midpoint of the two capacitors on the DC bus, to achieve low common mode current and high efficiency inverter topology. The HB-ZVR topology solves the problem that bidirectional switches S5 and S6 of the Heric topology cannot turn on, and this topology will always find a way in the bidirectional switch. Figure 5(d) shows the T-type inverter topology [15], formed by a set of switches Sa3/Sa4 as a bidirectional switch to achieve the main switch Sa1/Sa2 clamping function. It uses the clamp diodes or clamp bit capacitance to improve the midpoint clamping circuit, reducing the number of devices and uneven distribution of the loss. In the topological selection, T-type three-level circuit leverages many advantages of the nonisolation technology as well as the multilevel technology. Therefore, it is very suitable for the photovoltaic grid-connected power generation occasions; however, it is required to effectively suppress the circuit leakage current and system efficiency.

By comparing the above different new topologies, we see that the proposed multilevel inverter topology optimizes the performances of the inverter by adding auxiliary/clamping circuit, using hybrid switch or asymmetric structure.

Figure 6 shows the topology of the hybrid T-type inverter, which is on the basis of T-type structure and composed of nine MOSFET switches, i.e., Sa2, Sb2, Sc2, . . ., Sa4, Sb4, Sc4. We choose IGBT for Sa1, Sb1, and Sc1, since the reverse recovery ability of the body diode in the field effect transistor is poor; therefore they act in low frequencies. The high frequency MOSFET semiconductor switches, i.e., Sa2, Sb2, Sc2, . . ., Sa4, Sb4, Sc4, provide good switching characteristics and low on-resistance. Moreover, due to the low speed characteristics of the built-in diode of MOSFETs, MOSFET cannot be used in the upper bridge arm. We take advantage of the two devices, to reduce the harmonic content and the power loss of the converter and improve the conversion efficiency of the system.

2.3. Loss Analysis of the Proposed Topology. The high power inverter works in high voltage and large current situations,

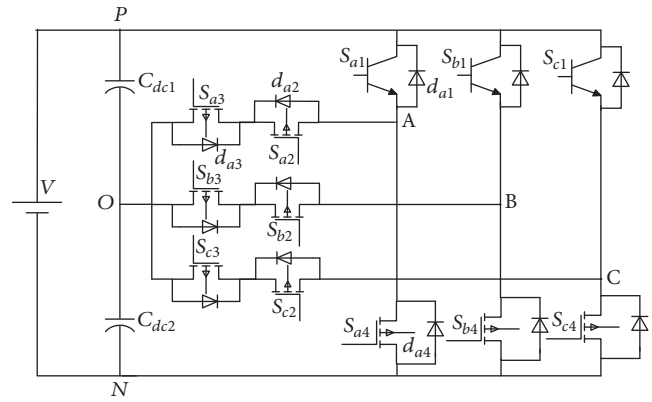


Figure 6: The proposed hybrid T-type inverter.

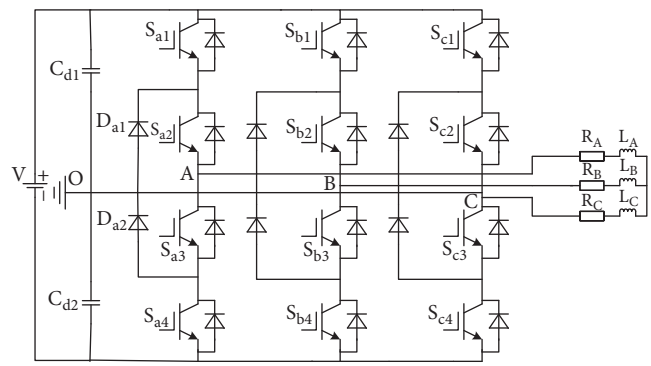


Figure 7: Diode clamped three-level inverter.

where various losses caused by the opening device are relatively large. Besides, optimization of the switching characteristics of the power electronic devices yields bigger conduction losses of the system, especially for soft switching technology, where the switching loss of the power electronic devices is reduced, and the source of the power loss is converted to the conduction loss [16]. Therefore, it is a key step to accurately calculate the state loss for the design of grid-connected inverter systems. Take A phase of Figures 6 and 7 as an example, we compare the various losses of diode clamped (Figure 7) and hybrid T-type (Figure 6) inverter losses and their conversion efficiency. We assume that the output current of the grid-connected inverter is an ideal sine wave; the output voltage of the inverter integrates the conduction period in the period T. Then, the conduction losses per device may be expressed as

$$P_{s_{a1}} = \frac{1}{2\pi}\left[\int_0^{\pi-\theta} d(\omega t)\, U_{\text{com}}(i)\left(I_{\text{com}} \sin(\omega t)\, d(\omega t)\right)\right] \quad (1)$$

where $P_{s_{a1}}$ is the conduction loss of the per device, $d(\omega t)$ is the duty cycle, $U_{\text{com}}(i)$ represents the conduction voltage drop of the IGBT, I_{com} denotes the conduction current peak of the IGBT, and ω is the angle speed. The integral interval from 0 to π-θ is a chopper phase of the semiconductor switch Sa1 in

a fundamental period. The conduction loss of the antiparallel diode in the IGBT reads

$$P_{da1} = \frac{1}{2\pi}\int_{\pi-\theta}^{\pi}\left(-m * \sin\left(\omega t + \phi\right)\right)\left[U_{od}I_{\text{com}}\sin\left(\omega t\right) + R_{od}\left(I_{\text{com}}\sin\left(\omega t\right)\right)^2\right]d\left(\omega t\right) \quad (2)$$

where P_{da1} is the conduction loss of the antiparallel diode in the IGBT, m is the modulation index, Φ is the output power factor angles, and R_{od} and U_{od} are the conduction pressure drop constants of the antiparallel diode.

When IGBT/MOSFET is turned off, the current flows from the clamped diodes and then reads the following clamped diode conduction loss:

$$\begin{aligned} P_{Da1} = {} & \frac{1}{2\pi}\int_{0}^{\pi-\theta}\left(1 - m * \sin\left(\omega t + \phi\right)\right) \\ & \cdot\left[U_{dt}I_{\text{com}}\sin\left(\omega t\right) + R_{dt}\left(I_{\text{com}}\sin\left(\omega t\right)\right)^2\right]d\left(\omega t\right) + \frac{1}{2\pi} \\ & \cdot\int_{0}^{\pi-\theta}\left(1 + m * \sin\left(\omega t + \phi\right)\right)\left[U_{dt}I_{\text{com}}\sin\left(\omega t\right) + R_{dt}\left(I_{\text{com}}\sin\left(\omega t\right)\right)^2\right]d\left(\omega t\right) \end{aligned} \quad (3)$$

where U_{dt} and R_{dt} are the conduction pressure drop constants of the clamped diode.

We considered the DC side voltage of 700 V, carrier frequency fc of 5 kHz, gate resistance of 1.65 ohm, output frequency equal to 60 Hz, modulation rate of unity, and power factor of 0.8. We used MELCOSIM software to simulate the loss. Table 1 presents the calculated loss of different components.

In Table 1, the power losses of Sa1 and Sa4 as well as Sa2 and Sa3 IGBT switches are identical. The four antiparallel diode power dissipations, da1, da2, da3, and da4, are also identical. Moreover, clamping diodes, Da1 and Da2, have the same loss. Table 2 lists the overall loss of the two topologies, which may be calculated based on the number of components contained in two topologies. This table also presents the total power of the inverter, which is 10 kW, and the conversion efficiency of each topology.

The conversion efficiency is lower than 90% because of the higher switching frequency. We chose the frequency of 10 Khz MOSFET, and the switching frequency is relatively high; at the same time the switching loss itself is higher than at power frequency, so the conversion efficiency is lower than 90%.

Table 3 shows the comparison between the NP and T-type three-level inverters.

2.4. SVPWM Control Method. The theoretical basis of the SVPWM is the mean equivalent principle, that is, combining the fundamental voltage vectors in a switching cycle to make the average value equal to the given voltage vector. At a certain moment, the voltage vector rotates into a certain region, which may be achieved by a different combination over time of two adjacent nonzero vectors and zero vectors that make up this region. The action time of the two vectors

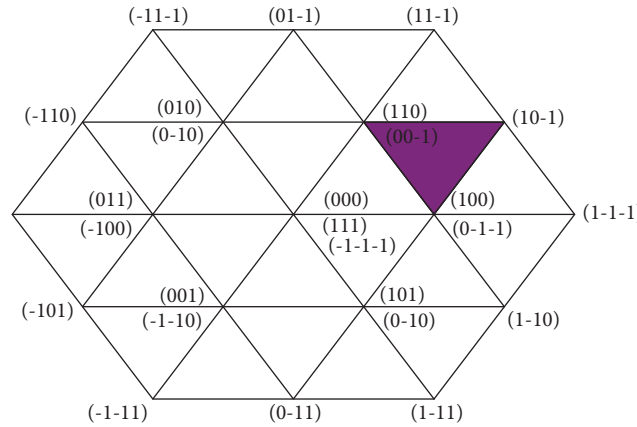


Figure 8: Three-level space vector diagram.

is repeatedly applied in one sampling period, so that it controls the action time of each voltage vector. This rotates the voltage space vector in accordance with the circular trajectory and approaching ideal flux circle through the actual magnetic flux, generated by different switching states of the inverter. Then, it determines the inverter switch state by the comparison, at the end form of the PWM waveform.

SVPWM presents lower total harmonic distortion (THD) compared to other control strategies, and it may refine the steady and dynamic state performances of the PV grid-connected system, simultaneously. Meanwhile, output results of the inverters with SVPWM control strategy provide better power quality than that of the inverters with other control strategies. The SVPWM control strategy with three-phase three-level voltage source inverter is effective and feasible [17]. The detailed equations of the SVPWM strategies based on the proposed topology are as follows.

In this paper we used decomposition hexagon method.

Idea: decompose the multilevel space vector into a combination of multiple two-level space vectors to achieve greatly simplified PWM calculation method.

The three-level space vector diagram is shown in Figure 8. Any reference vector must fall within a small triangle. The vertex of this triangle is the basic voltage vector that composes this reference vector.

The reference vector falling into the shadow in Figure 8 can be decomposed into an offset vector and a two-level vector, as shown in Figure 9.

Steps

2.4.1. Sector Judgments. Based on Clark's transformation, the normalized output vectors transformed from abc to $\alpha\beta$ reference frame may be expressed as

$$\begin{pmatrix} V_\alpha \\ V_\beta \\ V_o \end{pmatrix} = \begin{pmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ 1 & 1 & 1 \end{pmatrix}\begin{pmatrix} V_A \\ V_B \\ V_C \end{pmatrix} \quad (4)$$

Table 1: The loss of each device in hybrid T-type inverter.

Switch type	device	Loss (W)		
		Conduction loss	Switching loss	Total loss
IGBT	S_{a1}	90.45	26.46	116.92
	S_{a2}	31.78	1.03	32.82
Freewheeling diode	d_{a1}	40.59	0.47	41.07
Clamped diode	D_{a1}	2.23	9.93	12.17

Table 2: The power loss and conversion efficiency of two topologies.

component	The number of DC	Loss (W)			conversion efficiency
		IGBT	diode	Total loss	
NPC	1	998.88	310.72	1309.6	0.8690
Hybrid T-type	1	898.44	319.44	1217.88	0.8782

Table 3: Similarities and differences of diode clamped and T-type three-level circuit topologies.

Compared items	Diode clamped three-level inverter	T-type three-level inverter
Switch pressure	Sa1~Sa4: 0.5 UPV	Sa1/Sa2: Upv; Sa3/Sa4: 0.5 Upv
Commutation path	Long commutation path and short commutation path	All paths are consistent
Efficiency	The higher switching frequency (>16 kHZ) increases efficiency	The lower switching frequency (<16 kHZ) increases efficiency
Modulation strategy	Traditional control strategy of current PI loop	Traditional control strategy of current PI loop
Number of components	4 switches plus 2 diodes	4 switches
Drive power	4 groups	3 groups

Table 4: The relations between N and the sector where V_{ref} is located.

N	1	2	3	4	5	6
sector	II	VI	I	IV	III	V

where V_α, V_β, V_o are voltages on the two-phase stationary coordinate system and V_A, V_B, V_C are voltages on the three-phase stationary coordinate system.

We define $N = A+2B+4C$, and the value of N determines in which sector the reference vector V_{ref} is located. So the relations between N and the corresponding sector are shown in Table 4.

2.4.2. Basic Vector Dwell Time Calculation. We assume V_{ref} is located at sector I, which yields the following equation:

$$\begin{aligned} V_\alpha T_s &= T_1 \left|V_1\right| + T_2 \left|V_2\right| \cos\frac{\pi}{3} \\ V_\beta T_s &= T_2 \left|V_2\right| \sin\frac{\pi}{3} \\ T_s &= T_1 + T_2 + T_{0,7} \end{aligned} \tag{5}$$

where T_s is the sampling period; T_1, T_2, and T_0 represent the dwell times of the basic vectors V_1, V_2, and V_0, respectively.

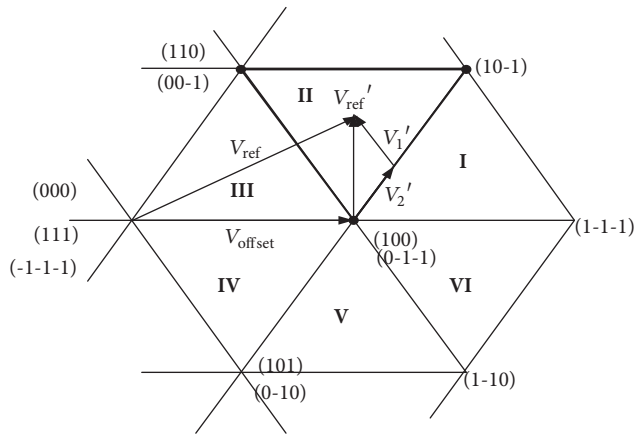


Figure 9: Decomposed two-level space vector diagram.

According to the above expressions, we can obtain the following equation:

$$\begin{aligned} T_1 &= \frac{\sqrt{3}T_S}{2V_{dc}}\left(\sqrt{3}V_\alpha - V_\beta\right) \\ T_2 &= \frac{\sqrt{3}T_s V_\beta}{V_{dc}} \\ T_{0,7} &= T_s - T_1 - T_2 \end{aligned} \tag{6}$$

Table 5: The relations between vector dwelling time and its sector.

sector	I	II	III	IV	V	VI
T_1	Z	Y	-Z	-X	X	-Y
T_2	Y	-X	X	Z	-Y	-Z

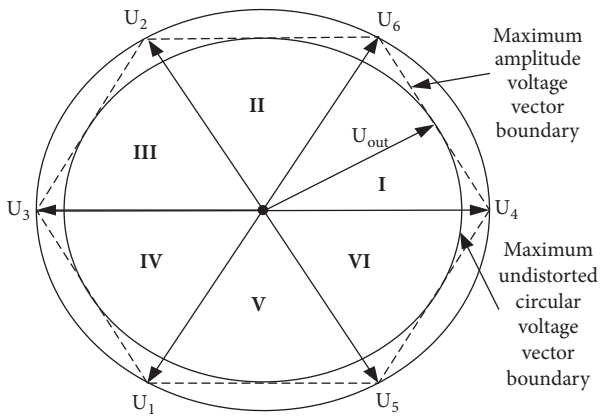


Figure 10: Voltage vector amplitude boundary in SVPWM mode.

Following the same principle, the dwell time of each vector, we achieve V_{ref} of different sectors. To facilitate the solution, we may define it as (7). The value of T_1 and T_2 at different sectors could be set according to Table 5.

$$X = \sqrt{3}\frac{T_S}{V_{dc}}V_\beta$$
$$Y = \frac{T_s}{V_{dc}}\left(\frac{\sqrt{3}}{2}V_\beta + \frac{\sqrt{3}}{2}V_\alpha\right) \quad (7)$$
$$Z = \frac{T_s}{V_{dc}}\left(\frac{\sqrt{3}}{2}V_\beta - \frac{\sqrt{3}}{2}V_\alpha\right)$$

2.4.3. Vector Switching Point Calculation. When the synthesized voltage vector endpoint falls between the regular hexagon and the circumscribed circle, as shown in Figure 10, the overmodulation has occurred and the output voltage will be distorted. So we use a proportional scaling algorithm to control the overmodulation. The vector dwell time that first occurs in each sector is defined as T_{Nx}, and the vector dwell time that occurs after is defined as T_{Ny}. When $T_x + T_y \leqslant T_{\text{NPWM}}$, the vector endpoint is within the regular hexagon and no overmodulation occurs. When $T_{\text{Nx}} + T_{\text{Ny}} > T_{\text{NPWM}}$, the vector endpoint is beyond the regular hexagon and overmodulation occurs. The output waveform will be seriously distorted and must take the following measures.

Suppose that the nonzero vector dwell time is T'_{Nx}, T'_{Ny}, when the endpoint of the voltage vector trace is pulled back to the inscribed circle of the regular hexagon, and then there is a proportional relationship:

$$\frac{T'_{Nx}}{T_{Nx}} = \frac{T'_{Ny}}{T_{Ny}} \quad (8)$$

Therefore, T'_{Nx}, T'_{Ny}, T_{N0}, T_{N7} can be obtained by the following formula:

$$T'_{Nx} = \frac{T_{Nx}}{T_{Nx} + T_{Ny}}T_{N\text{PWM}}$$
$$T'_{Ny} = \frac{T_{Ny}}{T_{Nx} + T_{Ny}}T_{N\text{PWM}} \quad (9)$$
$$T_0 = T_7 = 0$$

According to the above process, the action time of two adjacent voltage space vectors and zero-voltage vectors in each sector can be obtained. The operation relationship is shown in Figure 11 when U_{ref} is in sector I. After the U_{ref} sector and the corresponding effective voltage vector are determined, according to the PWM modulation principle, the value of each corresponding comparator is calculated, and the operation relationship is as follows:

$$t_{\text{aon}} = \frac{\left(T_s - T_x - T_y\right)}{2}$$
$$t_{\text{bon}} = t_{\text{aon}} + T_x \quad (10)$$
$$t_{\text{con}} = t_{\text{bon}} + T_y$$

Other sectors follow the same above principle.

Here, T_{cm1}, T_{cm2}, T_{cm3} denote the transistor's switching time. And the relation between sector switching point and its appropriate sector is tabulated in Table 6.

3. Results and Discussion

This study put forward a novel hybrid T-type inverter topology which is composed of basic units A and B on the basis of previous research studies. We established a three-phase three-level hybrid T-type photovoltaic grid-connected inverter topology model, which is shown in Figure 12, using MATLAB platform. Considering the A-phase bridge leg, for example, it consists of one half-bridge IGBT, one half-bridge MOSFET, and two neutral point MOSFETs. Switches Sa1 and Sa2 work in the mutual intermittent state, and switches Sa3 and Sa4 only work near the current zero-crossing point with high frequency. This topology is rather suited for the photovoltaic nonisolated AC system applications.

The topological structure is on the basis of T-type structure, changing the nine switches into MOSFET, i.e., Sa2, Sb2, Sc2 $\cdots$ Sa4, Sb4, and Sc4. We choose IGBT for Sa1, Sb1, and Sc1; since the reverse recovery ability of the body diode in the field effect transistor is poor, therefore they act in low frequencies. The high frequency MOSFET semiconductor switches, i.e., Sa2, Sb2, Sc2, . . ., Sa4, Sb4, Sc4, provide good switching characteristics and low on-resistance. Moreover, due to the low speed characteristics of the built-in diode of MOSFETs, MOSFET cannot be used in the upper bridge arm. We take advantage of the two devices, to reduce the harmonic content and the power loss of the converter and improve the conversion efficiency of the system.

Regarding the topology selection, the three-level circuit combines the advantages of the nonisolation and multilevel

Table 6: The relationship between the vector switching point and its corresponding sector.

sector	I	II	III	IV	V	VI
T_a	T_{bon}	T_{aon}	T_{aon}	T_{con}	T_{con}	T_{bon}
T_b	T_{aon}	T_{con}	T_{bon}	T_{bon}	T_{aon}	T_{con}
T_c	T_{con}	T_{bon}	T_{con}	T_{aon}	T_{bon}	T_{aon}

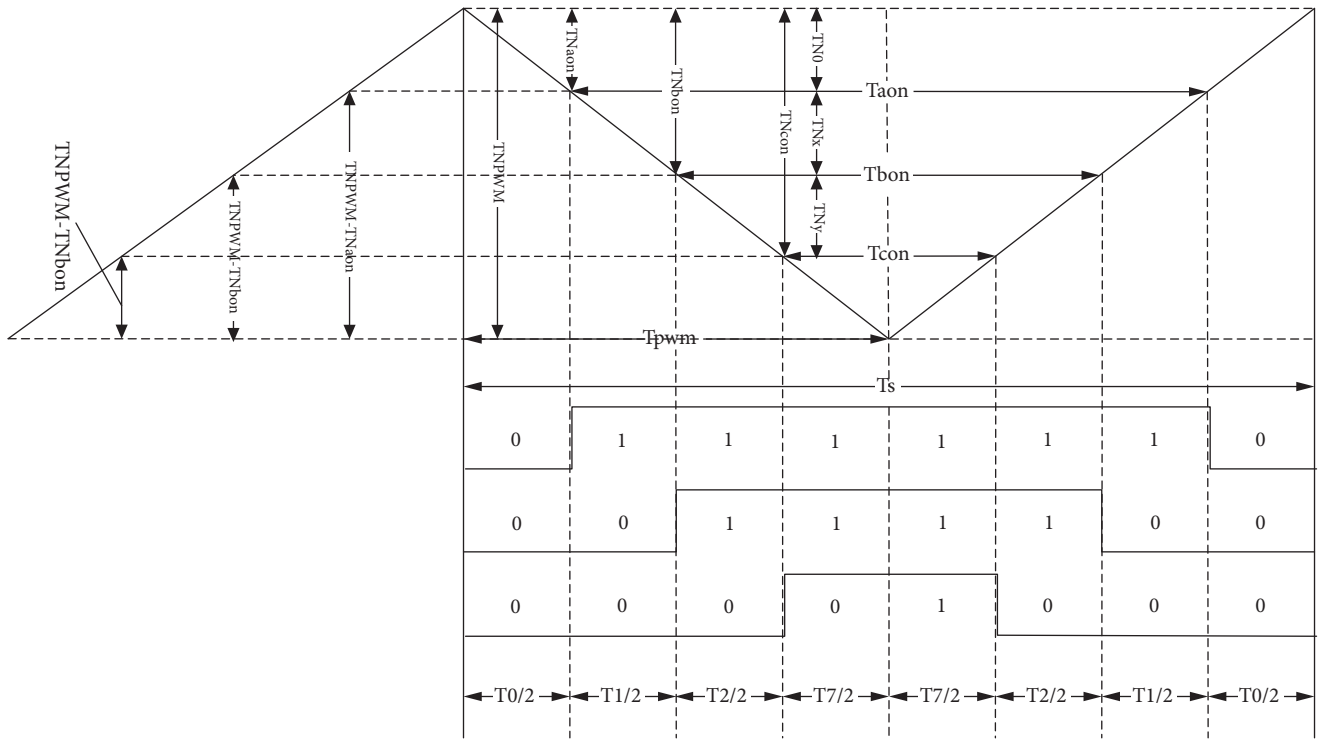


Figure 11: Operation relationship when U_{ref} is in sector I.

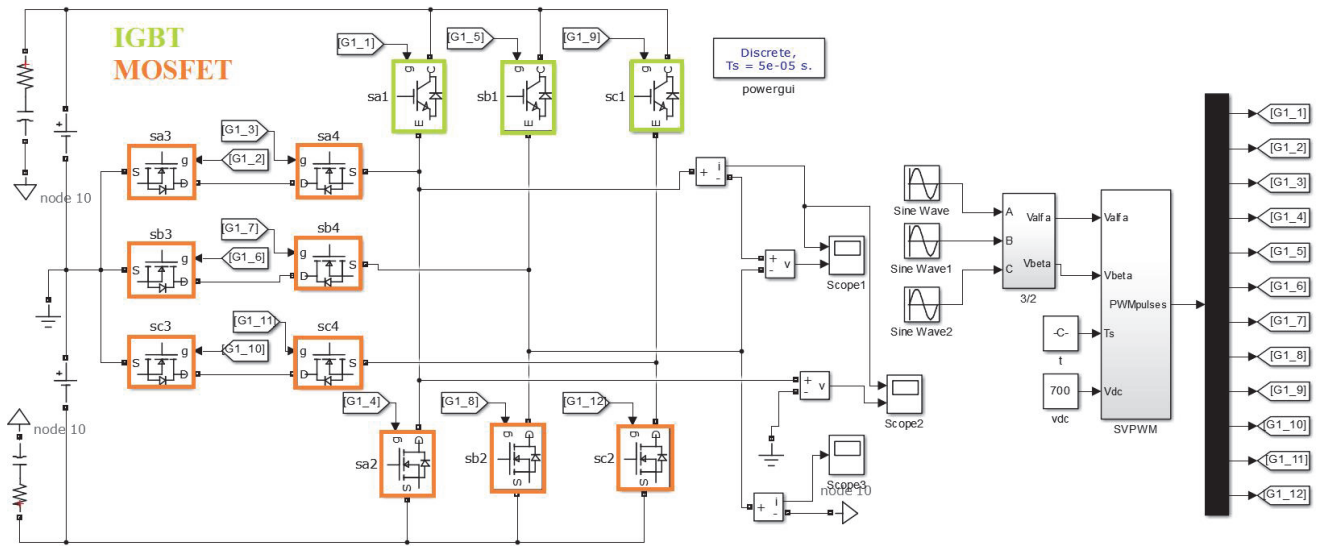


Figure 12: The simulation model of the SVPWM controlled novel T-type three-phase three-level inverter.

Table 7: The classification of the influence of the switching state of the short and medium vectors on the direction of the neutral point current.

Positive short vector switching status	io	Negative short vector switching status	io	Medium vector switching status	io
100	ia	211	- ia	210	ib
221	ic	110	- ic	120	ia
010	ib	121	- ib	021	ic
122	ia	011	- ia	012	ib
001	ic	112	- ic	102	ia
212	ib	101	- ib	201	ic

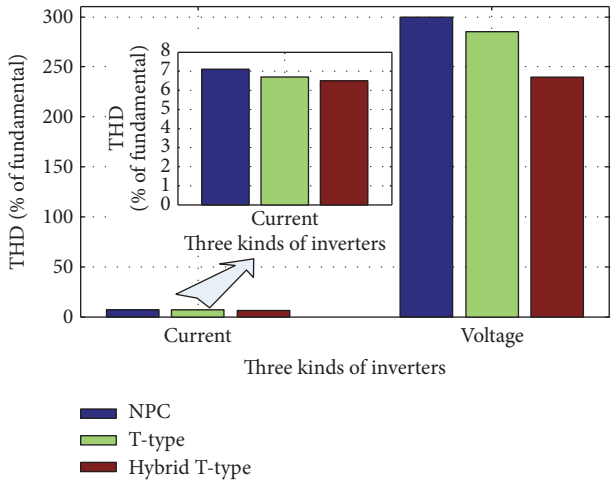


Figure 13: The current and voltage THD comparison of three types of inverters.

technologies, which is very suitable for the photovoltaic grid-connected power generation.

System simulation parameters are as follows: The DC-link voltage is 700 V, with the frequency of 50 Hz, the value of the support capacitor reads 3300 uF, with the AC-side inductance of 3 mH, the AC-side resistance is 0.1 Ω, and the switching frequency is 10 kHz. The value of the stray capacitance is 10e−6 F, and the small resistor is connected in parallel with the stray capacitance of $R = 10e - 6$ ohm.

Table 7 shows the neutral point current when the positive and negative short vector and medium vector act. It can be seen that positive and negative short vector and medium vectors will cause neutral voltage fluctuations.

The neutral point voltage control method is based on the SVPWM. According to the influence of the medium and short vectors on the neutral point voltage offset and by selecting the appropriate switching state and the most suitable switching sequence for the neutral point voltage, the midpoint voltage offset during each control cycle has been minimized.

So selecting the excellent transistor sequence is really important. To solve this problem we run through all the transistors in every possible combination and permutation on the condition of the following switch rules.

(1) The switching states of the devices in every bridge leg are independent. (2) The switching states of any two adjacent switches of each bridge leg are complementary (e.g., if Sa1 is turned on, then Sa2 must be switched off). (3) According to the principle of complementarity, if the switching state of any of the devices in the same bridge leg is determined, the state of the other switching devices of that bridge leg can also be confirmed [18].

The influence of harmonic current on the power grid is greater than the harmonic voltage and it is the fundamental cause of most of the problems, and the neutral voltage fluctuations are proportional to the amount of the harmonic current. So, as can be seen from Table 8, giving comprehensive consideration, choose the following optimal transistor sequence: Sa1-Sa3-Sa4-Sa2-Sb1-Sb3-Sb4-Sb2-Sc1-Sc3-Sc4-Sc2.

The control method is achieved by the SVPWM with 12 trigger pulses. Switching sequence reads Sa1-Sa3-Sa4-Sa2-Sb1-Sb3-Sb4-Sb2-Sc1-Sc3-Sc4-Sc2.

Figure 13 shows the output voltage and current harmonic content of the three types of inverter topology structure, using SVPWM control method. From Figure 13 we could see that current and phase voltage THD (total harmonic distortion) of the NPC inverter is the biggest, the T-type inverter is the middle one, and the proposed hybrid T-type is the smallest one. Meanwhile, the amplitude of the three kinds of inverter current harmonics is not obvious; however, the voltage THD results of the three kinds of inverter are sharply comparable.

The topology and control strategy of the two circuits are the same, except the devices used. The T-type topology consists of 12 IGBTs, while the hybrid T-type topology consists of 9 MOSFETs and 3 IGBTs. And the off-delay time and dead time of the IGBT are longer than those of the MOSFET.

Although the proportion of dead time is often very small relative to one switching cycle, the dead zone will make the three-phase control system deviate from the ideal mathematical model. When the switching frequency becomes higher, the dead-zone effect will gradually accumulate, and when it accumulates to a certain degree, it will distort the AC-side voltage waveform, which will affect the waveform quality of the input current. It will also cause fluctuations in the DC voltage, which degrades the accuracy of the entire system. In addition, the dead time can cause common mode voltage waveform distortion, resulting in higher harmonics [19]. So the THD of the novel T-type inverter is the lowest.

From Figure 14 we see that the common mode current of the proposed novel T-type inverter is smaller than the previous T-type inverter topology. In conclusion the proposed

Table 8: Comparison of output parameters under various switching sequence (simulation time: 0.1 s).

Sequence of the transistors	Power factor	Current harmonics%	voltage harmonics%
Sa1- Sa2- Sb1- Sb2- Sc1- Sc2- Sa3- Sa4- Sb3- Sb4- Sc3- Sc4	0.7209	27.27	158.99
Sa1- Sa2- Sb1- Sb2- Sc1- Sc2- Sa4- Sa3- Sb4- Sb3- Sc4- Sc3	0.7263	21.73	236.75
Sa1- Sc2- Sb1- Sa2- Sc1- Sb2- Sa3- Sa4- Sb3- Sb4- Sc3- Sc4	0.647	11.61	149.13
Sa1- Sc2- Sb1- Sa2- Sc1- Sb2- Sa4- Sa3- Sb4- Sb3- Sc4- Sc3	0.6158	7.81	224.95
Sa1- Sa2- Sa3- Sa4- Sb1- Sb2- Sb3- Sb4- Sc1- Sc2- Sc3- Sc4	0.5799	0.63	156.03
Sa1- Sa2- Sa4- Sa3- Sb1- Sb2- Sb4- Sb3- Sc1- Sc2- Sc4- Sc3	0.447	0.92	230.51
Sa1- Sa3- Sa4- Sa2- Sb1- Sb3- Sb4- Sb2- Sc1- Sc3- Sc4- Sc2	0.7132	6.61	248.44
Sa1- Sa4- Sa3- Sa2- Sb1- Sb4- Sb3- Sb2- Sc1- Sc4- Sc3- Sc2	0.6225	6.91	158.98

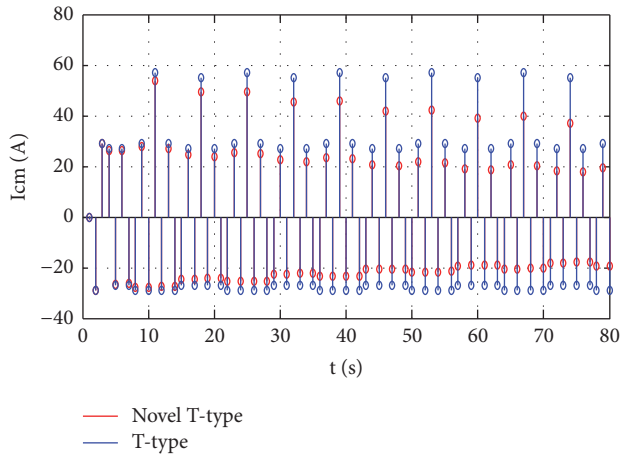


Figure 14: The obtained CM-current of the novel and previous T-type inverters.

hybrid T-type inverter has priority compared to the NPC and T-type inverter.

The instantaneous common mode voltage and ground leakage current could be given by the following equation:

$$u_{cm} = \frac{u_{AN} + u_{BN} + u_{CN}}{3}$$
$$i_{cm} = C\frac{d_{u_{cm}}}{dt} \quad (11)$$

where u_{AN}, u_{BN}, and u_{CN} are the pulse voltages between the branch midpoint and the dc bus minus terminal, respectively

It can be seen from the equation that the common mode current i_{cm} is proportional to the change rate of the common mode voltage u_{cm}.

According to the above interpretation it can be got that the dead time of the proposed topology is the shortest because of the smallest number of IGBTs compared with the other two topologies, so that the common mode voltage and current are also the smallest.

4. Conclusions

We introduced a variety of new multilevel photovoltaic grid-connected inverter topologies, compared them with each other, and classified them according to the basic unit which predecessors proposed. We proposed the hybrid T-type inverter topology, which is composed of two best basic units. This structure makes full advantages of the two devices, which leads to reducing the harmonic content and power loss of the converter and improving the conversion efficiency of the system. By comparing the new topology, the new multilevel inverter topology is formed by the basic constituent elements to increase the auxiliary/embedded circuit or with a hybrid switch or with asymmetric structure to optimize the inverter performance. We use the space vector pulse width modulation (SVPWM) method to build the SIMULINK models of the proposed hybrid T-type and NPC three-level inverter in the MATLAB software and compare them with each other. The simulation results show that the proposed topology presents lower output harmonics than the NPC topology. We then provided further loss analysis for these two topologies, using the MELCOSIM software to calculate the loss of different components in each topology as well as the total power loss. The outcome is that the loss of the T-type topology is significantly lower than that of the NPC topology, and the conversion efficiency is higher than that of the NPC topology. Moreover the simulation results show that the common mode current of the proposed novel T-type inverter is smaller than the previous T-type inverter topology.

The proposed inverter topology has a certain practicality and economy to meet the actual needs.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

All the authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

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Research Article

Feedforward Harmonic Mitigation Strategy for Single-Phase Voltage Source Converter

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With the development of distributed generations (DGs), single-phase voltage source converter (SPVSC) has been widely used, but it brings about the problem of harmonic pollution to power grid. Hence, it is significant to explore the mechanism of harmonic injection from SPVSC and propose effective control strategies to mitigate the harmonic pollution. In this paper, a harmonic analysis model of SPVSC based on dynamic phasor (DP) has been established. With the model, the harmonics interaction between the ac side and the dc side can be analyzed with the consideration of the control strategies, which reveals the generation mechanism of the harmonics in SPVSC. Based on the mechanism, a feedforward harmonic mitigation strategy has been presented. The principle of the strategy is to add low-order harmonic signal to the PWM modulation signals to reduce the harmonic current on the ac side. The harmonic mitigation strategy not only has clear physical meaning and fast calculation, but also is robust for the uncertainty of parameters. Finally, the simulation and experiment results demonstrate the correctness of the model and the effectiveness of the harmonic mitigation strategy.

1. Introduction

Because of the capability of unity power factor and bidirectional energy flow, single-phase voltage source converters (SPVSC) have been widely applied in various industrial fields [1, 2], such as serving as the grid-connected interface of distributed generations (DGs) or microgrid with renewable energy systems [3, 4]. However, due to the strong nonlinearity of power electronic devices, SPVSC also brings about the problem of harmonic pollution which has a negative impact on power grid [5–7]. Hence, it is necessary to analyze the mechanism of harmonic injection and propose effective suppression measurements, laying a solid foundation for the promotion of SPVSC.

Three-phase VSC generates high-order harmonics under normal situation, which can generally be filtered by low pass filter [8], while SPVSC generates not only high-order harmonics but also low-order harmonics [9] even in normal situation, which is hard to be eliminated. The harmonic current generated from SPVSC is eliminated mainly from two aspects [10, 11]. One solution is to remove harmonic ripples in the voltage-loop and strengthen the antiharmonic disturbance capacity of current loop. Since harmonic ripples in the voltage-loop can be easily removed by employing low pass voltage filter [12] or notch filter [11], most studies focus on how to improve the performance of current-loop controller. Proportional Resonant (PR) controller [13, 14], which has the advantages of simplicity and zero steady-state error for tracking a sinusoidal signal, is widely used for selective harmonic elimination. However, it has high sensitivity to the frequency variations and may not be able to achieve a good effect, since a single PR controller only eliminates a single-order harmonic. Multiresonant controllers (MRCs) suppress harmonic distortions effectively by connecting PR controllers at harmonic frequency in parallel, but this causes heavy paralleling computation duty, particularly when high-order harmonics are required to be compensated. In the worst case, MRCs cause the system to be unstable [15]. In [16, 17], Repetitive Controller (RC) has been investigated which involved complicated analysis and designation. It is based on internal model principle and achieves zero steady-state error for tracking a sinusoidal signal. RC presented a much slower dynamic response than PR and MRCs. To achieve a minimum steady-state error while maintaining a fast-transient

response, a hybrid controller by combining PR and RC has been proposed in [12, 18]. However, the designation controller parameters were very complex to ensure the effectiveness of the control strategy and the stability of system.

The other solution is to add harmonic modulation signals to PWM modulated signals to offset harmonic currents on the ac side. Without additional controller, it can be implemented simply and has less computational burden. Moreover, the strategy not only can achieve a fast-dynamic response but also will not affect the stability of system no matter how many order harmonics need to be suppressed. Before the suppression strategy is put forward, it is important to establish an accurate harmonic analysis model which can reflect the harmonic generation mechanism. As an alternative to the traditional modeling approach [19, 20], dynamic phasor (DP) method is very useful for the harmonic analysis of SPVSC [21–23]. It was based on a linear time varying periodic (LTP) theory and considered the detailed switching dynamic of power electronic devices. DP was also very effective in revealing dynamical couplings between various quantities [24]; thus it was possible to analyze how harmonics transferred between ac and dc side of VSC.

To address the above issues, this paper develops a harmonic analysis model of SPVSC based on the dynamic phasor and the harmonic generation mechanism of SPVSC has been investigated comprehensively. According to such mechanism, a feedforward control strategy is put forward to mitigate the harmonics on grid side. The organization of this paper is as follows: in Section 2, the system configuration and time-domain model of SPVSC are shown and harmonic analysis model based on DP is investigated; in Section 3, the generation mechanism and transmission law of harmonic for SPVSC are analyzed; in Section 4, a feedforward harmonic mitigation strategy is proposed on the basis of the generation mechanism; in Sections 5 and 6, the simulation and experimental results are presented to verify the proposed model and harmonic mitigation strategy. Finally, the conclusion is drawn in Section 7.

2. Harmonic Analyzing Model of SPVSC

2.1. Time-Domain Model of SPVSC. The SPVSC topology studied in this paper is a single-phase H bridge voltage source converter as shown in Figure 1. U_s is the ac source voltage. R and L are the equivalent resistance and impendence of the ac system. I_R and U_{Rac} are the ac side current and voltage of SPVSC, respectively. U_{dc} is the voltage on dc side. C_{dc} is the capacitor on the dc side. R_{dc} is the equivalent resistance of the dc loads. I_{dc} and I_l are the output current and dc load current on the dc side. V_1, V_2, V_3, and V_4 are power electronic devices of converter.

The time-domain model of SPVSC can be described by

$$L\frac{dI_R}{dt} = U_s - RI_R - U_{Rac}$$
$$C_{dc}\frac{dU_{dc}}{dt} = I_{dc} - \frac{U_{dc}}{R_{dc}}. \quad (1)$$

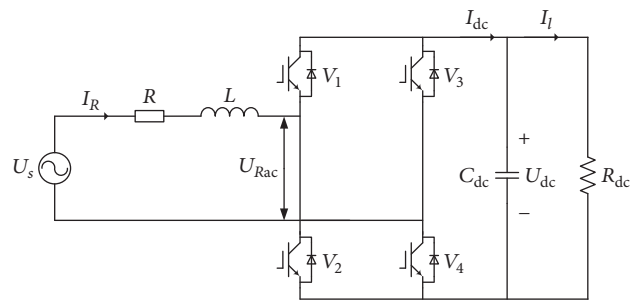


Figure 1: Topology of single-phase VSC.

The switching function is used to describe the interaction between the ac and dc side of SPVSC, so U_{Rac} and I_{dc} in (1) can be given as

$$U_{Rac} = S_R U_{dc}$$
$$I_{dc} = S_R I_R, \quad (2)$$

where S_R is the switching function of SPVSC. When V_1 and V_4 are switched on, it is 1, and when V_2 and V_3 are on, it is −1. S_R is related to the control strategy and determined by the PWM signal.

As shown in Figure 2, double closed-loop control strategy is occasionally employed in the control of converter. The dc-link voltage out-loop is controlled by a proportional integral (PI) controller and the peak value of reference current I_{m_ref} is obtained. I_{m_ref} is multiplied by $\cos\theta$, which is the ac system voltage phase cosine captured by phase locked loop (PLL), so as to operate at unity power factor. The current inner loop is controlled by proportional (P) controller to track the ac side current reference value I_{t_ref}.

What needs to be specially mentioned is that, considering the phase delay in the sampling, grid voltage feedforward sampling value U_{st} is obtained by multiplying the fundamental RMS of U_s with $\cos\theta$. After subtracting U_{st} from the output value of current controller and being divided by U_{dc_ref}, the modulation signal of SPVSC is obtained

$$U_m = \frac{1}{U_{dc\_ref}}\left[U_{st} - K_{ip}\left(I_{t\_ref} - I_R\right)\right], \quad (3)$$

where K_{ip} is the proportional regulation gain of current inner loop, U_{st} is the sampling value of grid voltage, U_{dc_ref} is the reference of dc voltage, and I_R and I_{t_ref} are the actual value and reference value of ac side current, respectively. I_{m_ref} is the peak value of reference current which can be obtained by $I_{m\_ref} = \sqrt{2}u_{dc}I_{dc}/U_{rms}$.

2.2. Dynamic Phasor Harmonic Analysis Model of SPVSC. The SPVSC time-domain model described by (1) and (2) can be transformed into dynamic phasor model, and the k-order

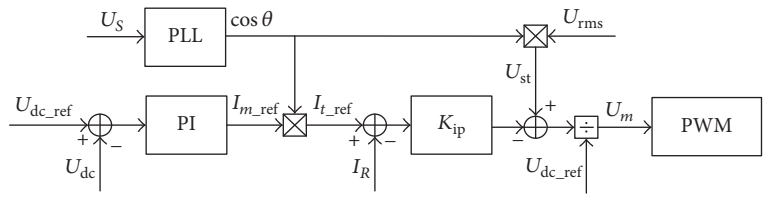


Figure 2: Double closed-loop control structure of voltage and current.

dynamic phase equation of the ac side current and the dc side voltage is expressed as

$$\begin{aligned}\frac{d\langle I_R\rangle_k}{dt} &= -\left(\frac{R}{L}+jk\omega_s\right)\langle I_R\rangle_k - \frac{\langle U_{\text{dc}}S_R\rangle_k}{L} + \frac{\langle U_s\rangle_k}{L}\\ \frac{d\langle U_{\text{dc}}\rangle_k}{dt} &= -\left(\frac{1}{R_{\text{dc}}C_{\text{dc}}}+jk\omega_s\right)\langle U_{\text{dc}}\rangle_k + \frac{\langle I_R S_R\rangle_k}{C_{\text{dc}}},\end{aligned} \tag{4}$$

where $\omega_s = 2\pi/T$ is the angular frequency and $\langle\cdot\rangle_k$ denotes the kth dynamic phasor.

$\langle U_{\text{dc}}S_R\rangle_k$ and $\langle I_R S_R\rangle_k$ are the convolution of switching function and dc side voltage or ac side current, respectively, which represents the interaction of harmonics between the ac and dc sides of SPVSC. It can be described by

$$\begin{aligned}\langle U_{\text{dc}}S_R\rangle_k &= \sum_i \langle S_R\rangle_{k-i}\langle u_{\text{dc}}\rangle_i\\ \langle I_R S_R\rangle_k &= \sum_i \langle S_R\rangle_{k-i}\langle I_R\rangle_i.\end{aligned} \tag{5}$$

In this paper, SPWM modulation with fixed switching frequency is adopted, so the dynamic phasor of switching function is determined by U_m and can be given as

$$\begin{aligned}\langle S_R\rangle_k &= \langle U_m\rangle_k\\ &= \frac{1}{U_{\text{dc\_ref}}}\left[\langle U_{\text{st}}\rangle_k - K_{\text{iP}}\left(\langle I_{t\_\text{ref}}\rangle_k - \langle I_R\rangle_k\right)\right].\end{aligned} \tag{6}$$

Since U_{st} and I_{t_ref} have only the fundamental component, the kth dynamic phasor is equivalent to 0, except $\langle U_{\text{st}}\rangle_1 \neq 0$ and $\langle I_{t\_\text{ref}}\rangle_1 \neq 0$. This paper is mainly aimed at the lower-order harmonic component within 13 orders, so the high-order component of the dynamic phasor of the switching function can be neglected. Equation (6) can be simplified as

$$\langle S_R\rangle_k = \begin{cases}\dfrac{\langle U_{\text{st}}\rangle_1 - K_{\text{iP}}\langle I_{t\_\text{ref}}\rangle_1}{U_{\text{dc\_ref}}} + \dfrac{K_{\text{iP}}\langle I_R\rangle_1}{U_{\text{dc\_ref}}}, & k=1\\ \dfrac{K_{\text{iP}}\langle I_R\rangle_k}{U_{\text{dc\_ref}}}, & k=2,\ldots,13.\end{cases} \tag{7}$$

By substituting (7) into (4), the kth dynamic phasor equation of the ac side current and the dc side voltage is obtained as follows:

$$\begin{aligned}\frac{d\langle I_R\rangle_k}{dt} &= -\left(\frac{R}{L}+jk\omega_s\right)\langle I_R\rangle_k + \frac{\langle U_s\rangle_k}{L}\\ &\quad - \frac{K_{\text{iP}}}{U_{\text{dc\_ref}}L}\sum_i \langle I_R\rangle_{k-i}\langle u_{\text{dc}}\rangle_i\\ &\quad - \frac{\langle U_{\text{st}}\rangle_1 - K_{\text{iP}}\langle I_{t\_\text{ref}}\rangle_1}{U_{\text{dc\_ref}}L}\langle u_{\text{dc}}\rangle_{k-1}\\ &\quad - \frac{\langle U_{\text{st}}\rangle_{-1} - K_{\text{iP}}\langle I_{t\_\text{ref}}\rangle_{-1}}{U_{\text{dc\_ref}}L}\langle u_{\text{dc}}\rangle_{k+1},\end{aligned} \tag{8}$$

$$\begin{aligned}\frac{d\langle u_{\text{dc}}\rangle_k}{dt} &= -\left(\frac{1}{R_{\text{dc}}C}+jk\omega_s\right)\langle u_{\text{dc}}\rangle_k\\ &\quad + \frac{\langle U_{\text{st}}\rangle_1 - K_{\text{iP}}\langle I_{t\_\text{ref}}\rangle_1}{U_{\text{dc\_ref}}C}\langle I_R\rangle_{k-1}\\ &\quad + \frac{\langle U_{\text{st}}\rangle_{-1} - K_{\text{iP}}\langle I_{t\_\text{ref}}\rangle_{-1}}{U_{\text{dc\_ref}}C}\langle I_R\rangle_{k+1}\\ &\quad + \frac{K_{\text{iP}}}{U_{\text{dc\_ref}}C}\sum_i \langle I_R\rangle_{k-i}\langle I_R\rangle_i,\end{aligned} \tag{9}$$

where $\langle I_{t\_\text{ref}}\rangle_{-1} = \langle I_{t\_\text{ref}}\rangle_1^*$ and $\langle U_{\text{st}}\rangle_{-1} = \langle U_{\text{st}}\rangle_1^*$, according to the conjugate property of dynamic phasor. In the convolution $\sum\langle I_R\rangle_{k-i}\langle u_{\text{dc}}\rangle_i$ and $\sum\langle I_R\rangle_{k-i}\langle I_R\rangle_i$, the product of two small quantities can be neglected. It means that only the items including dc component of voltage on dc side or fundamental current on ac side should be considered. Therefore, the accumulation of items in (8) and (9) can be simplified as

$$\begin{aligned}\sum_i \langle I_R\rangle_{k-i}\langle u_{\text{dc}}\rangle_i &= \langle I_R\rangle_k\langle u_{\text{dc}}\rangle_0 + \langle I_R\rangle_1\langle u_{\text{dc}}\rangle_{k-1} + \langle I_R\rangle_1^*\langle u_{\text{dc}}\rangle_{k+1}\\ \sum_i \langle I_R\rangle_{k-i}\langle I_R\rangle_i &= 2\langle I_R\rangle_{k-1}\langle I_R\rangle_1 + 2\langle I_R\rangle_{k+1}\langle I_R\rangle_1^*.\end{aligned} \tag{10}$$

The kth dynamic phasor of current on ac side and voltage on dc side can be obtained by solving (8) and (9). The calculation results are the different order harmonics of current on ac side and voltage on dc side. Therefore, the

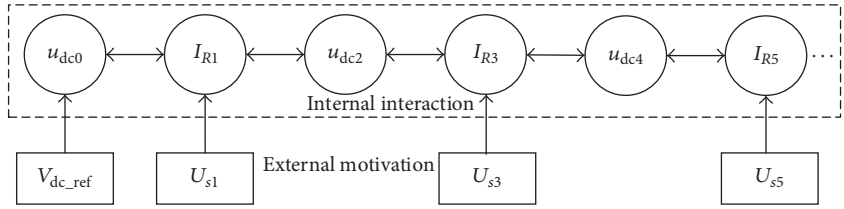


Figure 3: Harmonic interaction law of single-phase VSC.

dynamic phasor model of SPVSC can be used to analyze the generation mechanism of harmonic.

3. Mechanism of SPVSC Harmonic Generations

In the steady state, the dc component of dc side voltage is equivalent to its reference; that is, $\langle u_{dc}\rangle_0 = V_{dc\_ref}$. The differential of the dynamic phasor of ac side current and the dc side voltage can be neglected, so $d\langle I_R\rangle_k/dt = 0$ and $d\langle u_{dc}\rangle_k/dt = 0$. The harmonic generation mechanism of SPVSC under steady-state conditions is analyzed below.

The dc voltage on dc side can be obtained by (8), as shown in

$$\begin{aligned}&\frac{1}{R_{dc}}\langle u_{dc}\rangle_0\\&\quad=\frac{\langle U_{st}\rangle_1-K_{iP}\left(\langle I_{t\_ref}\rangle_1-\langle I_R\rangle_1\right)}{U_{dc\_ref}}\langle I_R\rangle_1^*\\&\quad+\frac{\langle U_{st}\rangle_1^*-K_{iP}\left(\langle I_{t\_ref}\rangle_1^*-\langle I_R\rangle_1^*\right)}{U_{dc\_ref}}\langle I_R\rangle_1.\end{aligned}\tag{11}$$

Equation (11) can describe the interaction between the dc voltage on dc side and the fundamental current on ac side.

Similarly, the fundamental current on ac side can be further written as

$$\begin{aligned}&\left(R+j\omega_sL\right)\langle I_R\rangle_1\\&\quad=-\frac{\langle U_{st}\rangle_1-K_{iP}\left(\langle I_{t\_ref}\rangle_1-\langle I_R\rangle_1\right)}{U_{dc\_ref}}\langle u_{dc}\rangle_0\\&\quad-\frac{\langle U_{st}\rangle_1^*-K_{iP}\left(\langle I_{t\_ref}\rangle_1^*-\langle I_R\rangle_1^*\right)}{U_{dc\_ref}}\langle u_{dc}\rangle_2\\&\quad+\langle U_s\rangle_1.\end{aligned}\tag{12}$$

Therefore, the fundamental current on ac side not only interacts with the dc voltage on dc side, but also interacts with the 2nd harmonic voltage on dc side.

The 2nd harmonic voltage on dc side and the 3rd harmonic current on ac side can be expressed as follows:

$$\begin{aligned}&\left(\frac{1}{R_{dc}}+j2C\omega_s\right)\langle u_{dc}\rangle_2\\&\quad=-\frac{\langle U_{st}\rangle_1-K_{iP}\left(\langle I_{t\_ref}\rangle_1-\langle I_R\rangle_1\right)}{V_{dc\_ref}}\langle I_R\rangle_1\\&\quad-\frac{\langle U_{st}\rangle_1^*-K_{iP}\left(\langle I_{t\_ref}\rangle_1^*-\langle I_R\rangle_1^*\right)}{V_{dc\_ref}}\langle I_R\rangle_3\\&\quad+\frac{K_{iP}\langle I_R\rangle_3\langle I_R\rangle_1^*}{V_{dc\_ref}},\end{aligned}\tag{13}$$

$$\begin{aligned}&\left(R+j3\omega_sL+K_{iP}\right)\langle I_R\rangle_3\\&\quad=-\frac{\langle U_{st}\rangle_1-K_{iP}\left(\langle I_{t\_ref}\rangle_1-\langle I_R\rangle_1\right)}{V_{dc\_ref}}\langle u_{dc}\rangle_2\\&\quad-\frac{\langle U_{st}\rangle_1^*-K_{iP}\left(\langle I_{t\_ref}\rangle_1^*-\langle I_R\rangle_1^*\right)}{V_{dc\_ref}}\langle u_{dc}\rangle_4\\&\quad+\langle U_s\rangle_3.\end{aligned}\tag{14}$$

In (13), the state variables on the right are $\langle I_R\rangle_1$ and $\langle I_R\rangle_3$, which indicates that the 2nd harmonic voltage on dc side not only interacts with the fundamental current on ac side, but also interacts with the 3rd harmonic current on ac side. Similarly, it can be obtained from (14) that the 3rd harmonic current on ac side not only interacts with the 2nd harmonic voltage on dc side, but also interacts with the 4th harmonic voltage on dc side. Meanwhile, the 3rd voltage background harmonic of power grid will also induce the 3rd harmonic current on ac side. Therefore, the generation mechanism and interaction law of harmonic current on ac side and harmonic voltage on dc side can be summarized as in Figure 3.

In Figure 3, u_{dci} and I_{Ri} are ith harmonic voltage on dc side and ith harmonic current on ac side, respectively. V_{dc_ref} is the dc voltage reference in controller. U_{si} is ith harmonic voltage of ac side source. The single arrow represents the effect of external excitation on harmonics, and the double arrow represents the interaction between two variables.

There are two reasons for the lower-order harmonic generation of SPVSC, that is, external excitation and internal interaction. From the internal interaction, SPVSC will generate a series of odd harmonic currents on ac side and a series of even harmonic voltages on dc side. From the

external excitation relationship, it can be concluded that when the voltage of power grid is distorted, it will aggravate the harmonic generation from SPVSC and lead to more serious harmonic pollution to the power grid.

4. Harmonic Current Mitigation Strategy

In order to reduce the harmonic currents injecting to the power grid, a feedforward harmonic mitigation strategy is investigated based on the results in Section 3. Its principle is to superimpose low-order harmonic signal into the PWM modulation wave, which can cut off the external incentive and internal transfer path of harmonic propagation, thus eliminating the lower-order harmonic current on ac side.

Aiming at Nth ($N = 3, 5, \ldots, 13$) harmonic currents on ac side, (4) can be simplified as

$$\left(R + jk\omega_s L\right)\left\langle I_R\right\rangle_N = -\sum_i \left\langle S_R\right\rangle_{N-i}\left\langle U_{\mathrm{dc}}\right\rangle_i + \left\langle U_s\right\rangle_N. \quad (15)$$

The harmonic currents on ac side are mainly induced by the grid voltage distortions and the internal interaction between the harmonic voltages on dc side just shown in Figure 3. The grid voltage distortions $\langle U_s\rangle_N$ are normally uncontrolled, mainly induced by other nonlinear loads. However, the ac voltage of SPVSC $\sum_i \langle S_R\rangle_{N-i}\langle U_{\mathrm{dc}}\rangle_i$ can be easily controlled by adjusting controller. It can be implied from (15) that $\langle S_R\rangle_N\langle U_{\mathrm{dc}}\rangle_0$ can be utilized to offset the harmonic currents generated by $\langle U_s\rangle_N$ and $\sum_{i\neq 0}\langle S_R\rangle_{N-i}\langle U_{\mathrm{dc}}\rangle_i$. If the right side of (15) is equal to 0, the internal interaction between the ac and dc side harmonics and external excitation from grid voltage distortions can be offset; thus the Nth harmonic current on ac side can be eliminated effectively.

From (6) and (8), the lower-order harmonic components $\langle \Delta S\rangle_N$ which should be superimposed on the PWM signal can be derived as follows:

$$\begin{aligned}&\langle \Delta S\rangle_N \\ &= \frac{\left(\left(\left\langle U_{\mathrm{st}}\right\rangle_1 - K_{\mathrm{iP}}\left(\left\langle I_{t\_\mathrm{ref}}\right\rangle_1 - \left\langle I_R\right\rangle_1\right)\right)/U_{\mathrm{dc\_ref}}\right)\left\langle u_{\mathrm{dc}}\right\rangle_{N-1} + \left(\left(\left\langle U_{\mathrm{st}}\right\rangle_1^* - K_{\mathrm{iP}}\left(\left\langle I_{t\_\mathrm{ref}}\right\rangle_1^* - \left\langle I_R\right\rangle_1^*\right)\right)/U_{\mathrm{dc\_ref}}\right)\left\langle u_{\mathrm{dc}}\right\rangle_{N+1} - \left\langle U_s\right\rangle_N\right)}{\left\langle u_{\mathrm{dc}}\right\rangle_0}.\end{aligned} \quad (16)$$

Above all, the feedforward compensation control strategy is implemented by superimposing lower-order harmonic components in the PWM signal to suppress the low-order harmonic currents on ac side. The control block diagram is shown in Figure 4. The harmonic voltage component on dc side and the background harmonic voltage on ac side are detected in real time. According to (16), the amplitude and phase angle of the Nth harmonic components needed to be superposed in the PWM signals are obtained, so as to suppress the harmonic current on ac side dynamically.

The harmonic mitigation strategy not only has clear physical meaning and fast calculation speed, but also will not be affected by the uncertainty of circuit parameters which can be seen from (16). Moreover, without additional controller, it avoids the complex parameter design and will not affect the stability of the system.

5. Simulation Results

In order to verify the correctness of the harmonic analysis model, a SPVSC model is set up in MATLAB/Simulink. The key parameters for the simulation model are listed in Table 1.

The control strategy is shown in Figure 2, which is voltage and circuit double closed-loop control. The simulation results and the theoretical results of the harmonic currents on ac side and the harmonic voltages on dc side are shown in Tables 2 and 3, respectively. The simulation results of the amplitude and angle of the harmonic currents on ac side and the harmonic voltages on dc side are well-matched with those obtained by the harmonic analysis model. There are a series of low-order odd harmonic currents on the ac side, in which the 3rd harmonic current is dominant. The amplitude decreases with the harmonic order increasing. There are series of low-order even harmonic voltages on dc side. The 2nd harmonic voltage is the most obvious. The harmonic content is obviously reduced with the increase of the harmonic order. Therefore, the correctness of the low-order harmonic analysis model of SPVSC with closed-loop control strategy is verified.

In order to verify the harmonic transmission law of SPVSC, injecting 3rd and 5th voltage background harmonics to power grid, respectively, the harmonic spectra of the ac side current and the dc side voltage are obtained, which is shown in Figure 5. The black bar represents the situation without background harmonic voltage. The red bar represents the situation with 3rd background harmonic voltage, and the blue bar represents the situation with 5th background harmonic voltage.

It can be seen that when the power grid contains 3rd background harmonic voltage, the third harmonic current on ac side increased significantly, and the 4th harmonic voltage on dc side also increased because of the interaction between the ac side and dc side. Simultaneously, it passes back to ac side and generates 5th harmonic current. But after the second transmission, the impact on 5th harmonic current is weak. Similarly, when the grid contains 5th background harmonics voltage, the 6th harmonic voltage on dc side increased because of the impact of 5th harmonic current on ac side. But when it is passed back to the 7th harmonic current

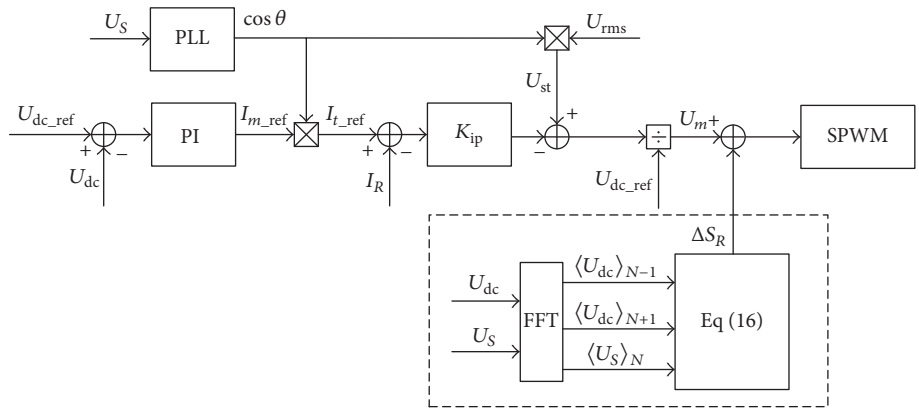


Figure 4: Control block diagram of injected N-order modulation wave.

Table 1: Simulation parameters.

Parameter	Meaning	Value
U_s	RMS of ac source voltage	220 V
R, L	Impedance of the ac system	0.02 Ω/3 mH
C_{dc}	Capacitor on dc side	3400 μF
R_{dc}	Load resistance	10 Ω
$V_{\text{dc\_ref}}$	Reference of dc voltage	428 V

Table 2: Comparison of theoretical results and simulation results of harmonic currents on ac side.

Frequency	Simulation result		Calculation result	
	Magnitude (A)	Angle (°)	Magnitude (A)	Angle (°)
50 Hz	124.43	2.7	124.61	2.5
150 Hz	1.65	221.4	1.69	230.2
250 Hz	0.11	118.8	0.08	116.6

Table 3: Comparison of theoretical results and simulation results of harmonic voltages on dc side.

Frequency	Simulation result		Calculation result	
	Magnitude (V)	Angle (°)	Magnitude (V)	Angle (°)
0 Hz	428.10	90.0	430.16	90.0
100 Hz	20.57	183.7	20.60	183.8
200 Hz	0.33	49.7	0.33	52.65

on ac side, the impact is weak. The harmonic transfer law shown in Figure 3 can be validated.

In order to verify the effectiveness of the feedforward harmonic mitigation strategy, the simulation is carried out and the dynamic compensation effect can be observed by changing the system conditions. Initially, the grid voltage has 0.1 pu 3rd and 0.05 pu 5th harmonic distortions. At 0.4 s, the feedforward harmonic mitigation strategy is employed and the low-order harmonic signals are superimposed to PWM modulated waves. At 0.5 s, the grid voltage changes suddenly, only containing 0.01 pu 5th background harmonic voltage. At 0.7 s, the grid voltage becomes undistorted, and the load resistance on dc side changes from 10 Ω to 6.67 Ω. At 0.9 s, the harmonic mitigation link is turned off. Figure 6 presents the harmonic injection component of PWM signals. Table 4 presents the harmonic currents on ac side before and after the harmonic mitigation strategy being employed.

Before the feedforward harmonic mitigation strategy is employed, there are a large number of 3rd and 5th harmonic currents on ac side, which amplitudes are 6.48 A and 2.85 A, respectively. When the harmonic mitigation strategy is employed, the harmonic is effectively suppressed and the amplitude decreased to 0.37 A and 0.09 A, respectively. At 0.5 s and 0.7 s, the background harmonic voltages in grid and load are changed abruptly, but the harmonic suppression is still effective. Moreover, low-order harmonic signal superimposing to PWM can quickly track the changes of system conditions, to suppress the harmonics current on ac side dynamically. Above all, the effectiveness of the harmonic mitigation strategy is verified.

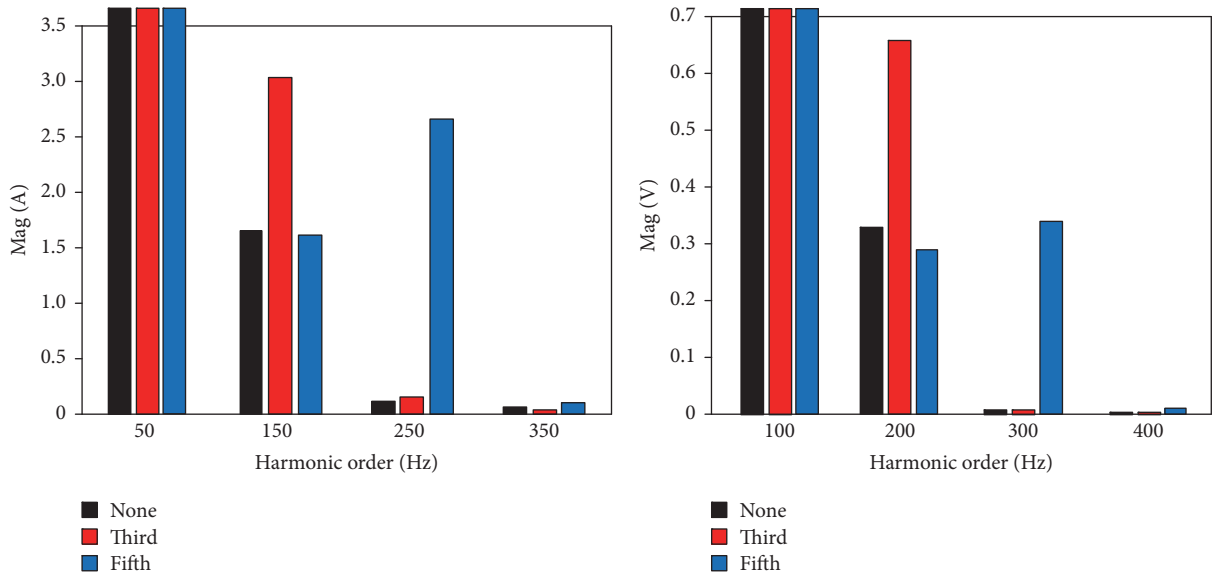
6. Experimental Results

The experimental setup of single-phase voltage source converter is shown in Figure 7. The inductance on the ac side is 6 mH. The capacitance and resistance on dc side are 3400 μF and 100 Ω. The carrier wave frequency is 7500 Hz. The converter uses the intelligent power module (IPM) and the controller uses DSP TMS320F28335. The control strategy is the same as simulation.

The grid voltage is used as the system voltage on ac side, in which RMS is 220 V. The measurement results show that the most obvious background harmonic voltage is 3rd, 5th, and 7th harmonic voltage, so the experiment mainly aims at 3rd, 5th, and 7th harmonic current to verify the effectiveness of the proposed suppression strategy. By inducing the harmonic component feedforward of the ac side voltage and the dc side voltage, the amplitude and phase angle of harmonic signal which needs to be superimposed in PWM modulation wave can be obtained by controller and applied to the converter. The Fluke 435 is used to measure the voltage and current wave on the ac side of SPVSC and analyze the spectrum characteristics of ac current. In this section, a comparison between multiresonant control strategy [14, 15] and the proposed

Table 4: The harmonic current on ac side before and after N-order modulated wave injection (A).

Harmonic order	0~0.4 s without	0.4~0.5 s with	0.5~0.7 s with	0.7~0.9 s with	0.9~1.1 s without
Fund	123.80	123.82	124.48	184.49	184.36
3rd	6.48	0.37	0.23	0.45	2.51
5th	2.85	0.09	0.07	0.11	0.23



(a) Spectrum of current on ac side

(b) Spectrum of voltages on dc side

Figure 5: The grid voltage contains third and fifth harmonic.

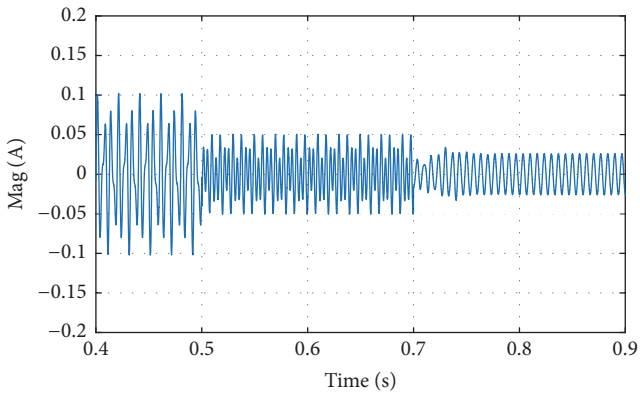


Figure 6: Harmonic injection component of PWM modulated wave.

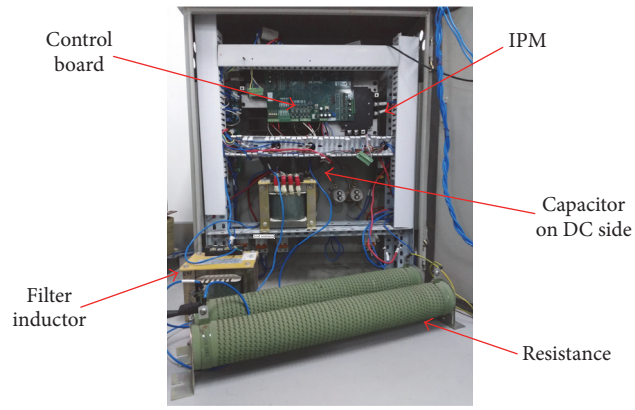
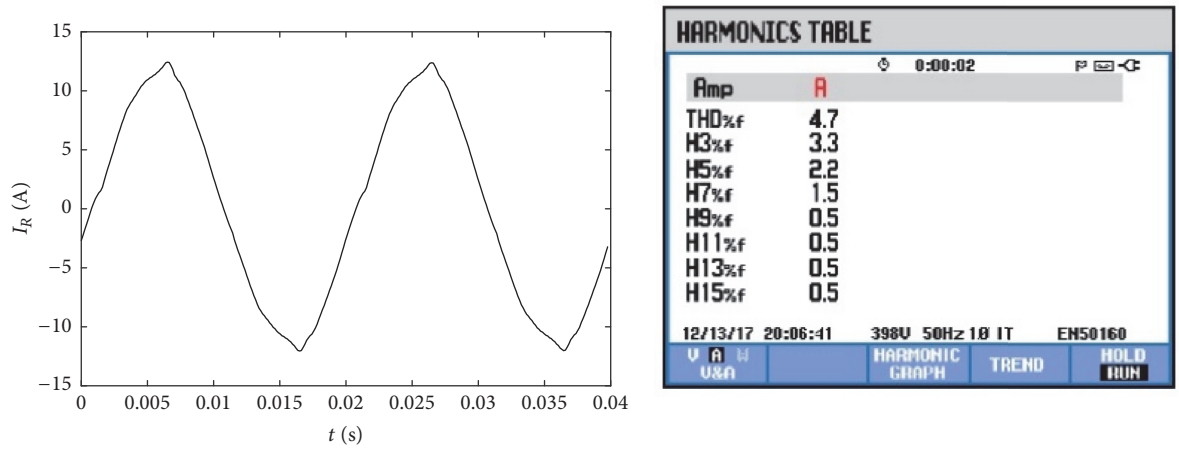


Figure 7: Experimental setup of single-phase voltage source converter.

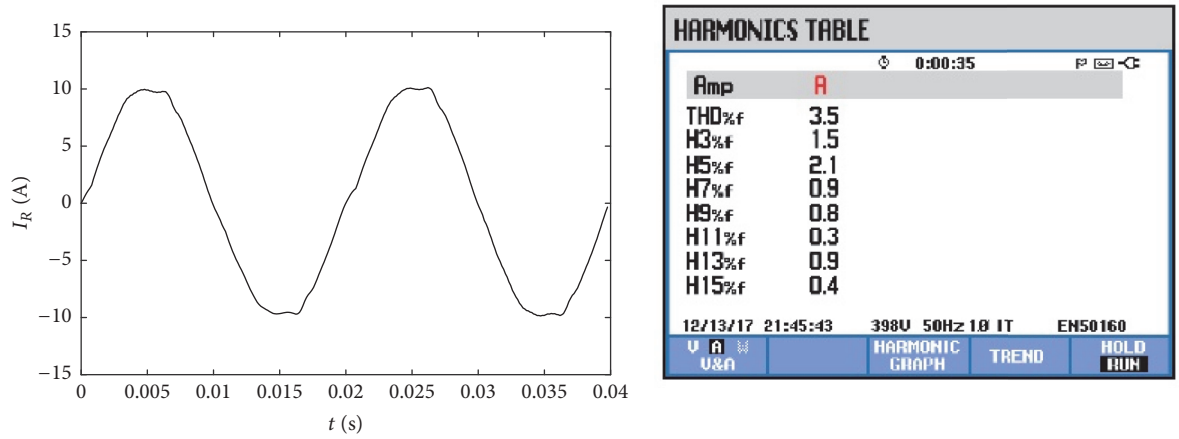
feedforward harmonic mitigation strategy is carried out. The waveforms and harmonics tables of current on ac side without harmonic mitigation strategy, with multiresonant control strategy and with the proposed strategy, are shown in Figures 8, 9, and 10, respectively.

From the experimental results, it can be found that after the multiresonant control strategy is employed, the total harmonic distortion of current (THDI) decreases from 4.7% to 3.5%, and the harmonic content of 3rd, 5th, and 7th current decreases from 3.3% to 1.5%, 2.2% to 2.1%, and 1.5% to 0.9%, respectively. However, after the feedforward harmonic mitigation strategy is employed, THDI decreases from 4.7% to 2.5%, and the harmonic content of 3rd, 5th, and 7th harmonic current decreases to 0.8%, 1.6%, and 1.1%, respectively. It is clearly shown that the proposed strategy has better performance than multiresonant control strategy, which has verified the effectiveness of the proposed harmonic



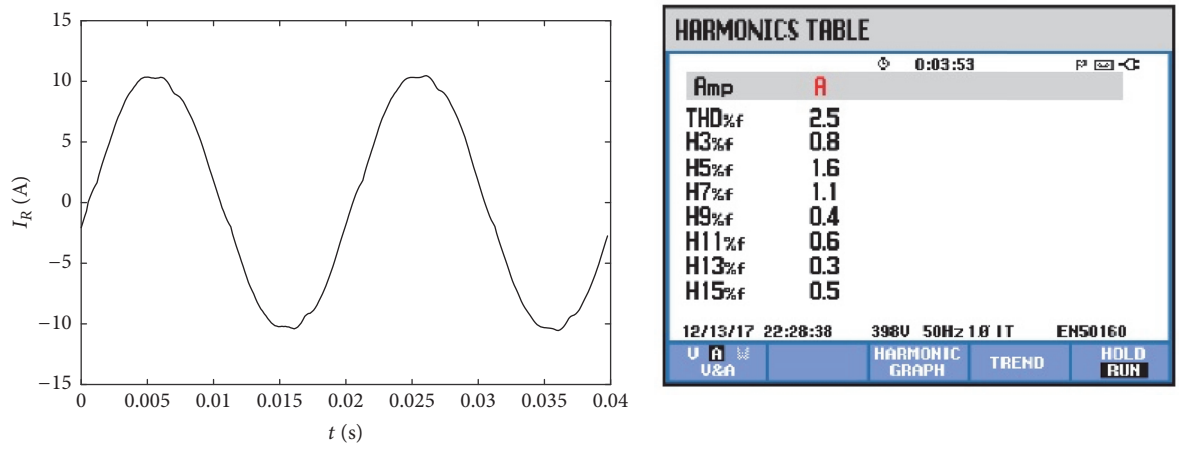
(a) Waveform (b) Harmonics table

Figure 8: Waveform and harmonics table of current on ac side without harmonic mitigation strategy.



(a) Waveform (b) Harmonics table

Figure 9: Waveform and harmonics table of current on ac side with multiresonant control strategy.



(a) Waveform (b) Harmonics table

Figure 10: Waveform and harmonics table of current on ac side with feedforward harmonic mitigation strategy.

mitigation strategy. However, because the theoretical analysis does not consider the effect of PWM dead zone and control delay, it cannot completely eliminate the harmonic current. At the same time, it can be explained that after the 3rd, 5th, and 7th harmonic signal are superimposed in the PWM modulation wave, the other order harmonics currents cannot be suppressed.

7. Conclusion

Based on the dynamic phasor method, a harmonic analysis model of SPVSC was established, which takes the controller into consideration. The proposed model is used as a tool to analyze the generation mechanism of harmonic as well as the harmonic interaction between the ac and dc side. The harmonic currents injecting to the grid from SPVSC can be mainly carried out in two ways: external excitation and internal interaction. With the internal interaction between ac and dc side, SPVSC generates series of low-order odd harmonic currents on ac side and series of low-order even harmonic voltages on dc side. With the external excitation, the distorted grid voltages will exacerbate the generation of harmonic currents on ac side. According to the generation mechanism, a feedforward control strategy was put forward to mitigate the harmonic currents from SPVSC which has clear physical meaning, fast calculation speed, and robustness. Meanwhile, it avoids the design of controller parameter and will not affect the stability of the system. Simulation and experimental results are finally presented to verify the proposed harmonic analyzed model and feedforward harmonic mitigation strategy.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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