Research Article

PLL Based Energy Efficient PV System with Fuzzy Logic Based Power Tracker for Smart Grid Applications

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This work aims at improving the dynamic performance of the available photovoltaic (PV) system and maximizing the power obtained from it by the use of cascaded converters with intelligent control techniques. Fuzzy logic based maximum power point technique is embedded on the first conversion stage to obtain the maximum power from the available PV array. The cascading of second converter is needed to maintain the terminal voltage at grid potential. The soft-switching region of three-stage converter is increased with the proposed phase-locked loop based control strategy. The proposed strategy leads to reduction in the ripple content, rating of components, and switching losses. The PV array is mathematically modeled and the system is simulated and the results are analyzed. The performance of the system is compared with the existing maximum power point tracking algorithms. The authors have endeavored to accomplish maximum power and improved reliability for the same insolation of the PV system. Hardware results of the system are also discussed to prove the validity of the simulation results.

1. Introduction

The steady increase in demand for power supply with overexploited decreasing conventional sources increases the necessity for alternative energy sources. Photovoltaic (PV) array, using solar energy as a source, is a better option as it provides a pollution-free, easily available, clean energy source [1]. For a smart grid application, PV array can be used as a source of energy in conjunction with the existing conventional source and wind energy. A photovoltaic system converts photon energy from sunlight into electricity. With PV panel prices dropping and the desire to “go green” expanding, demand for PV power is improving. As the efficiency of a PV array is much less, it becomes imperative to extract the maximum available power out of it. Various maximum power point tracking (MPPT) techniques are available to extract maximum power available from the solar energy [2–6]. According to maximum power transfer theorem, if the source impedance is equal to the load impedance, maximum energy can be transferred from the source to the load. The inclusion of DC-to-DC converter with MPPT technique varies the

equivalent impedance, thereby matching the load resistance to achieve maximum power transfer. The perturb and observe (P&O) method is the simplest method. Maximum power control is achieved by forcing the derivative of the power to be equal to zero under power feedback control [7, 8]. But this method produces oscillations closer to the maximum power point, thereby raising the response time. Incremental conductance (INC) process traces the maximum power by observing the conductance. It uses dI/dV and compares it with I/V , thereby adjusting the step size to track the maximum power point of PV array [9, 10]. Incremental resistance (INR) is similar to INC except that it compares dV/dI with V/I for tracking maximum power point [11]. Fuzzy logic control is an artificial intelligence technique which can be used to track the maximum power point to improve the performance of the system. As there is fuzziness in the input for PV array like change in insolation, temperature, and shading effect during the entire day, this logic is more suitable than the other methods for tracking maximum power point. In addition, this system does not require the knowledge

FIGURE 1: Block diagram of cascaded converter fed PV array connected to grid.

of the exact model [12–17]. To transmit the power at the required voltage and current level from the PV array to the load, boost converter is used [18]. The interleaved soft-switching boost converter (ISSBC) shares the input current all along each phase, thereby decreasing the current rating of the switching device. The ripple content present in the input current and the output voltage and the size of the passive components are also reduced in this converter [19, 20]. The problems caused due to EMI, switching loss, and diode recovery loss can be overcome by using the resonant soft-switching technique [21–24]. This technique does have certain limitations. The fidelity of the PWM signal to the analog input is determined by the linearity of the ramp-wave signal. The performance of the comparator determines speed, accuracy, and jitter. Phase-locked loops (PLLs) synchronize a local voltage-controlled oscillator (VCO) to an external frequency input by means of an electronic servo loop [25]. It is used with converter to achieve constant operating frequency over a wide output voltage range, eliminating the dependence of switching frequency on duty cycle or voltage conversion range [26].

In the present work, to improve the dynamic performance of the PV system, cascaded converter topology is used with intelligent power tracker and modified control strategy. The first conversion stage uses the fuzzy logic controller to track the maximum power. The simulation is performed for three algorithms in comparison with fuzzy based MPPT whereas in the literature comparison of fuzzy logic with any one algorithm is available. The phase-locked loop is used in the cascaded three-stage converter to extend the soft-switching region to minimize the losses. The interleaved soft-switching technique available in the literature is extended in the present work for three-stage converter for improved efficiency. In addition, the power handling capability is improved and the ripple content at the output is reduced.

The PLL control scheme prevents the operating frequency of the circuit from being lower than the resonant frequency. In this work, phase-locked loop is implemented to maintain the required frequency of operation with reduced ripple and to increase the soft-switching range of operation. The PV array was mathematically modeled using the basic equations to match the actual parameters of the nonlinear model. The performance of the system is compared with the other conventional algorithms. The simulation is performed using the Simulink software and the hardware results are found to be in line with the simulation results.

This paper is organized as follows. Section 2 presents system description. Mathematical model of solar PV module is discussed in Section 3. In Section 4, fuzzy logic based maximum power tracker used in the present work is discussed. Section 5 presents design of three-stage soft-switching boost converter. Section 6 describes the phase-locked loop for extending the soft-switching region. Section 7 deals with results and discussions. Finally, Section 8 summarizes the work done as conclusions.

2. System Description

Block diagrammatic representation of the PLL based energy efficient PV system with intelligent power tracker and cascaded converter is shown in Figure 1. The system consists of PV array acting as the source which converts light energy into electrical energy. In this work, both feedforward and feedback control are performed. Maximum power point tracking is performed as feedforward control by using fuzzy logic controller for the first converter in the cascaded network. Driving pulses to the switches are generated using the fuzzy based power tracking algorithm. Three-stage soft-switching boost converter (TSSSBC) is used for the second stage of cascaded converter to match the load requirements. Pulses for the

TABLE 1: Monocrystalline PV module specifications at standard test conditions.

Terms (unit)	Value
Open circuit Voltage (V)	21.4
Short circuit current (A)	6.4
Voltage at maximum power (V)	17.4
Current at maximum power (A)	5.75
Maximum power (Wp)	100
Tolerance (%)	+5
Maximum system voltage (V)	1000

FIGURE 2: Photovoltaic panel under testing.

TSSSC are 120° phase shifted from each other. A three-stage boost converter is designed, developed, and modified from a normal boost converter. As the number of stages in the boost converter is increased, the size of the inductor is reduced, so that it could be made compact and reduction in ripple content could also be achieved. The phase delay for each stage is given by $360/N$, where N is the number of stages. As the number of stages increases, the quality of regulated output increases, but, at the same time, the complexity of the circuit also increases. To ensure reduced complexity with reduced ripple content, a three-stage boost converter is used in the present work. To ensure accurate terminal voltage with lower ripple content, feedback control with phase-locked loop is proposed in the present work.

3. Mathematical Model of Solar PV Module

Use of equivalent circuits makes it possible to model the characteristics of a PV cell [27–29]. A single diode model for PV array is considered in this work. The model for PV panel is developed as per the specifications given in Table 1 and the same is considered for simulation using the MATLAB/Simulink package. The test setup of the PV panel is shown in Figure 2.

The basic equation that mathematically describes the I - V characteristics of an ideal PV cell is

$$I = I_{PV,cell} - I_D, \quad (1)$$

where $I_{PV,cell}$ is the current generated by the PV panel and I_D is the diode current. Substituting for I_D , we get

$$I = I_{PV} - I_0 \left[\exp \left(\frac{qV}{akT} \right) - 1 \right], \quad (2)$$

where I_0 is the reverse saturation current.

The basic equation does not represent the actual characteristic of the array and hence requires inclusion of additional parameters of equivalent series (R_s) and parallel resistance (R_p). Hence,

$$I = I_{PV} - I_0 \left[\exp \left(\frac{V + IR_s}{a \cdot V_t} \right) - 1 \right] - \left(\frac{V + I \cdot R_s}{R_p} \right), \quad (3)$$

where V_t is the thermal voltage.

The photon generated current is also influenced by the temperature according to the following equation:

$$I_{PV} = (I_{PV,n} + K_I \Delta T) \frac{G}{G_n}, \quad (4)$$

where $I_{PV,n}$ is the light generated current at nominal condition; $\Delta T = T - T_n$, where T and T_n are actual and nominal temperatures in kelvin; G is the irradiation on the panel; and G_n is the nominal irradiation. The diode saturation current I_0 is given by

$$I_0 = I_{0,n} \left(\frac{T_n}{T} \right)^3 \exp \left[\frac{qE_g}{ak} \left(\frac{1}{T_n} - \frac{1}{T} \right) \right], \quad (5)$$

where E_g is the energy gap and $I_{0,n}$ is the nominal saturation current:

$$I_{0,n} = \frac{I_{sc}}{\exp(V_{oc}/aV_{t,n}) - 1}, \quad (6)$$

with $V_{t,n}$ being the thermal voltage at T_n . The saturation current I_0 is further improved by including voltage and current coefficients:

$$I_0 = \frac{I_{sc} + K_I \Delta T}{\exp((V_{oc} + K_V \Delta T)/aV_t) - 1}, \quad (7)$$

where K_V and K_I are the voltage and the current coefficients, respectively. V and I are the terminal voltage and current. The relation between R_s and R_p is given by

$$R_p = \frac{V_{mp}(V_{mp} + I_{mp}R_s)}{V_{mp}I_{PV} - V_{mp}I_0 \exp \left[\left((V_{mp} + I_{mp}R_s)/N_s a \right) (q/kT) + V_{mp}I_0 - V_{mp}I_{mp} \right]}. \quad (8)$$

By using the above equations, the PV model is implemented with MATLAB using the Sim Power system block set.

4. Intelligent Maximum Power Tracker

A DC-DC boost converter is used in the first stage of circuit to boost the low voltage from PV array.

The first step in the design of this converter is to determine the duty ratio

$$D = 1 - \frac{V_{in(min)} \times \eta}{V_{out}} \quad (9)$$

The next step is to determine the ripple in the inductor current

$$\Delta I_L = \frac{V_{in(min)} \times D}{f_s \times L} \quad (10)$$

The maximum output current is

$$I_{maxout} = \left(I_{min} - \frac{\Delta I_L}{2} \right) \times (1 - D) \quad (11)$$

The maximum switch current is

$$I_{SW(max)} = \frac{\Delta I_L}{2} + \frac{I_{out(max)}}{1 - D} \quad (12)$$

The value of inductor is chosen based on the following equation:

$$L = \frac{V_{in} \times (V_{out} - V_{in})}{\Delta I_L \times f_s \times V_{out}} \quad (13)$$

The output capacitor value for a desired output voltage ripple is

$$C_{out(min)} = \frac{I_{out(max)} \times D}{f_s \times \Delta V_{out}} \quad (14)$$

To track the maximum power to be transferred from the PV array to the load, maximum power point tracking algorithm is embedded in the first conversion stage. The tracking algorithms are based on the principle that maximum power will be transferred to load when source impedance is equal to load impedance. Out of the many available algorithms, the artificial intelligence technique based FLC for maximum power tracking is considered in this work. Fuzzified natural behavior of change in the insolation level and partial shading effects due to sudden change in climate are considered in the proposed work. Hence, this method proves more advantageous than other methods. This technique can be applied to a system, even if the mathematical model of the system process is not defined for the input-process-output model. For the system under consideration, the fuzzy subsystem fits in deciding the duty ratio of the TSSSBC. To define the

control surfaces, each input variable and each output variable are decomposed into a set of fuzzy regions. The control variables considered in the fuzzy set that semantically shows the concept associated with it are error (e), change in error (Δe), and the solution variable being the control signal (Δd). Seven membership functions, PB, PM, PS, ZE, NS, NM, and NB, are used to describe them. The formula used to calculate the error (e) at k th instant is given by

$$e(k) = \frac{P(k) - P(k-1)}{V(k) - V(k-1)} \quad (15)$$

Change in error (Δe) is given by

$$\Delta e = e(k) - e(k-1) \quad (16)$$

Mamdani method was chosen for fuzzy inference. For fuzzification, triangular membership function is chosen for error (e), change in error (Δe), and control signal. For the case of the Positive Medium (PM), the membership function is

$$\mu^{PM}(u) = \begin{cases} \max \left\{ 0.1 + \frac{u - 0.5}{0.5} \right\}, & \text{if } u \leq 0.5, \\ \max \left\{ 0.1 + \frac{0.5 - u}{0.5} \right\}, & \text{otherwise.} \end{cases} \quad (17)$$

Similar equations are also defined for the rest of the input and output membership functions.

To define the behavior of control surfaces, rule base is framed.

Below is an example for the rule base framed.

Rule 1. IF error (e) is PB AND change in error (Δe) is PB THEN control signal is NB.

Thus, each entry in the table framed is a rule and there are 49 rules that form the knowledge repository of the fuzzy logic controller.

The flowchart for the proposed FLC controller is shown in Figure 3. Inputs were fuzzified in the fuzzification process and rule base is framed for this work to produce the required control signal. The centroid method of defuzzification which is the most prevalent and physically appealing of all the defuzzification methods is used to obtain the control signal to drive the pulse for the converter. The formula used is

$$z^* = \frac{\int \mu(z) \cdot z dz}{\int \mu(z) dz} \quad (18)$$

where z^* is the defuzzified value of duty ratio.

Defuzzified signal is the control signal used to vary the duty ratio to extract maximum power from array.

5. Design of Three-Stage Soft-Switching Boost Converter

Based on the working of single switch soft switching boost converter (SSSSBC), the three-stage soft switching boost

TABLE 2: Current and voltage equations of SSSSBC for various modes.

Modes	$i_L(t)$	$i_{L_r}(t)$	$V_{C_r}(t)$	$V_{C_a}(t)$
Mode 1	$i_L(t_0) - \frac{(V_0 - V_{in})}{L}t$	0	V_0	0
Mode 2	$i_1 - \frac{(V_0 - V_{in})}{L}t$	$\frac{V_0}{L_r}t$	V_0	0
Mode 3	I_{min}	0	$I_{min} + \frac{V_0}{Z_r} \sin \omega_r t$	$V_0 \cos \omega_r t$
Mode 4	$I_{min} + \frac{V_{in}}{L}t$	I_2	0	0
Mode 5	I_{max}	$I_2 \cos \omega_a t$	$\frac{I_2}{C_a}$	$Z_r I_2 \sin \omega_a t$
Mode 6	$I_3 - \left(\frac{V_0 - V_{in}}{L}\right) * t$	$I_2 \cos \omega_a t$	V_0	$Z_r I_2 \sin \omega_a t$
Mode 7	$I_3 - \left(\frac{V_0 - V_{in}}{L}\right) * t$	$\left(\frac{V_0}{Z_a} - I_2\right) \sin \omega_a t$	V_0	V_2
Mode 8	$I_4 + \left(\frac{V_0 - V_{in}}{L}\right) * t$	$I_s - \left(\frac{V_0}{L_r}\right) * t$	V_0	0

FIGURE 3: Flowchart of fuzzy logic based power tracker.

converter (TSSSBC) has been developed and analyzed with eight modes [20]. Figure 4 shows the equivalent circuit diagram for various modes of operation of SSSSBC. For TSSSBC, the same is applicable with a phase shift of 120° for

the MOSFET gate pulse in each arm. The formulae for $i_L(t)$, $i_{L_r}(t)$, $V_{C_r}(t)$, and $V_{C_a}(t)$ during various modes of operation are summarized in Table 2.

The circuit diagram for three-stage soft-switching boost converter (TSSSBC) is shown in Figure 5. In the proposed TSSSBC, the three main inductors (L_1 , L_2 , and L_3) and resonant inductors (L_{r1} , L_{r2} , and L_{r3}) of reduced magnitudes ($1/3$ rd of the original values) are considered. Driving pulses for the three switches were phase shifted by 120° .

By introducing soft-switching technique, the switching loss is minimized. Hence, the total loss is minimized with the TSSSBC.

6. Phase-Locked Loop

Block diagram of the phase-locked loop (PLL) considered in this work to enhance the performance of the system under consideration is shown in Figure 6.

A PLL is a closed-loop feedback structure that sets fixed phase relationship between its output phase and the phase of a reference. It tracks the phase changes that are within the bandwidth of the PLL.

A PLL comprises several components, namely, phase or phase-frequency detector, charge-pump current, loop filter, voltage-controlled oscillator, and frequency divider.

The open-loop transfer function can be written as

$$H_{open}(s) = K_{PFD} \cdot \frac{I_{CP}}{2\pi} \cdot F(s) \frac{K_{VCO}}{s}, \quad (19)$$

where K_{PFD} is the phase-frequency detector gain, $F(s)$ is the loop filter transfer function, and K_{VCO} is the transfer gain of the VCO. The closed-loop transfer function from the input

FIGURE 4: Equivalent circuit diagram of SSSBC for various modes of operation.

phase to the output phase is a low-pass filter. This low-pass behavior of a PLL is desirable because it rejects input noise frequencies higher than the PLL bandwidth. Similarly, the closed-loop transfer function from the VCO control voltage, V_{ctrl} , to the output phase is a bandpass filter. It rejects internal noise coupled into V_{ctrl} within the PLL bandwidth. Filtering out noise sources by the closed-loop behavior of the PLL forms the baseline for jitter analysis. Noise of the PLL's output clock can be optimally filtered by adjusting the loop bandwidth and peaking in frequency response based on the dominant noise source. The loop bandwidth and peaking are adjustable by varying loop parameters. Natural frequency is proportional to square-root of the loop gain. Damping factor is inversely proportional to zero frequency. By adjusting the zero frequency through the loop filter resistor, R , and charge-pump current, ζ and ωn can be adjusted. To further improve

the noise performance, the loop parameters of a PLL should be tuned for minimum output jitter in real system noise conditions.

7. Results and Discussions

The developed cascaded converter is simulated using MATLAB/Simulink software package. The subsystem for mathematical model for PV array derived from the equations used in the Simulink model is shown in Figure 7. Simulink model for fuzzy logic controller based boost converter is shown in Figure 8. Figure 9 shows the error block associated with the system.

The fuzzy logic considered in this work is feedforward network (not feedback from load).

FIGURE 5: Circuit diagram for three-stage soft-switching boost converter.

FIGURE 6: Block diagram of phase-locked loop.

Voltage and current signal sensed from PV array are given as input to filter block and it is sampled. By using multiplier for voltage and current, power is calculated and thereby error and change in error can be calculated using the formulae

$$e(k) = \frac{P(k) - P(k-1)}{V(k) - V(k-1)}, \quad (20)$$

$$\Delta e = e(k) - e(k-1).$$

These two signals are multiplexed and given as input to fuzzy logic block. Fuzzy rule base controls the duty ratio against the variations in error and change in error.

The control variables considered in the fuzzy set that semantically shows the concept associated with it are error (e), change in error (Δe), and the solution variable being the control signal. The membership functions for error (e),

TABLE 3: Rule base for FLC.

e	Δe						
	NB	NM	NS	ZE	PS	PM	PB
NB	PB	PB	PB	PM	PM	PM	PS
NM	PB	PB	PM	PM	PM	PS	ZE
NS	PB	PB	PM	PM	PS	PS	ZE
ZE	PB	PM	PS	ZE	ZE	ZE	NS
PS	PM	PM	PS	PS	ZE	S	NS
PM	PM	PM	PS	ZE	NS	NS	NM
PB	PS	PS	ZE	NS	NM	NM	NB

change in error (Δe), and control signals are shown in Figure 10.

In the proposed design, the universe of discourse for first input, error (e) is assigned in terms of seven linguistic variables which are denoted by NB, NM, NS, ZE, PS, PM, and PB. The membership functions for the variable are shown in Figure 10(a). Figure 10(b) shows the universe of discourse for the second input variable change in error (Δe) which is classified into seven fuzzy sets similar to error. Figure 10(c) shows the control surface of the output variable control signal.

Triangular membership is chosen for both inputs and outputs. The range of values chosen for e , Δe , and control signal is $(-20, 20)$, $(-2, 2)$, and $(-0.3, 0.3)$, respectively, based on trial and error. The control signal is added with the reference signal with limits bounded and compared with a ramp signal of desired frequency of operation. The surface viewer is shown in Figure 11. Rule base considered in this work is shown in Table 3.

FIGURE 7: Subsystem for PV array.

In the second stage of the cascaded converter, three-stage soft-switching boost converter is used. The values of the

inductor and the capacitor for auxiliary resonant circuit of TSSBC are chosen so as to design the resonant frequency to be less than the switching frequency. The main inductor rating is 33% of the actual inductor rating used in a single-stage boost converter. The boost converter, interleaved boost converter, and the three-stage boost converter are simulated for the same input voltage and switching frequency and the performances of the three converters were compared and the results are tabulated in Table 5. The comparison with graphical representation is shown in Figure 14. From the tabulated results, it is clear that the ripple content with the three-stage converter is reduced to a greater extent with respect to the single-stage and the interleaved converter for duty ratios from 10% to 90%. In this way, the three-stage boost converter becomes superior to the other ones. A small

FIGURE 9: Subsystem of error block.

FIGURE 10: (a) Membership functions of error. (b) Change in error. (c) Control signal.

TABLE 4: Performance parameters of different algorithms.

Input power (W)	Rise time (s)			Settling time			Output power			Ripple			Efficiency				
	p&O	INC	INR	Fuzzy	P&O	INC	INR	Fuzzy	P&O	INC	INR	Fuzzy	P&O	INC	INR		
100	0.54	0.52	0.48	0.42	0.56	0.54	0.49	0.43	91.22	93.43	95.95	97.35	4.5	3.17	4.5	96	97.35
200	0.73	0.7	0.68	0.66	0.76	0.72	0.71	0.67	182	186.2	189.4	191.6	5.2	5.05	5.2	93.1	95.8
300	1.32	1.22	1.2	0.95	1.35	1.25	1.23	0.96	270.75	278.1	282	289.2	6.22	5.9	5.7	94.4	95.3
400	1.53	1.47	1.43	1.2	1.55	1.48	1.44	1.22	360.4	368.4	376	378.4	7.3	6.9	6.5	92.1	94.6
500	1.72	1.64	1.63	1.5	1.76	1.67	1.64	1.54	447.7	453.5	467.5	475.5	8.1	7.7	7.2	93	94.1

TABLE 5: Comparison of single, interleaved, and three-stage converters.

	V_0	I_s	I_0	P_s	P_0	ΔV_0	ΔI_s	ΔI_0	ΔP_s	ΔP_0	Power loss	Efficiency
Single-stage												
10%	21.41	1.04	0.93	20.78	19.93	0.08	0.02	0.00	0.33	0.15	0.85	95.91
20%	24.16	1.32	1.05	26.47	25.38	0.18	0.00	0.01	0.66	0.38	1.08	95.91
30%	27.69	1.74	1.20	34.74	33.34	0.31	0.05	0.01	0.99	0.75	1.40	95.96
40%	32.37	2.37	1.41	47.44	45.55	0.48	0.07	0.02	1.32	1.36	1.89	96.02
50%	38.85	3.42	1.69	68.35	65.62	0.72	0.08	0.03	1.64	2.43	2.73	96.01
60%	48.39	5.32	2.10	106.36	101.81	1.07	0.10	0.05	1.95	4.51	4.55	95.72
70%	63.67	93.16	2.77	186.33	176.29	1.63	0.11	0.07	2.22	9.06	10.04	94.61
80%	91.18	19.96	3.96	399.28	361.51	2.67	0.12	0.12	2.40	21.14	37.76	90.54
90%	142.95	62.39	6.22	1247.89	888.70	4.68	0.10	0.20	2.06	58.20	359.19	71.22
Two-stage												
10%	21.38	1.04	0.93	20.88	19.94	0.10	0.03	0.001	0.59	0.07	0.94	95.51
20%	24.18	1.33	1.05	26.69	25.42	0.07	0.05	0.001	1.00	0.15	1.27	95.24
30%	27.73	1.76	1.21	35.14	33.43	0.09	0.06	0.001	1.14	0.22	1.71	95.14
40%	32.45	2.41	1.41	48.10	45.78	0.08	0.04	0.001	0.88	0.23	2.32	95.17
50%	39.02	3.47	1.70	69.46	66.19	0.01	0.00	0.001	0.00	0.02	3.26	95.30
60%	48.78	5.42	2.12	108.43	103.45	0.18	0.07	0.01	1.32	0.78	4.97	95.41
70%	64.73	9.56	2.81	191.29	182.19	0.48	0.13	0.02	2.60	2.71	9.10	95.24
80%	94.98	20.95	4.13	419.04	392.24	1.05	0.19	0.05	3.79	8.68	26.80	93.60
90%	166.48	72.96	7.23	1458.08	1202.82	2.11	0.22	0.11	4.36	35.18	255.26	82.49
Three-stage												
10%	21.42	1.05	0.93	20.97	19.94	0.02	0.04	0.001	0.78	0.04	1.03	95.09
20%	24.19	1.35	1.05	26.90	25.43	0.03	0.05	0.001	1.00	0.07	1.47	94.54
30%	27.74	1.78	1.21	35.50	33.46	0.02	0.02	0.001	0.43	0.04	2.04	94.24
40%	32.47	2.43	1.41	48.67	45.85	0.04	0.04	0.001	0.89	0.11	2.83	94.20
50%	39.08	3.52	1.70	70.36	66.39	0.08	0.08	0.001	1.66	0.29	3.97	94.35
60%	48.92	5.50	2.13	109.93	104.03	0.08	0.07	0.001	1.32	0.35	5.90	94.63
70%	65.09	9.71	2.83	194.22	184.26	0.08	0.05	0.001	0.98	0.46	9.97	94.87
80%	96.32	21.40	4.19	428.07	403.36	0.48	0.19	0.02	3.86	4.01	24.71	94.23
90%	175.91	77.43	7.65	1548.52	1345.42	1.51	0.30	0.07	6.10	23.06	203.10	86.88

FIGURE 11: Surface viewer for FLC.

reduction in efficiency for low duty cycle is due to increased devices and hence increased switching losses for the

three-stage converter. Hence, efforts are made to introduce soft-switching technique to the three-stage boost converter to minimize the losses and to improve the performance of the system.

The simulated circuit of TSSSBC using Simulink software is shown in Figure 15 and the simulated results are shown in Figure 16. The driving pulses are obtained with 120° phase shift, as shown in Figure 16(a). Figures 16(b) and 16(c) show the main inductor current and the resonant inductor current, respectively. The switching losses are minimized by means of soft-switching technique. In Figure 16(d), the circle pointed out denotes the zero current and zero voltage switching achieved by the converter. Hence, reduction in power loss could be achieved with the proposed topology. The increase in efficiency due to TSSSBC in comparison with simple three-stage boost converter is shown in Table 6.

FIGURE 12: (a) Simulation result of fuzzy based system in comparison with perturb and observe (P&O), incremental conductance (INC), and incremental resistance (INR) method. (b) Zoomed view. (c) Voltage waveform. (d) Current waveform.

FIGURE 13: Comparison of performance parameters of different algorithms with respect to (a) rise time, (b) output power, (c) efficiency, and (d) output ripple.

FIGURE 14: Continued.

FIGURE 14: Comparison of performance parameters of single, interleaved, and three-stage converters for varying duty ratio.

FIGURE 15: Simulation circuit of three-stage soft-switching boost converter.

TABLE 6: Comparison of three-stage converter and TSSSBC.

Sl. number	Duty ratio	Efficiency of three-stage converter	Efficiency of the proposed TSSSBC
1	10%	95.09	96.43
3	30%	94.24	95.03
5	50%	94.35	95.01
7	70%	94.87	95.74
8	80%	94.23	95.02

TABLE 7: Specifications of the components.

Parameters	Symbol	Value	Unit
Main inductor	L_1, L_2, L_3	187.6	μH
Resonant inductor	L_{r1}, L_{r2}	6	μH
Auxiliary capacitor	C_{a1}, C_{a2}, C_{a3}	15.5	nF
Resonant capacitor	C_{r1}, C_{r2}, C_{r3}	405	nF
Output capacitor	C_o	10	μF

The specification of active and passive elements used in this work based on the design equation is tabulated in Table 7.

The simulation circuit of TSSSBC with embedded phase-locked loop for smart grid application is shown in Figure 17. The PLL consists of phase detector, VCO, and loop filter. The waveforms corresponding to switch parameters for various duty ratios are obtained through simulation with the proposed strategy and the conventional circuit without PLL is

shown in Figure 18. It clearly depicts that the soft-switching condition exists for the duty ratio range of 0.30 to 0.84 with the proposed system. In the conventional system without PLL, the soft-switching condition occurs only within the duty ratio of 0.30 to 0.72. By including the PLL, the power quality of the system is also improved due to reduced ripple contents.

The hardware setup is shown in Figure 19 and the layout diagram for the three-stage soft-switching converter is shown in Figure 20.

FIGURE 16: Voltage and current waveforms of TSSSBC. (a) Driving pulses. (b) Main inductors current. (c) Resonant inductors current. (d) Voltage and current through the switch.

FIGURE 17: Simulink diagram of TSSSBC with PLL.

The PV array is kept at the top floor of the main block. PIC microcontroller 16F84A is used to generate the driving pulses. IR2110 driver IC is used to provide the input at given rating for power MOSFET IRF840. Three resonant inductors and three main inductors along with capacitors form the resonant part in the converter unit. The size of the components is reduced as shown in Figure 19 due to three stages. Figure 21 shows the

waveform obtained from cascaded converter. Input voltage of 18.9 V is applied to the converter by the PV array during noon time. Output voltage of 45.98 V is obtained across the load.

Voltage and current through the switch are shown in Figure 21(a). Figure 21(b) shows the 120° phase shift between the switching patterns of TSSSBC.

FIGURE 18: Simulink waveform for different duty ratio.

FIGURE 19: Hardware setup for TSSSBC.

FIGURE 20: Hardware layout diagram.

FIGURE 21: Experimental results of TSSSBC. (a) Voltage across the switch. (b) Pulses for TSSSBC (120° apart).

8. Conclusions

The cascaded converters with intelligent control techniques are developed to track the maximum power from the photovoltaic (PV) system. Mathematical model of PV array is developed and the same is used for simulation. Sizes of the passive components in the converter are reduced by 33% and the power loss is minimized by adapting the soft-switching technique. The developed model is efficiently used for tracking the maximum power using FLC. The ripple content is minimized and the soft-switching region is increased by embedding PLL. With this arrangement, better transient response is achieved and efficiency of 97.35% is obtained. The experimental verification is done using PIC 16F84A and its results are analyzed. Experimental results are found to be in line with the simulation results. This work can be extended by considering the Genetic Algorithm or particle swarm optimization technique so that the Global Maxima can be obtained for the partial shading condition.

Competing Interests

The authors declare that there are no competing interests regarding the publication of this paper.

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