Guest Editorial

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It is my great pleasure to announce our long awaited next *Special Issue* on *VLSI Testing* we have been contemplating for quite sometime. We have been able to accommodate *nine* manuscripts in this *special issue*, and again all from recognized experts in the field of *VLSI* testing. Our first manuscript of the issue is by Jone *et al.* and discusses a novel approach, called *PGEN*, to generate test patterns for *resettable* or *non-resettable* synchronous sequential circuits. *PGEN* uses two major routines: Sequential *PODEM* or *S-PODEM* and differential fault simulator. For a given fault, *S-PODEM* utilizes the concept of multiple time compression supported by a pulsating model, and generates a test vector in a single, yet compressed, time frame. Logic simulation included in *S-PODEM* is next invoked to expand the *single* test vector into a test *sequence*. The test vector generation methodology and logic simulation are well coordinated to significantly facilitate test generation problem in sequential circuits. The authors also implemented a *modified* version of differential fault simulator for inclusion in *PGEN* to cover other faults detected by the expanded test sequence. Simulation studies were conducted and the results look promising. Our next manuscript by Majhi *et al.* presents a novel path delay simulator for combinational circuits capable of detecting both *robust* and *nonrobust* paths. The authors use binary logic rather than multiple-valued logic as commonly used in existing simulators to re-

duce the overall complexity of their algorithm. A rule-based approach is developed which identifies *all* robust and nonrobust paths testable by a two-pattern test, while backtracing from the primary outputs to the inputs in a depth-first manner. Rules are developed to find probable glitches and to determine how they propagate through the circuit. The authors also give experimental results on several *ISCAS* benchmark circuits to demonstrate the efficiency of the algorithm. The third manuscript by Kim and Saluja proposes a hybrid fault simulator, called *HYSIM*, for synchronous sequential circuits. The authors identify the inefficiencies of the *critical processes* in concurrent fault simulation and discuss systematic methods to remove such inefficiencies. They also consider dynamic memory usage reduction strategies for concurrent fault simulators. *HYSIM* maintains reduced fault lists yielding shorter processing time and improved dynamic storage. Besides, it employs *Release-and-Reconstruct* method for fault list construction that also helps in achieving better efficiency, as demonstrated by the experimental results provided in the manuscript on *ISCAS* benchmark circuits.

Our fourth manuscript in the issue is by Edirisooriya and examines aliasing probability in Multiple-Input Shift Registers or *MISRs* and a class of linear cellular automata (called *group* cellular automata) signature analyzers under the *q*-ary symmetric error model. By modeling the signature analyzer as a

Markov process, the author shows that the *closed form* expression derived for aliasing probability by Pradhan *et al.* in MISRs with primitive polynomials holds for all MISRs irrespective of their feedback polynomials as well as for class of cellular automata (known as *group* cellular automata) signature analyzers. For q-ary symmetric errors, the author also demonstrates that the circuit complexity and propagation delay can be minimized by using a set of m single bit LFSRs without increasing aliasing probability, and further, leading to a *regular* register structure. The fifth manuscript by Srinivas and Patnaik discusses a genetic algorithm based approach for determining the optimal input signal probabilities for *random* tests. A cost function based on the COP testability measure to determine the efficacy of the input distributions is defined, and implementation details with overview of genetic algorithms or GAs are provided. Experimental results based on ISCAS benchmark circuits are also given. The authors compare the performance of their approach with earlier ones as well and conclude that while GA generates more efficient signal probabilities, the overheads of GA in computing the signal probabilities are larger. The authors analyze in the manuscript the landscape of the COP-based cost function to account for the relatively quick convergence and prove that the cost function is *unimodal* in the search space which makes it amenable to optimization by gradient descent techniques. The sixth manuscript by Vandris and Sobelman proposes a new switch-level fault simulation method for MOS circuits combining concepts of compiled switch-level simulation and functional fault modeling of transistor faults based on differential fault simulation. The simulator models both node *s-a-0*, *s-a-1* faults and transistor *stuck-on*, *stuck-open* faults. The switch-level circuit components are first compiled into functional models and then every compiled circuit component is assigned a dominance *attribute* which abstracts relative strength information in the circuit. Dominance is used during simulation to resolve the X-state due to fighting pull-up and pull-down transistor paths and to deduce transistor fault detectability and fault equivalence. The differential fault simulator as claimed provides excellent performance with minimum storage, though it incurs a high overhead at the switch-level

than at the gate-level due to the dynamic memory properties of MOS circuits.

The next manuscript of our issue is by Menon *et al.* and considers fault modeling of ECL for high fault coverage of physical defects. The authors examine the behavior of simple and complex ECL gates in the presence of physical faults and assess the effectiveness of the classical *stuck-fault* model in representing their physical failures. The conventional *stuck-fault* model is then shown to be inappropriate in representing a majority of circuit level faults. The authors propose a new augmented *stuck-fault* model which provides significantly higher coverage of physical failures, and is also applicable to other logic families that use logic gates with both *true* and *complementary* outputs. A design for testability approach is suggested as well for *on-line* detection of certain error conditions in ECL devices. The eighth manuscript by Basu *et al.* presents a modified approach to test plan generation for BILBO test methodology. Though the approach was implemented for the general case of n -port combinational logic blocks or CLBs, only 2-port CLBs are actually discussed. The problem in this particular case is modeled as a Step Scheduling Matrix and an algorithm is also given for the solution. The algorithm was tested on a number of benchmark circuits and the results were compared with those obtained through existing methods. The effectiveness of the proposed approach in terms of total testing time and in the number of test plans generated looks encouraging. The final manuscript of the *special issue* is by Bandyopadhyay *et al.* and proposes methodology for testing arbitrary bilateral bit-level systolic arrays. The controllability and observability issues in bilateral bit-level systolic arrays are considered and a test procedure given on *partitioning* a given array into several *identical* subarrays, applying repetitive test patterns and propagating test outcomes to the observable extremities, ensuring in the process that every cell in the array is tested by a *minimal* test sequence. The authors also discuss set of sufficient conditions for an arbitrary bilateral bit-level systolic array to be tested for single faults.

In concluding this editorial I would like to express my sincerest gratitude to those of my friends and professional colleagues who helped me in so many ways

to bring this endeavor to a grand success. First amongst all is Professor George W. Zobrist, the *Editor-in-Chief* of the Journal, who has been a constant source of encouragement, help, and guidance during the long months starting from the very planning to the completion of this enormous task. His immense help and esteemed guidance came as always whenever and in whatever form they were solicited. Without him and his neverending patience this dream of our next *special issue* would probably have never been materialized. He has been simply wonderful! My grateful thanks are also due to those people behind the scene—those *anonymous reviewers*—whose selfless, dedicated, and timely professional helps contributed to the superb quality and content of this *special issue*.

Finally, my special thanks go to my colleagues and many other staff members both here at the Department of Electrical Engineering, University of Ottawa, Ottawa, Ontario, Canada, and at the Center for Reliable Computing, Department of Electrical Engineering, Stanford University, Stanford, CA for providing me all the support, both moral and material, that I needed in the days while the *preparation* of this *special issue* and other ones were in progress.

Guest Editor's Biography

Sunil R. Das is a Professor of Electrical Engineering at the University of Ottawa, Ottawa, Ontario, Canada. He holds a B.Sc. (Honors) in Physics and an M.Sc. (Tech) and a Ph.D. in Radiophysics and Electronics from the University of Calcutta, Calcutta, West Bengal, India. He previously held academic positions with the Center for Reliable Computing, Computer Systems Laboratory, Department of Electrical Engineering, Stanford University, Stanford, CA (*on sabbatical leave*), the Institute of Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan, Republic of China, and the Center of Advanced Study, Institute of Radiophysics and Electronics, University of Calcutta.

Dr Das published extensively in the areas of switching and automata theory, digital logic design, fault-tolerant computing, microprogramming, com-

puter architecture, graph theory, and combinatorics. He served in the Technical Program Committees and Organizing Committees of many International Conferences, Symposia, and Workshops, and also acted as *session organizer*, *session chair*, and *panelist*.

Dr Das was elected one of the delegates of the *GOOD PEOPLE, GOOD DEEDS* of the Republic of China in 1981 in recognition of his outstanding contributions in the field of research and education. He is listed in the *MARQUIS WHO'S WHO Biographical Directory of the Computer Graphics Industry*, Chicago, IL (First Edition, 1984).

Dr Das is presently the *Managing Editor* of the *IEEE VLSI Technical Bulletin*, a publication of the IEEE Computer Society *Technical Committee (TC) on VLSI*, an *Executive Committee Member* of the IEEE Computer Society *Technical Committee (TC) on VLSI*, an *Associate Editor* of the *IEEE Transactions on Systems, Man, and Cybernetics*, an *Administrative Committee (ADCOM) Member* of the *IEEE Systems, Man, and Cybernetics Society*, an *Associate Editor* of the *SIGDA Newsletter*, the quarterly publication of the *ACM Special Interest Group on Design Automation*, and a *Member* of the *Editorial Board* and a *Regional Editor* for Canada of the *VLSI Design* published by Gordon and Breach Science Publishers, NY. He was the former *Associate Editor* of the *International Journal of Computer Aided VLSI Design* published by Ablex Publishing Corporation, Norwood, NJ, an *Associate Guest Editor* of the *IEEE Journal of Solid-State Circuits Special Issues on Microelectronic Systems (Third and Fourth Special Issues)*, and *Guest Editor* of the *International Journal of Computer Aided VLSI Design* (September 1991) as well as *VLSI Design* (March 1993) *Special Issues on VLSI Testing*. He edited jointly with P. K. Srimani a book entitled *Distributed Mutual Exclusion Algorithms* published by the IEEE Computer Society Press, Los Alamitos, CA 1992 in its *Technology Series*, and is the author jointly with C. L. Sheng of a text on *Digital Logic Design* published by Ablex Publishing Corporation. He is also the *Co-Chair* of the IEEE Computer Society (*IEEE-CS*) *Student Activities Committee* from Region 7 (Canada).

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