

Design of an ASIC Chip for Skeletonization of Graylevel Digital Images

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This paper describes the design of an ASIC chip for thinning of graylevel images. The chip implements a Min-Max skeletonization algorithm and is based on a pipeline architecture where each stage of the pipeline performs masking operations on the graylevel images. The chip operates in real time at a frequency of 8 MHz and utilizes about 321 mils \times 410 mils of silicon area.

Key Words: ASIC, VLSI Design, Image Processing, Skeletonization, Image Thinning

1 INTRODUCTION

There has been a recent trend to develop special architectures for image processing which exploit the inherent parallelism found both in image data and in image processing algorithms. Unless this parallelism is suitably exploited, the sheer number of operations to be performed per second for even low level image processing tasks precludes economic real time processing with currently available processing speeds. It is, therefore, desirable to produce compact, high performance image processors that can execute basic image processing functions needed in different applications in real time. By operating in real time, it is possible to utilize all available data and hence achieve the highest possible throughput and, in addition, the need for external buffer memories, which add to system complexity, cost and size, is avoided. Although several such VLSI ASIC chips have been developed [1-4] for implementing various image processing operations, none has so far been reported for thinning or skeletonization of a digital image.

Thinning procedures play a central role in a broad range of problems in image processing. Before an object is recognized, it is necessary to process the input image and identify the required features. In low level image processing operations commonly employed, thinning of

the input image helps in clearly identifying the image boundary.

The skeleton of a region may be defined via the medial axis transformation [5]. The so called MAT of a region R with border B may be described as follows. For each point p in R, we find its closest neighbour in B. If p has more than one such neighbours, then it is said to belong to the medial axis of R. Although the MAT of a region yields an intuitively pleasing skeleton, a direct implementation of the above definition is generally prohibitive from the computational point of view because it potentially involves calculating the distance from every interior point to every point on the boundary of a region. A number of algorithms have been proposed for improving the computational efficiency while at the same time producing a medial axis representation of a given region.

Typically, most thinning algorithms iteratively delete edge points of a region subject to the constraints that the deletion of these points does not (i) delete end points, (ii) break connectedness and (iii) cause excessive erosion of the region. These algorithms can be broadly classified into two groups. The first group of algorithms operate on binary images only. Hence a graylevel image must be first converted into an equivalent binary image by suitable selection of thresholds before these algorithms are applied. The second group of algorithms have been

designed for finding the skeleton directly from the gray level images. The latter have the advantage that thinning of the image can be performed without the need for thresholding.

In the present paper an ASIC design for skeletonization of digital images on a single VLSI chip is described. The reported design is based on a Min-Max graylevel skeletonization algorithm developed by Goetcherian [6], which belong to the first category mentioned above. The selection of the algorithm has been prompted by its usefulness in keeping the hardware complexity of the chip fairly low.

2 MIN-MAX SKELETONIZATION

Goetcherian [6] has shown that many algorithms developed for binary images can be adopted for use with graylevel images by substituting MIN and MAX functions for AND and OR functions and by treating the logical inverse of a binary image as being equivalent in graylevel images to one (the maximum gray value) minus the image. In the present work, Goetcherian's technique has been applied to a skeletonization algorithm developed by Arcelli et al [7] for thinning of digital binary images with the help of a set of 3×3 masks. The result of any operation is placed in the central position of the mask. The masks are shown in Fig. 1 and the order in which they are applied is: A1, B1, A2, B2, A3, B3, A4, B4.

Each of the masks consists of two subgroups, white and black, as shown by the unshaded positions and positions shaded black respectively in Fig. 1. The positions marked by 'x' in the masks are 'don't care' positions and need not be considered for a particular mask. The operation of each mask can be divided into the following three stages:

(i) Find whether all the pixels in the white subgroup are lesser in graylevel value than the pixel on which the mask is currently centred.

(ii) Find whether the pixels in the black subgroup are greater in value than the central pixel.

(iii) If both the conditions given above in (i) and (ii) are satisfied, then replace the pixel in the central position of the mask by the maximum of the graylevel values of the pixels in the white subgroup.

Following Goetcherian's technique, for every pixel in an image, its eight neighbours have to be considered for performing any computation. Therefore, the first major task is to provide every mask with pixel values corresponding to a central pixel and its eight neighbouring

pixels. The memory unit has, therefore, been designed so that it provides a pixel in one column with three rows simultaneously. To obtain all the eight neighbours of a particular pixel simultaneously, a set of six registers (R_1, \dots, R_6) clocked by a 3-phase clock, generated internally, has been incorporated in the design.

3 CHIP ARCHITECTURE

The overall datapath for the complete operation is shown in Fig. 2. The chip comprises eight blocks, with each block performing the operation corresponding to a mask represented by Goetcherian's algorithm. Each block has three RAM banks each of 512 bytes capacity. The algorithm specifies that the operation of the i -th mask should be performed on the output of the $(i - 1)$ th mask. The blocks implementing operations of the masks are, therefore, connected in a pipeline style. Each mask requires data corresponding to three consecutive rows for performing any operation and each of them extends the image on all four sides. A mask can start computation

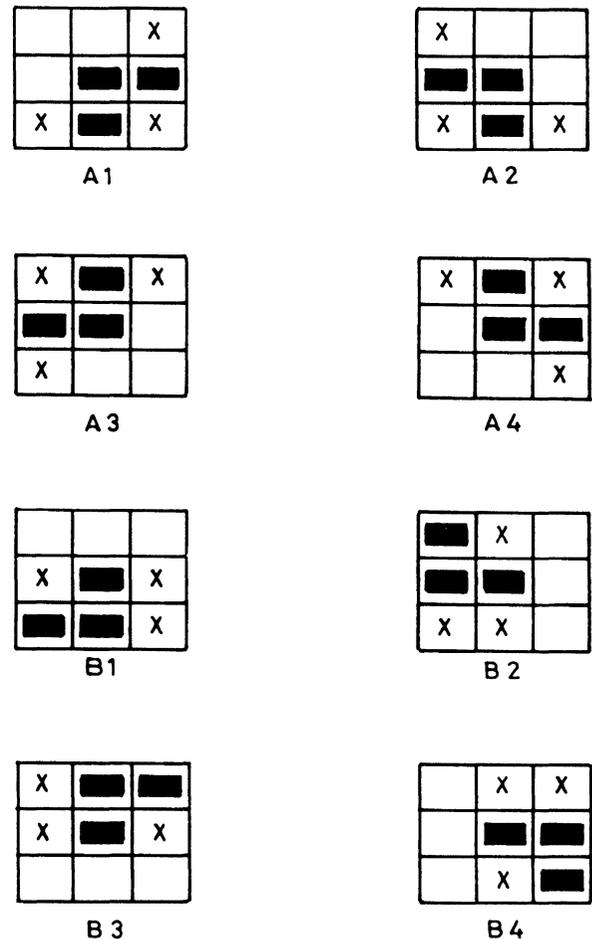


FIGURE 1 Masks used for the skeletonization.

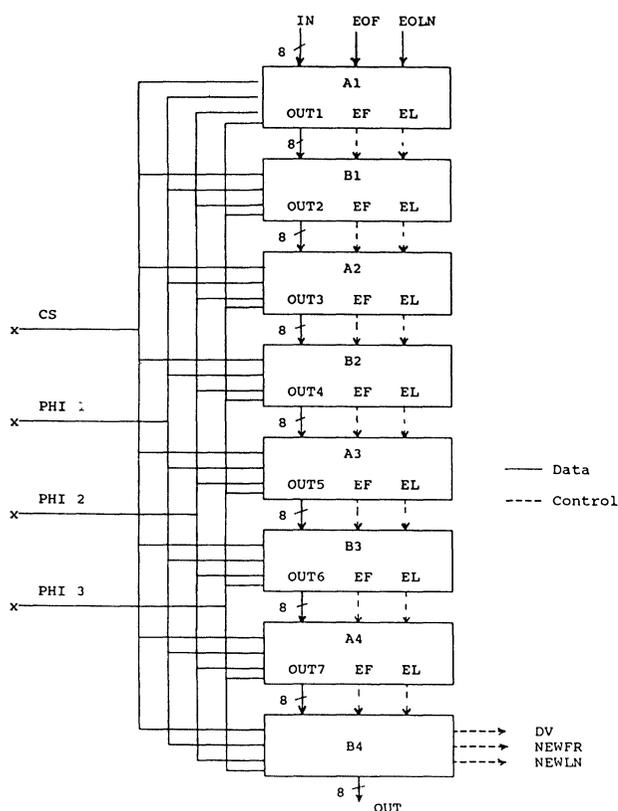


FIGURE 2 Overall datapath for the chip.

when it receives (i) data corresponding to the second row from the previous mask, (ii) the data corresponding to the first row which has already been stored in its memory bank, and, (iii) the second row of data which it is currently receiving.

3.1 The Datapath

The datapath can be followed with reference to the schematic diagram of a mask shown in Fig. 3(a). There are two sets of registers (R_1, R_2, R_3) and (R_4, R_5, R_6). These two register sets are clocked by the phases PHI2 and PHI3 of a three phase non-overlapping clock. The inset in Fig. 3(a) shows the phases of the clock. The three outputs of the memory unit go to the first set of registers as inputs while the outputs of the latter are connected to the second set of registers. The outputs of the second set of registers (R_4, R_5, R_6), which are clocked by PHI3, provide the $(j - 1)$ th column pixels of the rows $(i - 1)$, i and $(i + 1)$. The outputs of the first set (R_1, R_2, R_3) clocked by PHI2, give the j th column pixels of the same three rows. The outputs of the memory unit provide the $(j + 1)$ th column pixels in turn. The pixel P_{ij} obviously occurs at the output of one of the first set of registers (R_1, R_2, R_3). Since the memory unit outputs change at the end

of the clock phase PHI1, the outputs at the memory unit will have the $(j + 1)$ th column pixels at the end of PHI1 at which time the pixels neighbouring p_{ij} will be obtained at the appropriate positions. The computation to be performed in each mask has to be completed before the values at the outputs of the registers and the memory unit change.

3.2 Implementation of Mask Operations

The mask operations have been implemented with the help of the module Find-Max shown in Fig. 3(a & b). Since the white subgroup consists of three pixels in each mask and the black subgroup of two pixels (Fig. 1) a total of five 8-bit comparators are required for implementing operations (i) and (ii) above. For finding the maximum of the pixels in the white subgroup, two 8-bit comparators and two 8-bit multiplexers have been used. Another multiplexer is used to select either the central pixel value or the maximum of the pixel values in the white subgroup on the conditions given in (i) and (ii) for onward transmission to the next memory unit (the central pixel value should not be changed in the current unit because the pixel would be used for computations centred on other pixels).

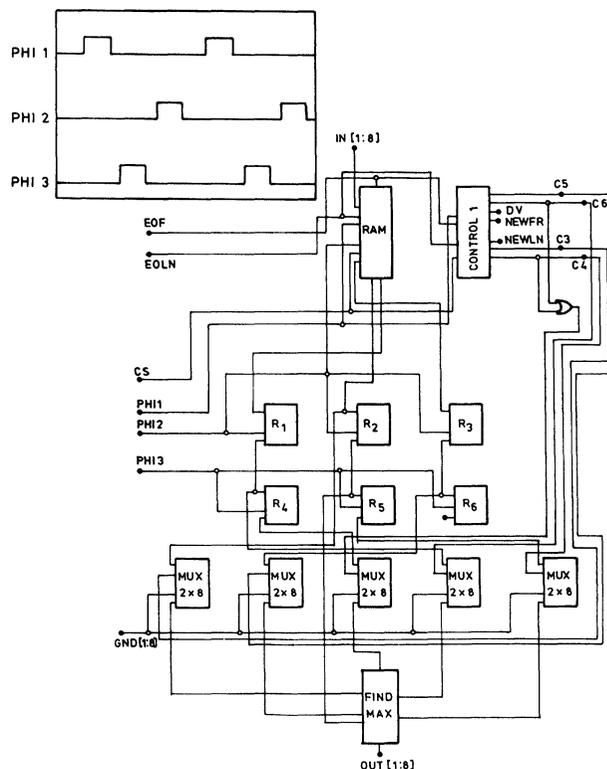


FIGURE 3(a) Schematic of mask A_1 (Inset: Three phases of the clock).

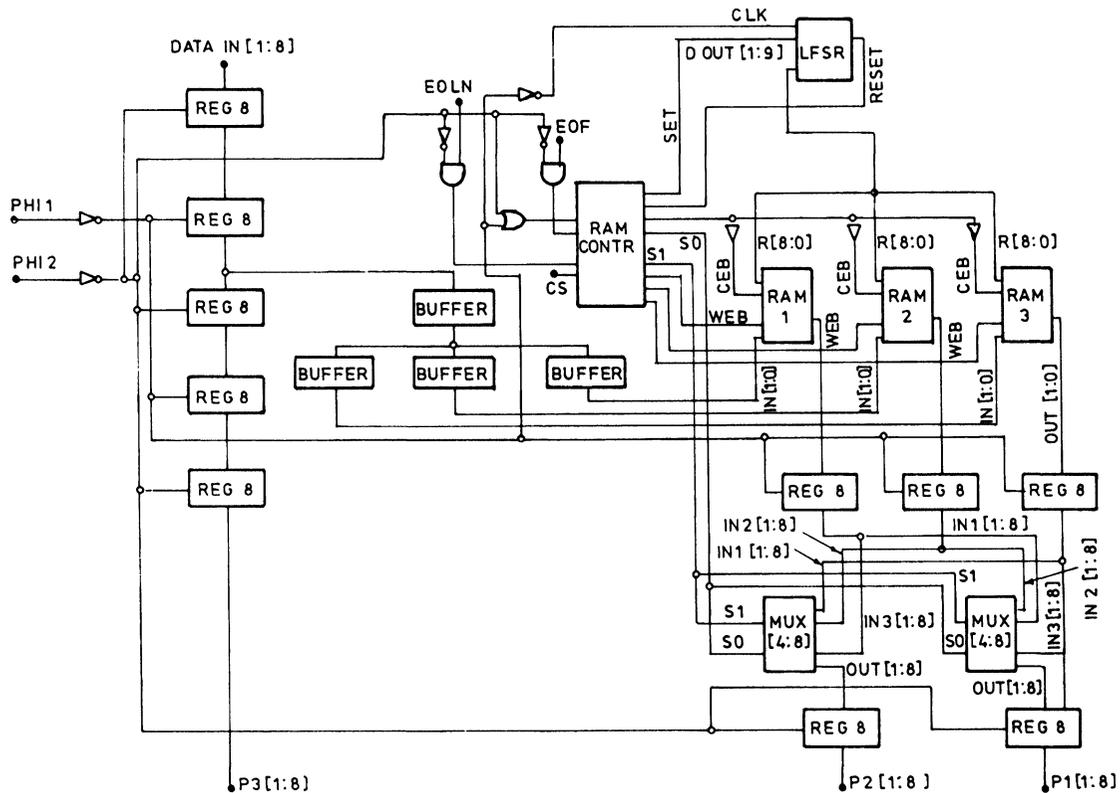


FIGURE 4 Schematic of memory unit.

3.5.1 RAM Controller

The RAM controller supplies the signals CEB (Chip Enable Bar) to initiate read or write, the three Write Enable Bar signals WEB1, WEB2 and WEB3 for the three RAM banks, the status signals S0 and S1 to control the multiplexers and the set and reset pulses for the address generator. The inputs to the RAM controller are the signals EOLN (end of line), EOF (end of frame) and the chip select CS. The clock is obtained by Or-ing PHI1 and PHI2.

3.5.2 Chip Controllers

The chip controllers CONTROL 1 and CONTROL 2 take as their input signals EOF, EOLN and RESET which initializes the controllers and the chip. The controllers provide the control signals needed for extension of the image at the four sides as well as control signals required for interface between two consecutive masks. They also provide the signals DV (data valid), NEWFR (new frame) and NEWLN (new line).

The state diagram for CONTROL 1 is shown in Fig. 5. It has 25 states and is clocked by PHI1. The output signals are C₃, C₄, C₅, C₆, DV, NEWFR and NEWLN. The controller goes to state I whenever the chip RESET

line is made active, and remains there until an EOF signal is detected whereupon it moves to state A. It waits in state A for one row while the first row is being stored

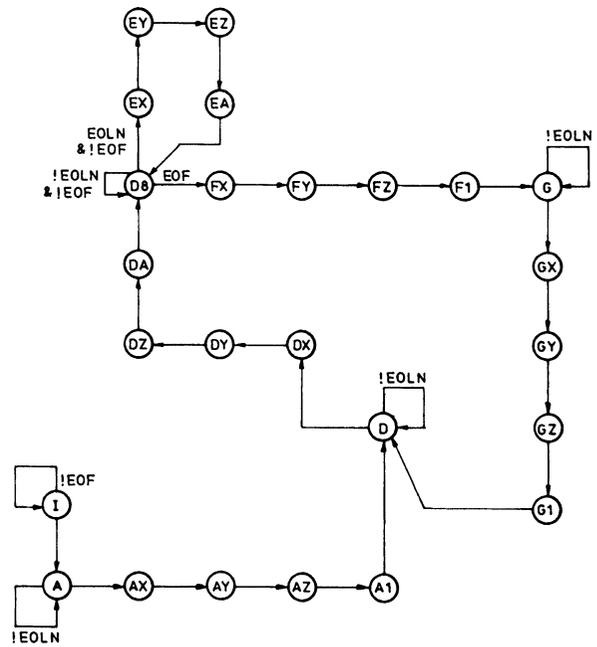


FIGURE 5 State Diagram for chip controller CONTROL 1.

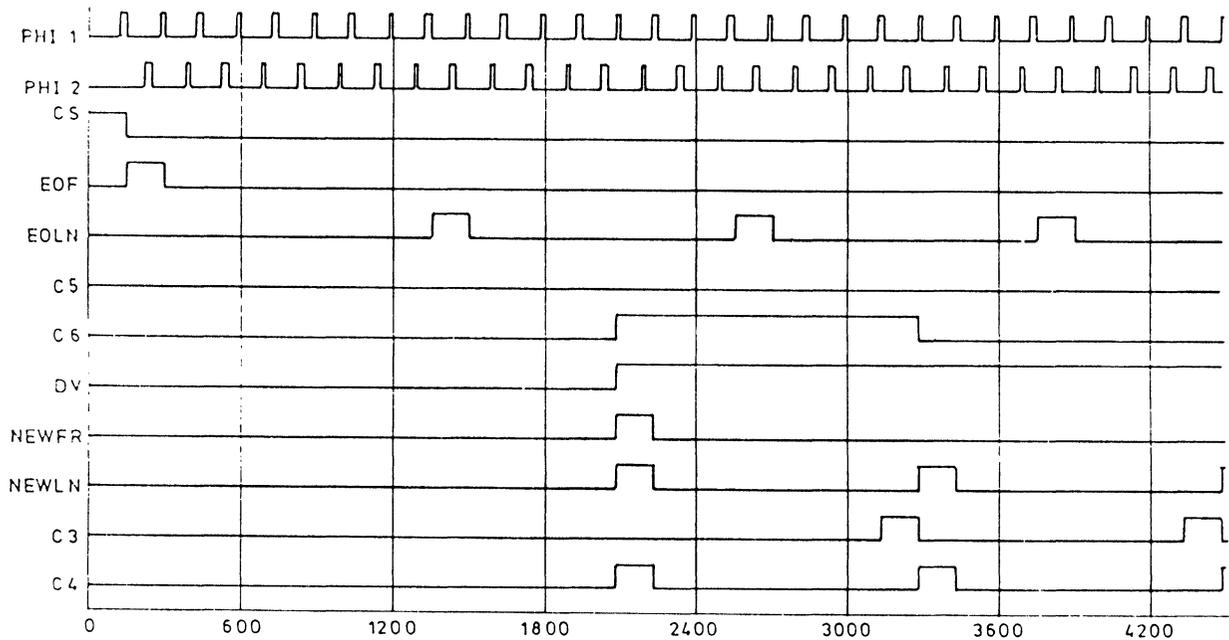


FIGURE 6 Control signals generated by CONTROL 2.

and, when an EOLN signal is detected, it moves to AX. Fig. 5 illustrates the state transitions through one complete frame and the control signals generated by CONTROL 1 are shown in Fig. 6.

Chip controller CONTROL 2 is used to interface between two consecutive masks. The inputs to the controller are the 'end of frame' and 'end of line' signals of the previous mask. For the first mask A_1 , these are identical to the EOF and EOLN signals input to the chip. For the other masks these signals are the EF (end of frame) and EL(end of line) signal output of CONTROL 2 of the previous mask. The state transition diagram for CONTROL 2 is illustrated in Fig. 7.

3.6 Operating Frequency

Since the chip requires a three-phase non-overlapping clock, a clock generator has been designed using JK flip-flops. The input to the chip can be a single clock which would be converted to the three phase non-overlapping clock internally by the clock generator. The operating frequency of the clock is decided by the rate at which data come into the chip (fresh data are supposed to come into the chip on every positive pulse of PHI2). For a 512×512 image and a frame rate of 30 per second, a clock period of 127 ns is obtained. The minimum operating frequency of the chip would thus be around 8 MHZ. In the present work, a higher operating frequency could not be envisaged because the pseudo-static RAMs used in the design have a cycle time of 100 ns which

allows only one read or write per cycle. The operating frequency can be considerably enhanced if faster RAMs are used.

4 IMPLEMENTATION OF THE DESIGN

The chip was implemented using VTI (VLSI Technology Inc) CAD tools based on a two metal CMOS process on a SUN 3 workstation. CMOS standard cells, having a minimum line geometry of 1.5 μ m, were used for implementing the datapaths. The controllers and the memory were implemented as compiled cells using the

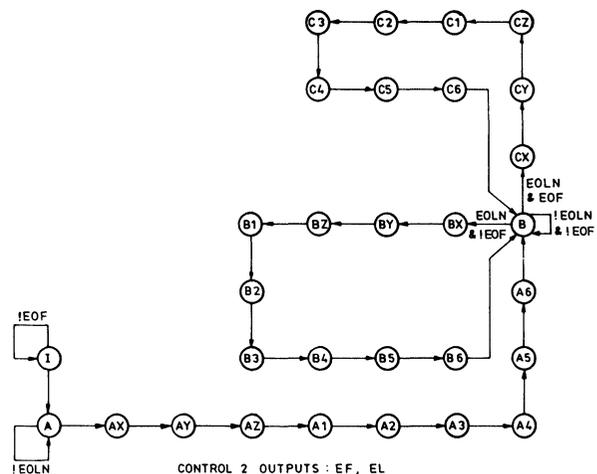


FIGURE 7 State diagram for ship controller CONTROL 2.

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Biographies

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