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Fault Modeling of ECL for High Fault Coverage of Physical Defects

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Bipolar Emitter Coupled Logic (ECL) devices can now be fabricated at higher densities and consumes much lower power. Behaviour of simple and complex ECL gates are examined in the presence of physical faults. The effectiveness of the classical stuck-at model in representing physical failures in ECL gates is examined. It is shown that the conventional stuck-at fault model cannot represent a majority of circuit level faults. A new augmented stuck-at fault model is presented which provides a significantly higher coverage of physical failures. The model may be applicable to other logic families that use logic gates with both true and complementary outputs. A design for testability approach is suggested for on-line detection of certain error conditions occurring in gates with true and complementary outputs which is a normal implementation for ECL devices.

Keywords: Fault Modeling, Design for Testability, Stuck-at fault model, Augmented Stuck-at fault model, Emitter Coupled Logic, Complementary Outputs

1. INTRODUCTION

Emitter Coupled Logic (ECL) using bipolar technology is a non-saturated form of digital logic which eliminates transistor storage time as a speed limiting characteristic, permitting very high speeds of operation [1]. Conventional bipolar ECL technology represents the state of the art in silicon speed, providing system propagation delays of the order of 300 to 500 pico seconds but the price paid for such speeds is very high power dissipation (1.5 mW or more per gate—way too much for VLSI densities) [2]. Transistor size and circuit density are two factors causing high power dissipation. Some recent developments in technology such as BIT1 [2] have made it possible to create smaller bipolar transistors and ECL devices are being fabricated at higher densities and much lower power. A BIT1 transistor takes about 1/20th the area of conventional ECL devices and the speed is comparable to the fastest ECL transistors which is achieved at 1/10th the power [2].

With the attainment of low power, high speed, as well as high density, ECL technology is expected to be used widely in various high performance digital circuits. Using the B5000 ECL Sparc series of components, for example, small ECL systems that perform have been designed that perform at a level equal to large mainframe computers and approach that of present day supercomputers [3]. Even more highly integrated bipolar and bipolar/MOS chips are expected in future, further narrowing the gap between low cost workstations and high performance servers.

Transistor level shorts and opens model a majority of the physical failures and defects in ICs [4,5]. Defects and failures in present day integrated circuits can be abstracted to shorts and opens in the interconnects and degradation of devices [6]. Therefore, fault models at the transistor level, can characterize failures quite accurately [5,7–12]. For MOS devices it has been shown that gate level models may not correctly represent some major failure modes [13–15]. Analysis of faults in simple logic circuits suggest that transistor level testing provides a higher coverage of faults compared to that at gate level [16]. It is necessary to study the effects of failures at the transistor level and develop accurate fault models at this level [4]. The major fault models at transistor level are stuck-at faults, stuck-shorts and opens of transistor and interconnects, and bridging faults [17]. Fault models for one-level and two-level ECL gates are given in [18] and [19] respectively. Modeling and analysis of bridging faults in Emitter Coupled Logic devices were presented in [20] and [21].

In this paper, we first examine an ECL OR/NOR gate for various physical failures and their effects. SPICE simulations are used to verify analytically derived results. Delay faults due to various physical failures are not considered in this study. Effects of different physical faults are compared with the classical stuck-at fault model and the fault coverage is obtained. We propose an augmented stuck-at fault model which provides a higher coverage of physical failures, and extend this philosophy to a 2-level complex ECL gate. Morandi et. al. [22] have proposed an ECL logic model obtained using the dictionary for translating each circuit element into a gate level description, which results in a complicated logic model even for a simple ECL OR/NOR circuit description. The proposed augmented stuck-at fault model is much simpler than the logic level fault model proposed in [22]. Finally, a design for testability approach is suggested to detect certain error conditions, termed LIKE errors or loss of complementarity [23], exhibited by gates having true and complementary outputs.

This paper is organized as follows. In section 2, a brief description of Emitter Coupled Logic and ECL OR/NOR gate operation is given. Sections 3 and 4 deal with the analysis of physical defects, application of classical stuck-at fault model and proposed augmented stuck-at fault model of one-level and two-level ECL gates respectively. In Section 5, we suggest a design for testability approach. Conclusions are given in Section 6.

2. EMITTER COUPLED LOGIC

Schottky TTL produces speed improvement by prevention of saturation, but ECL uses differential amplifier configuration to control current levels so as to avoid saturation. Emitter Coupled refers to the manner in which the emitters of the differential amplifier are connected within the integrated circuit [24]. The differential amplifier provides a high input impedance and a voltage gain within the circuit. Emitter follower outputs restore the logic levels and provide low output impedance for good line driving and high fan-out capability [1]. OR/NOR gate is used as the basic building block in most implementations of current day ECL logic designs. Figure 1 shows the implementation used in the Motorola MECL logic family [1].

The operation of a basic ECL OR/NOR gate can be explained by referring to Figure 1. Transistors Q_1, Q_2 along with Q_3 form a differential amplifier with base voltage of Q_3 (VB_3) derived from an internal refer-

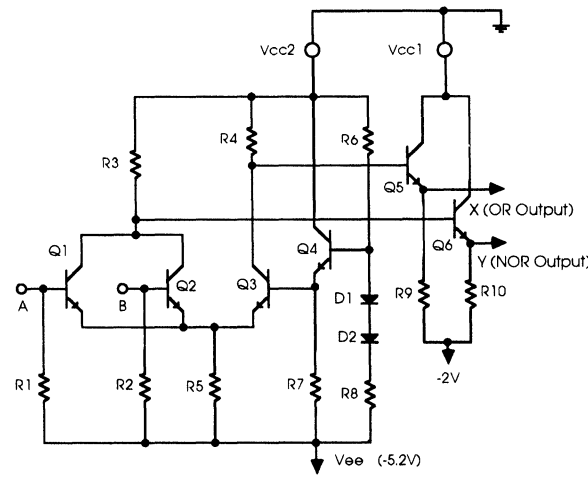

FIGURE 1 Circuit diagram of a 2-input ECL OR/NOR gate.

ence circuit. The transistor stage Q_4 is a temperature and voltage compensation network to provide stable reference (V_{BB}) at about the center of the output voltage swing. The functioning of the ECL OR/NOR gate can be summarized as follows: The transistor Q_3 will conduct only when the input transistors (Q_1) and (Q_2) are held OFF with low input voltages as (V_{IL}). As soon as any one of the transistors is turned ON (i.e. an input transition to V_{IH}), Q_3 turns OFF. Turning OFF of Q_3 causes output of Q_5 (OR output) to go to V_{OH} and that of Q_6 (NOR output) to go to V_{OL}. Similarly, when the input signals revert to low state, Q_1 and Q_2 are turned OFF again and Q_3 gets turned ON. The collector voltages resulting from the switching action of Q_1, Q_2 and Q_3 are transferred through the emitter followers to the output terminals. Hence, the circuit provides logic OR and NOR functions in positive logic, or AND and NAND in the negative logic. No inverters are needed in ECL since every gate provides a direct as well as a complemented output.

The input transistors have their bases held to the V_{ee} line by the pull-down resistors (R_1 and R_2) which provide a leakage current path. Unused input terminals can be left floating without risk of noise coupling to the differential amplifier inputs. The 50 Kohm input resistances maintain logic '0' at inputs with inputs disconnected. The emitter follower output provides sufficient drive capability and also changes the output voltage levels so that the they are compatible with ECL levels. The output of emitter followers are left open without internal load resistances, which allows the connection of matching transmission line and matching impedance/loads at the receive end according to the user requirement which increases speed and reduces power consumption. When using the faster type ECL gate with no output pull-down resistance, there is a choice of a load resistance between using 50 ohm to -2 V or using 510 ohm to the V_{ee} line. A 50 ohm resistor connected to -2 V is commonly used when transmission lines are used for driving. In practice, V_{CC1} and V_{CC2} are connected to ground and V_{ee} is connected to -5.2 V.

The reference voltage (emitter of transistor Q_4) which tracks V_{CC} is approximately -1.3 V. The output logic levels are between -1.63V and -1.85V for V_{OL} and -0.810V and -0.980 for V_{OH}. Transistor Q_4 along with the diode and resistor network forms the temperature and voltage compensated bias network. Transistors Q_5 and Q_6 constitute the emitter follower outputs. Resistors R_9 and R_{10} are connected externally and are not provided internally by the ECL OR/NOR gate.

Just like complex gates in nMOS and CMOS, multilevel implementations are possible in ECL. One of the techniques is called series gating in which transistor pairs are 'stacked' one above the other in 'tiers' so that current can be steered through different paths. The penalty for the additional functionality is an increase in the propagation delay; however, this generally is less than in the case where the function is decomposed into two or more gates [3].

3. FAULT MODELING OF THE ECL OR/NOR GATE

In this section, results obtained for fault modeling of ECL OR/NOR gate are summarized. The response of the basic ECL OR/NOR gate for various faults is evaluated. Possible hard failures considered here include all possible opens and shorts of transistors, diodes and resistors, transistor junction opens and shorts. ECL OR/NOR gate circuit outputs are obtained after performing analysis for all input vectors by simulating one fault at a time for all the possible hard faults (opens, shorts etc.) of all the devices (transistors, diodes and resistors). The ECL OR/NOR gate outputs obtained analytically have been verified with the SPICE simulation outputs to ensure that there are no inconsistencies.

Table I lists the various fault groups and the physical faults considered. This includes all opens and shorts of transistors, diodes and resistors, transistor junction opens and shorts. The output of the circuit behavior obtained under various defects are tabulated by combining and grouping the various faults. While some faults cause an undefined logic level, some faults are undetectable at logic level as there are no

TABLE I List of Fault groups vs Physical failures

ff: Fault-free, *R*1/*R*2 Open, *D*1/*D*2 Short.
*f*1: *Q*1 Emitter/Base Open, *R*1 Short.
*f*2: *Q*1 Collector Open.
*f*3: *Q*2 Emitter/Base Open, *R*2 Short.
*f*4: *Q*2 Collector Open.
*f*5: *Q*3 Emitter/Base Open, *Q*4 Emitter/Base/Collector Open, *R*6 Open, *R*7/*R*8/*Q*1/*Q*2 Short.
*f*6: *Q*3 Collector Open, *R*4/*Q*5 Short, *Q*5 Base to Collector Short.
*f*7: *Q*5 Emitter/Base/Collector Open, *R*4 Open, *Q*5 Base to Emitter Short, *R*9 Short.
*f*8: *Q*6 Emitter/Base/Collector Open, *R*3 Open, *Q*1/*Q*2 Base to Collector Short, *Q*6 Base to Emitter Short, *R*10 Short.
*f*9: *R*5 Open, *Q*3 Base to Emitter Short.
*f*10: *R*7 Open, *Q*4 Base to Emitter Short.
*f*11: *R*8/*D*1/*D*2 Open, *R*6/*Q*3/*Q*4 Short, *Q*4 Base to Collector Short.
*f*12: *R*9 Open.
*f*13: *R*10 Open.
*f*14: *R*3/*Q*6 Short, *Q*6 Base to Collector Short.
*f*15: *Q*1 Base to Emitter Short.
*f*16: *Q*2 Base to Emitter Short.
*f*17: *Q*3 Base to Collector Short.
*f*18: *R*5 Short.

input patterns for which the faulty and fault-free gate produces opposite logic values at any of the outputs.

An interesting observation which needs mentioning is that of the physical faults *R*1/*R*2 short. The purpose of the input resistances are to maintain the inputs at logic '0' with inputs disconnected. If an ECL gate with *R*1 or *R*2 short is driven by another ECL gate with output equal to logic '1', then the −5.2V appearing at the input due to the short of input resistance will dominate causing the input to appear as logic '0'. It has been verified with SPICE simulation that the input then effectively appears stuck-at-0. Diodes *D*1/*D*2 serve the purpose of temperature compensation and shorting only causes degradation of temperature compensation performance. Some of the fault groups represent effects of several equivalent faults.

3.1 Effectiveness of Classical Stuck-at fault model

In order to model the physical failures, the classical stuck-at fault model is applied to the ECL OR/NOR gate as shown in Figure 2a. The classical stuck-at

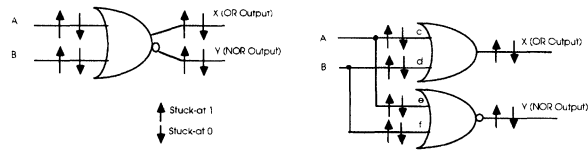

FIGURE 2 (a) Classical stuck-at fault model. (b) Proposed augmented stuck-at fault model.

fault model is exercised with all possible input combinations for fault-free as well as faulty conditions by introducing one stuck-fault at a time. The defective circuit behavior is then compared with the classical stuck-at fault model in representing various component failures. Correlation between OR/NOR gate classical stuck-at fault model output and physical failures is shown in columns 1–3 of Table II. In Table II, a subscript 1(0) is used to indicate a stuck-at 1(0) of a line, for example, A_1 indicates A stuck-at 1, and A_0 indicates A stuck-at 0. The physical failures as modeled by fault-groups $f1, f3, f5, f6, f7, f8$ and $f14$ are modeled accurately using the classical

TABLE II Correlation between Physical failures vs Stuck-at fault models.

		Physical failures vs Stuck-at faults	
Fault groups	No. of faults	Classical Stuck-at model fault	Augmented Stuck-at model fault True o/p, Comp. o/p
$f1$	2	A_0	c_0, e_0
$f2$	1	*Not Covered*	ff, e_0
$f3$	2	B_0	d_0, f_0
$f4$	1	*Not Covered*	ff, f_0
$f5$	10	A_1/B_1	$c_1/d_1/x_1$, $e_1/f_1/y_0$
$f6$	5	X_1	$c_1/d_1/x_1$, ff
$f7$	7	X_0	x_0, ff
$f8$	8	Y_0	ff, $e_1/f_1/y_0$
$f9$	2	*Not Covered*	$c_1/d_1/x_1$, y_1 †
$f10$	2	ff	ff, ff
$f11$	7	*Not Covered*	x_0, y_1 †
$f12$	1	@	@, ff
$f13$	1	@	ff, @
$f14$	3	Y_1	ff, y_1
$f15$	1	*Not Covered*	$c_1/d_1/x_1$, − **
$f16$	1	*Not Covered*	$c_1/d_1/x_1$, − **
$f17$	1	@	x_0, @ **
$f18$	1	*Not Covered*	x_0, y_0 †

ff = *fault-free*, ** = covered by one of the outputs, @ = cannot be modeled at gate level, † = multiple stuck-at fault, *No. of faults* = Number of Physical failures included, − = too complex to be modeled at gate level.

stuck-at fault model. The faults $f12$, $f13$ and $f17$ cause one of the output to become indeterminate, which cannot be represented by a logical fault model. From the rest, the classical stuck-at fault model leaves 7 fault groups uncovered, corresponding to 14 physical failures. In the next section, we present an augmented stuck-at fault model that provides a higher coverage of physical failures compared to the classical stuck-at fault model.

3.2 An Augmented Stuck-at fault model

As shown above, the classical input/output stuck-at fault model is not effective in modeling a large fraction of ECL gates. Figure 2b shows the proposed augmented stuck-at fault model which improves the fault coverage. Here, the device is modeled as a parallel combination of an OR gate and a NOR gate. There are thus six independent nodes to be considered. The augmented stuck-at fault model is exercised with all possible input combinations for fault-free as well as faulty conditions by introducing one stuck fault at a time.

For further classification and correlation between physical failures and stuck-at fault model, comparison is done between the circuit behavior [18] and with that of the proposed augmented stuck-at fault model output. The outcome is presented in column 4 of Table II, which also lists the faults modeled by the augmented stuck-at fault model. Here, (c_0,e_0) indicates that the true output is modeled as c stuck-at-0 and complementary output is modeled as e stuck-at-0. It can be seen that fault groups $f2, f4, f9, f11$, $f15, f16, f17$ and $f18$ not modeled by the classical stuck-at fault model, are modeled by the augmented stuck-at fault model [25]. Fault groups $f15, f16$ and $f17$ are modeled and are observable at one of the outputs only (True outputs in these cases). Fault groups $f15, f16$ and $f17$ exhibit the fault as a complex logical fault. Again, fault groups $f12$ (True output) and $f13$ (Complementary output) are not modeled by the augmented stuck-at fault model. These faults cannot be modeled at the gate level, as the erroneous output always appear as an undefined value (U), however the complementary output appears as fault free. Also note that, the multiple fault (c_0,e_0) is equivalent to A_0, which may be covered by the output of the driving logic stuck-at-0. The same is true for $f3$ and $f5$. Only the fault groups $f9, f11$ and $f18$ are always required to be represented by multiple stuck-at faults.

The multiple stuck-at fault model is an extension of the single stuck fault model, where in several lines are considered to be simultaneously stuck. If n is denoted to be the number of possible single stuck fault sites, then there are 2^n single stuck faults. Assuming that any multiple stuck fault can occur including the condition of all lines simultaneously stuck, there are $3^n - 1$ possible multiple stuck faults. Assuming that the multiplicity of a fault is no greater than a constant k, then the number of possible multiple stuck faults (F) is given as,

$$F = \sum_{i=1}^{k} \binom{n}{i} 2^i$$

which is usually too large a number to deal explicitly with all multiple faults [26]. For example, the number of multiple faults (double faults, where $k = 2$) in a circuit with $n = 1000$ possible fault sites is about 2 million.

Applying multiple stuck-at faults to Figure 2a with a multiplicity of faults equal to 2, i.e. double faults, would need 72 multiple faults to be considered, which is obtained by substituting $k = 2$ and $n = 10$ in the expression for F. Considering all 72 multiple stuck faults and obtaining a table for all input vectors is too difficult a task. Referring to column 4 of Table II, we know apriori the behavior of augmented fault model to the 2-level ECL gate. For fault group $f9$, one possibility is to consider the multiple stuck fault of x_1 and y_1 for true and complementary outputs respectively. Similarly, multiple stuck faults need to be considered only for $f11$ and $f18$. Only 3 multiple stuck faults need be considered out of 72 possible double faults since the multiple faults are known apriori from the augmented fault model.

Excluding $f10$, $f12$, $f13$ and $f17$, only about 73.58% of the physical failures are covered by the

classical stuck-at fault model whereas 94.33% coverage of all detectable faults is obtained using the augmented stuck-at fault model. Even better coverage is obtained if special handling is done for $f15$, $f16$ and $f17$. Test generation and fault simulation would be able to function properly if the complemented output for these cases are assumed to be unknown. In that case 100% fault coverage of the deterministically testable faults would be obtained. Only 8 single and 3 double stuck-at fault groups need to be considered for modeling all the physical failures of the ECL OR/NOR gate. The proposed augmented stuck-at fault model is also a much simpler and effective fault model compared to the complicated logic model proposed by Morandi et. al. [22], which is obtained using the dictionary for translating circuit elements into a gate level description.

Another possibility is to consider the structure of the fault model shown in Figure 2a with multiple stuck-at faults which would provide 90.56% fault coverage. Fault groups $f2$ and $f4$ in this case cannot be included by multiple stuck-at faults using the structure shown in Figure 2a. The fault coverage obtained would still be less than the fault coverage obtained using the proposed augmented stuck-at fault model but the number of nodes need to be considered would be less.

4. TWO-LEVEL COMPLEX ECL GATE

In this section we extend the fault model to a 2-level ECL gate.The response of the 2-level ECL gate is evaluated for various faults. The 2-level ECL gate circuit realizing the true function $(A + B).(C + D)$ and its complementary function $\overline{(A + B).(C + D)}$ is used as an example and is shown in Figure 3.

A list of possible hard failures (opens, shorts etc.) which affect the circuit functionality is given in Table III. Possible hard failures considered include all possible opens and shorts of transistors, diodes and resistors, transistor junction opens and shorts.

The 2-level ECL gate circuit outputs are obtained after performing SPICE simulations for all input vectors by simulating one failure at a time for all the possible hard failures (opens, shorts etc.) of all the devices (transistors, diodes and resistors). The output of the circuit behavior obtained under various defects are tabulated by combining and grouping the various faults [19]. Results for a few interesting fault groups are given in Table IV.

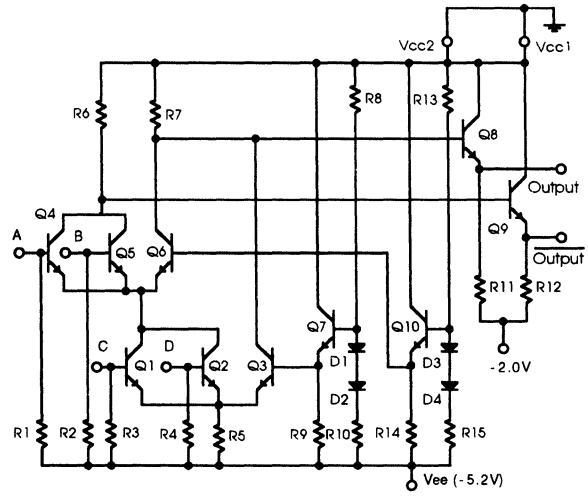

FIGURE 3 Two-level implementation of $(A + B)(C + D)$ and $(A + B)(C + D)$.

Effectiveness of Classical Stuck-at fault model for 2-level Complex ECL Gates

Several gate level implementations are possible for the logic function $(A + B).(C + D)$ and its complement $\overline{(A + B).(C + D)}$. A gate level implementation of the above functions is shown in Figure 4a. In order to model the physical failures, the classical stuck-at fault model is applied to the 2-level ECL gate as shown in Figure 4a. Results shown in Table V were obtained by exercising the model with all possible input combinations for fault-free as well as faulty conditions by introducing one stuck fault at a time. The defective circuit behavior (Table IV) now can be compared with the classical stuck-at fault model output (Table V) to obtain the effectiveness of the stuck at model in representing various component failures.

Correlation between 2-level ECL gate classical stuck-at fault model output and physical failures is shown in columns 1–3 of Table VI, where it can be seen that almost all the classical stuck-at faults model

TABLE III List of Fault groups vs Physical failures

ff: Fault-free, *R*1/*R*2/*R*3/*R*4/*R*9 Open, *D*1/*D*2/*D*3/*D*4/*R*9 Short, *Q*7 Base to Emitter Short.
*f*1: *Q*1 Emitter/Base Open, *R*2 Short.
*f*2: *Q*1 Collector Open.
*f*3: *Q*2 Emitter/Base Open, *R*1 Short.
*f*4: *Q*2 Collector Open.
*f*5: *Q*3 Emitter/Base Open, *Q*7 Emitter/Base/Collector Open, *R*8 Open, *R*9/*R*10 Short.
*f*6: *Q*3 Collector Open.
*f*7: *Q*4 Emitter/Base Open, *R*4 Short.
*f*8: *Q*4 Collector Open.
*f*9: *Q*5 Emitter/Base Open, *R*13 Open, *R*3 Short.
*f*10: *Q*5 Collector Open.
*f*11: *Q*6/*Q*10 Emitter/Base/Collector Open, *R*14/*R*15 Short.
*f*12: *R*14 Open, *Q*8 Emitter/Base/Collector Open, *R*11/*Q*3 Base to Collector Short.
*f*13: *Q*9 Emitter/Base/Collector Open, *R*6 Open, *R*12/*Q*9 Emitter to Base Short.
*f*14: *D*1/*D*2/*D*3/*D*4/*R*10/*R*15 Open, *Q*3/*Q*6/*Q*7/*Q*10 Short, *Q*10 Emitter to Base Short, *Q*7/*Q*10 Base to Collector Short, *R*8/*R*13 Short.
*f*15: *R*5 Open, *Q*1/*Q*2/*Q*3 Emitter to Base Short.
*f*16: *R*7 Open, *Q*8 Emitter to Base Short.
*f*17: *Q*9 Base to Collector Short, *R*6/*Q*9 Short.
*f*18: *Q*10 Emitter/Base Open, *Q*1/*Q*2 Short.
*f*19: *Q*4/*Q*5 Short.
*f*20: *Q*4 Emitter to Base Short.
*f*21: *Q*5 Emitter to Base Short.
*f*22: *Q*6 Emitter to Base Short.
*f*23: *Q*1 Base to Collector Short.
*f*24: *Q*2 Base to Collector Short.
*f*25: *Q*4 Base to Collector Short.
*f*26: *Q*5 Base to Collector Short.
*f*27: *Q*8 Base to Collector Short, *R*7/*Q*8 Short.
*f*28: *R*11 Open
*f*29: *R*12 Open
*f*30: *R*5 Open

TABLE IV Circuit behavior under physical failures of 2-level Complex ECL gate (*ff* = Fault-free, *f*1–*f*17 = Defective).

	2-lv ECL Stuck Open/Short Analysis										
Input	*ff*	*f*1	*f*2	*f*4	*f*14	*f*16	*f*18	*f*22	*f*27	*f*28	*f*29
ABCD	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y
0000	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	1 1	U 1	0 1
0001	0 1	0 1	0 1	0 1	0 1	0 0	1 0	0 1	1 1	U 1	0 1
0010	0 1	0 1	0 1	0 1	0 1	0 0	1 0	0 1	1 1	U 1	0 1
0011	0 1	0 1	0 1	0 1	0 1	0 0	1 0	0 1	1 1	U 1	0 1
0100	0 1	0 1	1 1	0 1	0 1	0 1	0 1	1 1	1 1	U 1	0 1
0101	1 0	0 1	1 1	1 0	0 1	0 0	1 0	1 1	1 0	1 0	1 U
0110	1 0	0 1	1 1	1 0	0 1	0 0	1 0	1 1	1 0	1 0	1 U
0111	1 0	0 1	1 1	1 0	0 1	0 0	1 0	1 1	1 0	1 0	1 U
1000	0 1	0 1	0 1	1 1	0 1	0 1	0 1	1 1	1 1	U 1	0 1
1001	1 0	1 0	1 0	1 1	0 1	0 0	1 0	1 1	1 0	1 0	1 U
1010	1 0	1 0	1 0	1 1	0 1	0 0	1 0	1 1	1 0	1 0	1 U
1011	1 0	1 0	1 0	1 1	0 1	0 0	1 0	1 1	1 0	1 0	1 U
1100	0 1	0 1	0 1	0 1	0 1	0 1	0 1	1 1	1 1	U 1	0 1
1101	1 0	1 0	1 0	1 0	0 1	0 0	1 0	1 1	1 0	1 0	1 U
1110	1 0	1 0	1 0	1 0	0 1	0 0	1 0	1 1	1 0	1 0	1 U
1111	1 0	1 0	1 0	1 0	0 1	0 0	1 0	1 1	1 0	1 0	1 U

X = OR Output, Y = NOR Output, U = Undefined.

some physical failures. The physical failures represented by fault-groups *f*1, *f*3, *f*5, *f*7, *f*9, *f*12, *f*13, *f*17, *f*18, *f*19 and *f*27 are modeled accurately using the classical stuck-at fault model. The faults *f*28 and *f*29 cause one of the outputs to become indeterminate, which cannot be represented by a logical fault model. From the remaining, the classical stuck-at fault model leaves 17 fault groups uncovered out of 28 detectable fault groups, corresponding to 40 physical failures out of 76 possible hard failures examined. Only 39.28% fault groups are covered using the classical stuck-at fault model corresponding to 47.36% of physical failures. In the next section, we present an augmented stuck-at fault model that provides a higher coverage of physical failures compared to the classical stuck-at fault model.

An Augmented Stuck-at fault model for 2-level ECL Gates

The classical input/output stuck-at fault model is not effective for modeling ECL gates. Figure 4b shows the proposed augmented stuck-at fault model which improves the fault coverage. Here, the device is modeled as a parallel combination of OR-AND and OR-NAND gates realizing the true and complementary

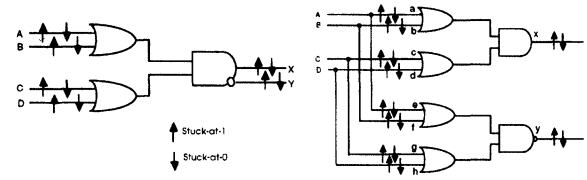

FIGURE 4 (a) Classical stuck-at fault model. (b) Proposed augmented stuck-at fault model.

TABLE V ECL 2-level Complex Gate outputs for Classical Stuck-at fault model.

	2-level ECL Gate Classical Stuck-at fault model												
Input	*ff*	A_0	A_1	B_0	B_1	C_0	C_1	D_0	D_1	X_0	X_1	Y_0	Y_1
ABCD	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y	X Y
0000	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	0 1	1 1	0 0	0 1
0001	0 1	0 1	1 0	0 1	1 0	0 1	0 1	0 1	0 1	0 1	1 1	0 0	0 1
0010	0 1	0 1	1 0	0 1	1 0	0 1	0 1	0 1	0 1	0 1	1 1	0 0	0 1
0011	0 1	0 1	1 0	0 1	1 0	0 1	0 1	0 1	0 1	0 1	1 1	0 0	0 1
0100	0 1	0 1	0 1	0 1	0 1	0 1	1 0	0 1	1 0	0 1	1 1	0 0	0 1
0101	1 0	1 0	1 0	0 1	1 0	1 0	1 0	0 1	1 0	0 0	1 0	1 0	1 1
0110	1 0	1 0	1 0	0 1	1 0	0 1	1 0	1 0	1 0	0 0	1 0	1 0	1 1
0111	1 0	1 0	1 0	0 1	1 0	1 0	1 0	1 0	1 0	0 0	1 0	1 0	1 1
1000	0 1	0 1	0 1	0 1	0 1	0 1	1 0	0 1	1 0	0 1	1 1	0 0	0 1
1001	1 0	0 1	1 0	1 0	1 0	1 0	1 0	0 1	1 0	0 0	1 0	1 0	1 1
1010	1 0	0 1	1 0	1 0	1 0	0 1	1 0	1 0	1 0	0 0	1 0	1 0	1 1
1011	1 0	0 1	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 0	1 0	1 0	1 1
1100	0 1	0 1	0 1	0 1	0 1	0 1	1 0	0 1	1 0	0 1	1 1	0 0	0 1
1101	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 1	1 0	0 0	1 0	1 0	1 1
1110	1 0	1 0	1 0	1 0	1 0	0 1	1 0	1 0	1 0	0 0	1 0	1 0	1 1
1111	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	0 0	1 0	1 0	1 1

X = OR Output, Y = NOR Output.

function. Thus, there are 10 independent nodes to be considered. Table VII presents the behavior of the device under this fault model.

For further classification and correlation between physical failures and stuck-at fault model, comparison is done between the circuit behavior [19] and with that of the proposed augmented stuck-at fault model output (Table VII). The outcome is presented in column 4 of Table VI, which also lists the faults modeled by the augmented stuck-at fault model. The fault groups $f2, f4, f6, f8, f10, f11, f14, f15, f16, f20, f21, f22, f23, f24, f25$ $f26$ and $f30$ not modeled by the classical stuck-at fault model, are modeled by the augmented stuck-at fault model [25]. Fault groups $f2, f4, f20, f21, f23$ and $f24$ are modeled and are observable at one of the outputs only. For these fault groups, the other output exhibits the fault as a complex logical fault. Fault groups $f28$ (True output) and $f29$ (Complementary output) cannot be modeled at the gate level, as the erroneous outputs always appear as undefined values (U), however, the complementary outputs appear as fault free.

Fault groups ($f2, f4, f20, f21, f23$ and $f24$) are modeled and observable at one of the outputs only, the other output exhibits complex behavior which cannot be modeled at the gate level. Abnormal behavior may be observed on the other output which is not modeled properly and might lead to fault masking when the outputs reconverge on a subsequent gate.

Table VI column 4 appears to indicate that most of the fault groups in augmented fault model are modeled as multiple faults (double faults). However, several multiple faults can be dropped because of equivalence, for example, the multiple fault ($b_0 f_0$) modeled by fault group $f1$ is equivalent to B_0, which may be covered by the output of the driving logic stuck-at-0. Only the fault groups $f14, f15, f16, f22, f25, f26$ and $f30$ are always required to be represented by multiple stuck-at faults.

Applying multiple stuck-at faults to Figure 4a with a multiplicity of faults equal to 2, i.e. double faults, would need 198 multiple faults to be considered, which is obtained by substituting $k = 2$ and $n = 10$ in the expression for F. Considering all 198 multiple stuck faults and obtaining a table for all input vectors is too difficult a task. Referring to column 4 of Table VI, we know apriori the behavior of augmented fault model of the 2-level ECL gate. For fault group $f14$, we need to consider the multiple stuck fault of x_0 and y_1 for true and complementary outputs. Similarly, multiple stuck faults need to be considered only for $f15, f16, f22, f25, f26$ and $f30$. Only 7 multiple

TABLE VI Correlation between Physical failures vs Stuck-at fault models for 2-level Complex ECL Gate.

Physical failures vs Stuck-at faults			
Fault groups	No. of faults	Classical Stuck-at model fault	Augmented Stuck-at model fault True o/p, Comp. o/p*
$f1$	2	B_0	b_0, f_0
$f2$	1	*Not Covered*	$-, f_0$ **
$f3$	2	A_0	a_0, e_0
$f4$	1	*Not Covered*	$-, e_0$ **
$f5$	6	A_1/B_1	$a_1/b_1, e_1/f_1$
$f6$	1	*Not Covered*	$-, ff$
$f7$	2	D_0	d_0, h_0
$f8$	1	*Not Covered*	ff, h_0
$f9$	3	C_0	c_0, g_0
$f10$	1	*Not Covered*	ff, g_0
$f11$	6	*Not Covered*	$c_1/d_1, ff$
$f12$	5	X_0	x_0, ff
$f13$	5	Y_0	ff, y_0
$f14$	15	*Not Covered*	x_0, y_1†
$f15$	4	*Not Covered*	x_1, y_1 †
$f16$	2	*Not Covered*	$x_0, e_1/f_1$ †
$f17$	3	Y_1	ff, y_1
$f18$	3	A_1/B_1	$a_1/b_1, e_1/f_1$
$f19$	2	C_1/D_1	$c_1/d_1, g_1/h_1$
$f20$	1	*Not Covered*	$c_0, -$ **
$f21$	1	*Not Covered*	$d_0, -$ **
$f22$	1	*Not Covered*	$c_1/d_1, y_1$ †
$f23$	1	*Not Covered*	$c_1/d_1, -$ **
$f24$	1	*Not Covered*	$c_1/d_1, -$ **
$f25$	1	*Not Covered*	c_0, y_0 †
$f26$	1	*Not Covered*	d_0, y_0 †
$f27$	3	X_1	x_1, ff
$f28$	1	@	@, ff
$f29$	1	@	ff, @
$f30$	1	*Not Covered*	x_0, y_0 †

ff = *fault-free*, ** = observable at one of the outputs, @ = cannot be modeled at gate level, † = multiple stuck-at fault, *No. of faults* = Number of Physical failures included, − = too complex to be modeled at gate level.

stuck faults need be considered out of 198 possible double faults since the multiple faults are known apriori from the augmented fault model.

90.78% coverage of all detectable faults is obtained by the augmented stuck-at fault model compared to 47.36% coverage obtained using the classical stuck-at fault model. Even better coverage is obtained if special handling is done for $f2$, $f4$, $f20$, $f21$, $f23$ and $f24$. In that case 100% fault coverage of the deterministically testable faults would be obtained. Only 14 single and 7 double stuck-at faults need be considered for modeling all the physical failures of the 2-level ECL gate investigated. It can be seen that the augmented fault model proposed for 2-level ECL gates is much simpler and effective compared to the logic model proposed by Morandi et. al. [22].

Another possibility is to consider the structure of the fault model shown in Figure 4a with multiple stuck-at faults which would provide 68.42% fault coverage. Fault groups $f8$, $f10$, $f11$, $f12$, $f13$, $f17$ and $f27$ in this case cannot be included by multiple stuck-at faults using the structure shown in Figure 4a. The fault coverage obtained would still be less than the fault coverage obtained using the proposed augmented stuck-at fault model but the number of nodes to be considered would be less.

5. DESIGN FOR TESTABILITY

Careful study of Table IV and corresponding results for ECL OR/NOR gates [18,19] indicate that for some of the physical failures, the input test vectors cause both the true and complementary outputs to exhibit erroneous *LIKE* outputs (i.e. similar outputs, 00 or 11) or loss of complementarity, instead of the true and complementary outputs exhibiting fault-free *UNLIKE* outputs (i.e. 01 or 10). Out of the 18 classified faults for various physical failures of devices for the ECL OR/NOR gate, 7 of the fault groups exhibit erroneous *LIKE* outputs with at least one or more input vectors, which is approximately 39% and out of the 30 classified fault groups for the 2-level ECL gate, 20 of them exhibit erroneous *LIKE* outputs which is approximately 66.66%. By using the following simple design for testability approach, it is possible to ON-LINE detect such faults. This maybe useful in fault-tolerant systems.

A design for testability approach may be based on the use of an exclusive-OR gate connected at the output of certain ECL gates, with the output of the exclusive-OR gate termed as the $\overline{ERROR}$ signal. When the true and complementary outputs of the ECL gate is fault-free *UNLIKE* output (i.e. 01 or 10), then the $\overline{ERROR}$ signal would be a 1 indicating that $\overline{ERROR}$ = 1 and *ERROR* = 0 (i.e. *NO ERROR*).

TABLE VII ECL 2-level Complex Gate outputs for Proposed Augmented Stuck-at fault model.

	2-level ECL Gate Augmented Stuck-at fault model																				
Input	*ff*	*ff*	a_0	a_1	b_0	b_1	c_0	c_1	d_0	d_1	e_0	e_1	f_0	f_1	g_0	g_1	h_0	h_1	x_0	x_1	y_0	y_1
ABCD	X	Y	X	X	X	X	X	X	X	X	Y	Y	Y	Y	Y	Y	Y	Y	X	X	Y	Y
0000	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	1
0001	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	1	1	1	0	1	0	1
0010	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	1	1	1	0	1	0	1
0011	0	1	0	1	0	1	0	0	0	0	1	0	1	0	1	1	1	1	0	1	0	1
0100	0	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0	1	0	1
0101	1	0	1	1	0	1	1	1	0	1	0	0	1	0	0	0	1	0	0	1	0	1
0110	1	0	1	1	0	1	0	1	1	1	0	0	1	0	1	0	0	0	0	1	0	1
0111	1	0	1	1	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	1	0	1
1000	0	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0	1	0	1
1001	1	0	0	1	1	1	1	1	0	1	1	0	0	0	0	0	1	0	0	1	0	1
1010	1	0	0	1	1	1	0	1	1	1	1	0	0	0	1	0	0	0	0	1	0	1
1011	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1
1100	0	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	1	0	0	1	0	1
1101	1	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	1	0	0	1	0	1
1110	1	0	1	1	1	1	0	1	1	1	0	0	0	0	1	0	0	0	0	1	0	1
1111	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1

X = OR Output, Y = NOR Output.

Whenever any of the faults cause the outputs of the gate to exhibit erroneous *LIKE* outputs (i.e. 00 or 11), then the $\overline{ERROR}$ signal would become a 0 indicating that $\overline{ERROR} = 0$ and $ERROR = 1$(i.e. an *ERROR* has occurred). Use of an Exclusive-OR or NOR to detect *LIKE* errors in single level ECL gates would be an increase in area overhead and might be prohibitive. However, if the gate is multiple level and sufficiently complex, then the overhead may be justifiable in some situations. This approach may be effective at module level, at the end of high speed data bus, in clock chains etc. and in other applications where there is probability of *LIKE* errors to occur.

6. CONCLUSIONS

The effectiveness of the classical stuck-at fault model in modeling physical failures that are possible in one and two-level ECL gates have been examined. An augmented stuck-at fault model has been proposed as the classical stuck-at fault model did not model a major fraction of the physical failures. High fault coverage can be obtained using the augmented stuck-at fault model for ECL gates compared to the classical stuck-at fault model. The augmented stuck-at fault model can easily be extended to multi-level complex ECL gates. A design for testability approach was presented for detecting *LIKE* error conditions or loss of complementarity occurring in gates with true and complementary outputs which is a normal implementation for ECL logic devices.

The proposed fault model is also applicable to other logic families such as CVSL (Cascode Voltage Switch Logic), where a logic gate produces a true and a complementary output. It is often noted that test sets based on classical stuck-at model provide a high fault coverage even when a fault is not directly modeled as a stuck-at fault. However, in cases where a fault is not covered explicitly by the model, the test set can only be as effective as a random test set in detecting such a fault. The model proposed here can be used with gate level test generation tools to increase the explicit fault coverage. Fault simulation is used to evaluate the effectiveness of a test set, generated at functional level or based on a fault model. Incorrect modeling of faulty behavior in either one of the outputs could cause the fault simulator to predict

incorrect logic output values. With the augmented model, it is possible to predict the values of both the outputs for a given fault. Consequently, the accuracy of fault coverage estimated using fault simulation can significantly be enhanced by using the augmented model.

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References

[1] W. R. Blood, Jr., *MECL System Design Handbook*, Motorola Semiconductor Products Inc., 1988.

[2] G. Wilson, "*Creating Low-Power Bipolar ECL at VLSI Densities*," VLSI Systems Design, pp. 84–86, May 1986.

[3] E. W. Brown, A. Agrawal, T. Creary, M. F. Klein, D. Murata and J. Petolino, "*Implementing Sparc in ECL*," IEEE Micro, pp. 10–22, Feb. 1990.

[4] J. A. Abraham and W. K. Fuchs, "*Fault and Error Models for VLSI*," Proc. IEEE, Vol. 74, pp. 639–653, May 1986.

[5] J. Gailiay, Y. Crouzet and M. Vergniault, "*Physical versus logical fault models in MOS LSI circuits: Impact on the testability*," IEEE Trans. Computers, Vol. C-29, pp. 527–531. June 1980.

[6] T. E. Mangir, "*Sources of failures and yield improvement for VLSI and restructurable interconnects for RVLSI and WSI: Part I-Sources of failures and yield improvement for VLSI*," Proc. IEEE, Vol. 72, pp. 690–708, June 1984.

[7] N. Burgess and R. I. Damper, "*The inadequacy of the Stuck-at fault model for testing MOS LSI circuits: A review of MOS failure mechanisms and some implications for computer-aided design and test of MOS LSI circuits*," Software Microsyst., Vol. 3, pp. 30–36, Apr. 1984.

[8] S. Gai, M. Mezzalama and P. Prinetto, "*A review of fault models for LSI/VLSI devices*," Software Microsys., Vol. 2, pp. 44–53, Apr. 1983.

[9] G. R. Case, "*Analysis of actual mechanisms in CMOS logic gates*," Proc. Design Automation Conf., pp. 265–270, 1976.

[10] C. Timoc, M. Buehler, T. Griswold, C. Pina, F. Stott and L. Hess, "*Logical models of physical failures*," Proc. IEEE Intl. Test Conf., pp. 546–553, Nov.1983.

[11] J. P. Hayes, "*Fault modeling*," IEEE Design and Test, Vol. 2, pp. 88–95, Apr. 1985.

[12] J. W. Bandler and A. E. Salama, "*Fault diagnosis of analog circuits*," Proc. IEEE, Vol. 73, pp. 1279–1325, Aug. 1985.

[13] P. Lamoureux and V. K. Agrawal, "*Non-stuck-at fault detection in nMOS circuits by region analysis*," Proc. Intl. Test Conf., pp. 129–137, 1983.

[14] R. Rajsuman, Y. K. Malaiya and A. P. Jayasumana, "*On accuracy of switch level modeling of bridging faults in complex gates*," Proc. 24th IEEE/ACM Design Automation Conf., pp. 244–250, June 1987.

[15] Y. K. Malaiya, A. P. Jayasumana and R. Rajsuman, "*A detailed examination of bridging faults*," Proc. Intl. Conf. on Computer Design, pp. 78–81, 1986.

[16] Y. K. Malaiya, Bidyut Gupta, Anura P. Jayasumana, Rochit Rajsuman, Sankaran Menon and Shoubao Yang, "*Functional Fault Modeling for Elementary Static Storage Elements*," IEEE Computer Society 12th Annual IEEE workshop on design for testability, April 18–21, 1989.

[17] C. C. Beh, K. H. Arya, C. E. Radke and K. E. Torku, "*Do stuck fault models reflect manufacturing defects?*," Proc. IEEE Test Conf., pp. 35–42, Nov. 1982.

[18] S. M. Menon, A. P. Jayasumana and Y. K. Malaiya, "*Fault Modeling of ECL devices*," Electronics Letters, pp. 1105–1108, July 1990.

[19] S. M. Menon, Y. K. Malaiya and A. P. Jayasumana, "*Fault Modeling and Testable Design of 2-level Complex ECL Gates*," Proceedings of the 4th CSI/IEEE Intl. Symp. on VLSI Design, pp. 23–28, Jan. 1991.

[20] S. M. Menon, A. P. Jayasumana and Y. K. Malaiya, "*On Bridging Faults in ECL Circuits*," Proceedings of the 5th CSI/IEEE Intl. Symp. on VLSI Design, pp. 55–60, Jan. 1992.

[21] S. M. Menon, A. P. Jayasumana, Y. K. Malaiya and D. Clinkinbeard, "*Modeling and Analysis of Bridging Faults in Emitter Coupled Logic (ECL) Devices*," IEE Proceedings, Part E: Computers and Digital Techniques, Vol. 140, No. 4, pp. 220–226, July 1993.

[22] C. Morandi, L. Niccolai, F. Fantini and S. Gaviraghi, "*ECL Fault Modelling*," IEE Proc. Part E, Computers and digital techniques, pp. 312–317, Nov 1988.

[23] N. Kanopoulos and N. Vasanthavada, "*Testing of DCVS Circuits*," IEEE Journal of Solid State Circuits, Vol. 25, No. 3, pp. 806–813, June 1990.

[24] J. A. Coekin, *High Speed Pulse Techniques*, Pergamon Press, New York, pp. 170–172.

[25] S. M. Menon, A. P. Jayasumana and Y. K. Malaiya, "*Modeling of Faults in Emitter Coupled Logic (ECL) Devices*," Technical Report, Dept. of Electrical Engineering/Computer Science, Colorado State University, 1990.

[26] M. Abramovici, M. A. Breuer and A. D. Friedman, *Digital Systems Testing and Testable Design*, Computer Science press, pp. 110-123, 1990.

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