Guest Editorial

Special Issue on Hardware Accelerators for VLSI Design

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The complexity of VLSI systems is now in a few millions of transistors per chip and is continuously increasing. In addition, the increasingly high speed of operation, lowering power supply voltage and on-chip integration of analog and digital circuits present new challenges to the computer-aided design of VLSI systems. Improved approaches are needed to reduce the enormous execution times in VLSI design tasks such as logic and analog simulation, fault simulation and test pattern generation, design rule checking, automatic placement and routing, and synthesis etc.

One possible approach to speeding up the VLSI design automation task is to parallelize it and use a general purpose parallel computer to execute it efficiently. Considerable effort is being devoted to this approach recently. Another approach, made feasible by the high density VLSI design itself, is to implement the compute intensive parts of a VLSI computer-aided design algorithm directly in Silicon. This chip is then used as an attached special-purpose processor to the workstation on which the design automation task is being carried out.

An existing algorithm's implementation in hardware may not always result in a considerable improvement in execution time. Thus new algorithms, which yield better parallelism and execution efficiency when implemented in hardware, need to be investigated. This special issue relates to this exciting

field and presents five papers with new approaches in accelerating logic and fault simulation, design rule checking and use of FPGAs in accelerating design automation tasks. Following is a brief summary of each of the five papers in this special issue.

An Evaluation of Parallel Synchronous and Conservative Asynchronous Logic-Level Simulations: Ausif Mahmood and William I. Baker

The authors analyze the available parallelism in synchronous and conservative asynchronous logic-level simulation schemes. A recent paper by Bailey had concluded that the idealized execution times of unit-delay, synchronous and conservative asynchronous logic simulations are equal under some restrictive conditions. However, by extending the analyses to multi-input, multi-output circuits with an arbitrary number of events, the authors in this paper show that the conservative asynchronous simulation extracts more parallelism and executes faster than synchronous simulation in general. Although the overhead associated with asynchronous simulation (maintaining input queues in each logic element etc.) is higher than synchronous simulation which makes it unattractive for software implementations, the work in this paper shows that it has high potential for hardware acceleration of logic simulation.

An Integrated Hardware Array for Very High Speed Logic Simulation: E. Scott Fehr, Stephen A. Szygenda and Granville E. Ott

This paper presents a massively parallel grid-connected architecture for accelerating unit delay, binary-valued logic simulation. In this design, a single netlist gate is mapped to a PE. The fundamental building block chip contains 256 PE cells arranged as two push-pull rows of 128 PEs each. Sequences of stimulus patterns can be executed at full speed in a pipeline fashion by replicating the fundamental chip so that the number of rows is as great as the depth of the leveled netlist. Overall the authors show that in this new design a multiple order of magnitude cost-performance advantage is gained over existing approaches.

A Hardware Accelerator Array for Fault Simulation utilizing a Reconfigurable Array Architecture: Sungho Kang, Youngmin Hur and Stephen A. Szygenda

This paper presents a new approach to massively parallel fault simulation. It uses a 2-D reconfigurable array of simple processing elements along with a new fault simulation algorithm. The basic mapping concept of the new architecture is a one-netlist-node-per-array-element representation of the circuit and it uses pass-gate logic for array inter-connections. The new algorithm expands all multi-input gates with more than two inputs to at most two inputs per gate. This allows the faults to be uniformly distributed on the PE array. Simulation results, based on benchmark circuits, indicate that the hardware accelerator developed in this paper would be orders of magnitude faster than a software simulation program on a workstation.

The Use of Field-Programmable Gate Arrays for the Hardware Acceleration of Design Automation Tasks: Neil J. Howard, Andrew M. Tyrrell and Nigel M. Allinson

This paper investigates the possibility of using FPGAs as reconfigurable attached processors for work-

stations to speed up design automation tasks. The recent availability of high density, low cost and high speed FPGAs allows design automation tasks to be implemented in hardware and to be upgraded easily as the FPGA technology advances. In addition, the static RAM based FPGAs allow for reconfigurable co-processors that can accommodate the diversity and dynamic nature of design automation tasks. The authors explore the use of FPGAs for acceleration of logic simulation and design rule checking. However, only modest speedups are reported. Some reasons for this low speedup and possible solutions are explained.

Hardware Design Rule Checker using a CAM Architecture: Seokjin Kim and Ramalingam Sridhar

This paper presents a hardware implementation of the design rule checker using a specialized Content Addressable Memory (CAM). The system is based on the raster scan method for the designs in Manhattan geometry. It consists of a rule set table and a pixel preprocessor. The rule set table uses a specialized CAM to reduce the number of memory references and to eliminate external logic comparisons. The simple architecture of the system allows low cost implementation.

Authors' Biographies

Ausif Mahmood is currently an associate professor in the department of Computer Science and Engineering at University of Bridgeport. He holds a B.S. in electrical engineering from university of engineering and technology Lahore, Pakistan and M.S. and Ph.D. degrees in electrical engineering from Washington State University. His research interests are in CAD for VLSI, computer architecture and parallel processing.