

Operational and Test Performance in the Presence of Built-in Current Sensors

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The effects of Built-In Current Sensors (BICS) on I_{DDQ} measurements as well as on the performance of the circuit under test are considered. Most of the Built-In Current Sensor designs transform the ground terminal of the circuit under test into a virtual ground. This causes increases in both propagation delay and I_{DDQ} sampling time with the increase in the number of gates, affecting both test as well as operational performance. The effects that current sensors have on the operational and test performance of a circuit are considered. Circuit partitioning may be used for overcoming the effects of BICS on I_{DDQ} measurements as well as on the performance of the circuit under test.

Keywords: I_{DDQ} testing, built-in current sensors, chip partitioning

1. INTRODUCTION

The use of leakage current measurement to detect faults in CMOS ICs has been under consideration for a number of years [1]. Recent studies on leakage current based testing techniques [2,3], have concluded that it is necessary to include I_{DDQ} monitoring to obtain highly reliable CMOS ICs. The data presented for four sample CMOS ICs showed that the defect detection increased between 60% to 180% when I_{DDQ} monitoring is added to a functional test set [2]. I_{DDQ} testing was demonstrated to reduce line fallout after 99.6% stuck-at fault testing failed to achieve desired quality goals [4].

I_{DDQ} testing is performed using either an external or a Built-In Current Sensor(BICS). The implementa-

tion of built-in current sensors has received a lot of interest in recent years. Built-in current sensors have an advantage over external sensors in terms of test speed. They also exhibit some drawbacks in terms of increases in propagation time (t_{pd}) as well as settling time (t_s) affecting both operational and test performances. Built-in current sensors are normally connected in series with the circuit under test and the power supply. This results in the ground terminal of the CUT becoming a virtual ground rather than a physical ground. As the virtual ground may not be at the same potential as the physical ground, the capacitance of the ground rail of the CUT assumes an important role. This capacitance consists of the lumped capacitance of the source terminals of all transistors

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as well as the capacitance associated with the wiring. This phenomenon causes an increase in settling time (t_s), thus slowing the I_{DDQ} testing process. The voltage difference between the virtual and physical grounds may also cause an increase of the propagation delay, thus affecting the normal operational performance of the circuit. In this paper, we present the limitations of BICS which rely on a virtual ground, which in turn affects the operational and test performance of the circuit under test (CUT).

In Section 2, we review the research on current testing. In Section 3, we discuss some of the existing built-in current sensor designs. Section 4 covers the dependence of I_{DDQ} testing on circuit size, where an upper bound on the number of gates in a partition for distinguishing faulty and normal I_{DDQ} values is given. Subsections 4.2 and 4.3 deal with effects of BICS on test speed and operational performances respectively. The importance of partitioning large circuits for I_{DDQ} testing is discussed in Section 5. Finally, conclusions are given in Section 6.

2. BACKGROUND

There are several reasons for using I_{DDQ} monitoring for testing ICs [5], [6]. Traditional IC testing techniques are not effective in detecting a number of failure modes in CMOS ICs. In general, faults such as gate oxide shorts [5], [7]–[11], certain bridging faults [12]–[15], certain open faults, stuck-on faults [8], punch-through faults, operation induced faults [16], parasitic devices, pn junction leakage, and abnormally high contact resistance may not manifest themselves as logic faults and therefore may not be detected by traditional tests which monitor the output logic levels. These localized defects degrade the electrical performance of the circuit without affecting its logical operation. Parametric faults such as incorrect threshold voltage, excessive parasitics, etc., are also difficult to detect by traditional test techniques, and often affect circuit signal delays as well as the power consumption. Implementing I_{DDQ} testing prior to

burn-in has resulted in a significant decrease in the fall-out [6].

A major fraction of failures caused by circuit fatigue will first appear as parametric drifts. Progressive gate oxide leaks, for example, may not initially affect the functionality of a device, but could become shorts within a short time, leading to the failure of a device [8]. Eventually, some of them will advance enough to alter the logical behavior or become circuit failure. Leakage current based testing will detect these parametric drifts before they actually change the circuit behavior. Data exists that shows that devices that fully pass the logic functional tests but fail the I_{DDQ} tests, fall into a significant category of devices that functionally fail more frequently in early life than normal [5].

Current testing also is an invaluable tool for detecting faults in devices that contain both analog and digital functions on a single substrate [17]. In the near future, a large fraction of devices are expected to combine both digital and analog functions on a single substrate [18].

Off-chip current testing has several other advantages over traditional functional testing techniques [1]. In functional testing, the site of a fault has to be excited and the effect of the fault has to be propagated to an output. In I_{DDQ} testing, the propagation of the effect is automatic. Further, it can provide transistor level resolution as opposed to gate level resolution. Off-chip current testing has proved to be very efficient for circuits like static RAMs [19].

Most of the gate oxide shorts cannot be modeled as stuck-at faults, especially for transistors with $W/L \gg 1$ [20], where W and L are Width and Length respectively, of the transistors. The use of current measurement techniques to find gate oxide leaks is investigated in [21], and techniques are presented to test quiescent I_{DD} to a $1 \mu\text{A}$ limit on every clock phase of a functional test. It also identifies several problems associated with the measurement of I_{DDQ} . The current drawn by I/O circuits for example, can mask the current drawn by a fault. Other problems identified include wideband noise across the load capacitance, dielectric absorption in output pads, input capacitance offered by the V_{DD} pin, and the presence of mixed

logic and redundant cells. To overcome these problems, the use of several techniques during the design of ICs have been proposed, including the use of separate V_{DD} pins for output buffers and internal logic.

Stuck-on faults in CMOS circuits cannot be detected using traditional functional fault testing techniques. Test generation for the detection of such faults, when I_{DDQ} testing is used, is considered in [22]. Different decision processes involved in detecting such faults have been examined. The voltage level in the presence of stuck-on or bridging faults in CMOS circuits depends on the relative impedances of the transistors involved and the bridge [23]. This makes detection of such faults difficult using voltage measurement techniques. However, I_{DDQ} testing detects such faults. It has been shown that I_{DDQ} testing also detects multiple stuck-at faults as well as logically redundant faults [23], [24].

Most of the research in this area considers the use of I_{DDQ} measurement techniques for detection of faults in CMOS circuits. This can be attributed to the fact that the static quiescent current drawn by a CMOS circuit is very small and therefore the detection of a fault which increases the I_{DDQ} is relatively easy to detect. With technologies such as nMOS and TTL, the quiescent current can be fairly large, and the increase in current drawn due to a fault may not be significant enough to be detected by measuring equipment. Even so, current testing techniques have been successfully used to detect faults in TTL circuits [25]. The faults that have been detected include open circuits, stuck-at faults and multiple faults. The supply current measurement has been supplemented in [26] with the measurement of the low frequency noise in the supply current, the circuit delay as a function of the supply voltage, the transient current as the circuit switches between states, and the noise in the transient current to provide an indication of an incipient failure in CMOS integrated circuits.

One obstacle for commercial acceptance of current testing of ICs has been the relatively slow measurement rate compared to normal logic testing. Typically, current testing is done at a rate less than 100K test patterns per second [21], whereas functional testing can be carried out at the normal operating fre-

quency of the device under test. The speed of IDDQ testing is limited by several factors. The width of the transient current pulse, the loading of the VDD pin due to output buffers and the impedance of the probing circuitry are some of them. It has been demonstrated that the rate of testing can be increased by several orders of magnitude by isolating the output buffers of an IC from the VDD pin [2].

The high resolution required for current testing has been cited as a problem that makes acceptance of current testing difficult at present [3]. The key to performing an effective I_{DDQ} test is the probe circuit used to measure the current. Such a circuit should be capable of measuring small currents, without affecting the supply voltage, especially during transients, and must be capable of fast measurements [27]. The different types of current probes in use are examined in [27], and a probe circuit has been proposed which allows a system to perform dynamic I_{DD} tests as an integral part of the functional testing of a CMOS device.

Built-in current sensing techniques have been proposed to overcome the disadvantages of existing off-chip current testing techniques. Current sensors have been proposed and implemented using CMOS technology, some capable of detecting currents as small as $2\mu\text{a}$ at 1MHz clock frequency [5]. In BIC testing, an IC is implemented using a number of modules and each module is connected to the power supply through a current sensor. Another circuit design for built-in current testing has recently been proposed [28]. The output of the current sensor of a module is observed with the proper input vectors to detect faults in that particular module.

3. BUILT-IN CURRENT SENSORS

The simplest current sensor can be built with either a resistive [3] or a capacitive [29] element (labeled by 'X' in Figure 1) along with a voltage comparator, as shown in Figure 1. The current flow I , will cause a voltage drop across the element X and the voltage on X is fed to the comparator [27], [29]. The other input

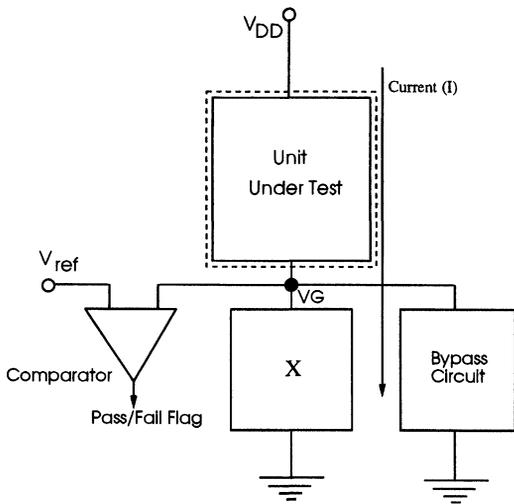


FIGURE 1 A general current sensor.

of the comparator is the standard voltage (V_{ref}), which is the reference voltage. Therefore, if the measured current I_{DDQ} is greater than I_{DDQth} (I_{DDQ} threshold, which is set by the V_{ref}), the output of the current sensor is 1. If I_{DDQ} is smaller than I_{DDQth} , the output of the current sensor is 0.

Various current sensors have been proposed [3, 27, 28, 29]. The BICS proposed by Maly, et. al. [3], is based on a non-linear resistance placed in the power supply current path. The exponential I-V characteristics exhibited by the non-linear resistance causes distinguishable voltage drop for a wide range of currents. The output of the current sensor distinguishes between the normal and abnormal quiescent currents by comparing the voltage drops with a reference voltage.

One of the current sensor circuits proposed by Rubio, et. al. [29], uses a capacitor instead of the non-linear resistance. Several schemes for current measurement are given in [27]. A circuit for built-in current testing presented in [28] measures the integral of the current during a certain time interval. The measured value of the current is used to decide if the circuit under test is fault-free or not.

In almost all of the BICS designs, the circuit under test is connected in series with the built-in current sensors in a manner such that the power supply

ground terminal is connected to the BICS input. The bypass circuit generally is made up of an nMOS transistor which provides a path for the ground terminal of the circuit under test to the physical ground, under normal operation. In the BICS proposed by [3], the bypass circuit is formed by an nMOS transistor and the base to emitter junction of a bipolar transistor. This results in the ground terminal of the CUT being a virtual ground. Limitations on the I_{DDQ} measurements due to virtual grounds are given in the next section.

4. DEPENDENCE OF I_{DDQ} TESTING ON CIRCUIT SIZE

When the circuit size is small, distinguishing the difference between normal and faulty I_{DDQ} values is not difficult. When the circuit size becomes large, it becomes hard to detect a fault using I_{DDQ} monitoring as the distinction between normal and faulty current becomes difficult to differentiate. Furthermore, the larger the circuit size, the more significant the effect of BICS on the operation speed and the test speed of the circuit will be. Below, we describe several factors regarding the effect of BICS on circuit operation and testing. The solution to this problem will be to partition the device under test into smaller modules. Each of the partitions will have its own current sensor. Partitioning to distinguish the difference between normal and faulty I_{DDQ} values is discussed in this section. The effects of BICS on test speed and on operational performance with increasing circuit size is covered in this section.

4.1 Difference between Normal & Faulty I_{DDQ} Values

A statistical characterization of faulty and fault-free I_{DDQ} distributions is presented in [30, 31]. The distinction between the distributions of normal and faulty I_{DDQ} is easy if the distributions are well separated. If the number of gates in a circuit is small, then

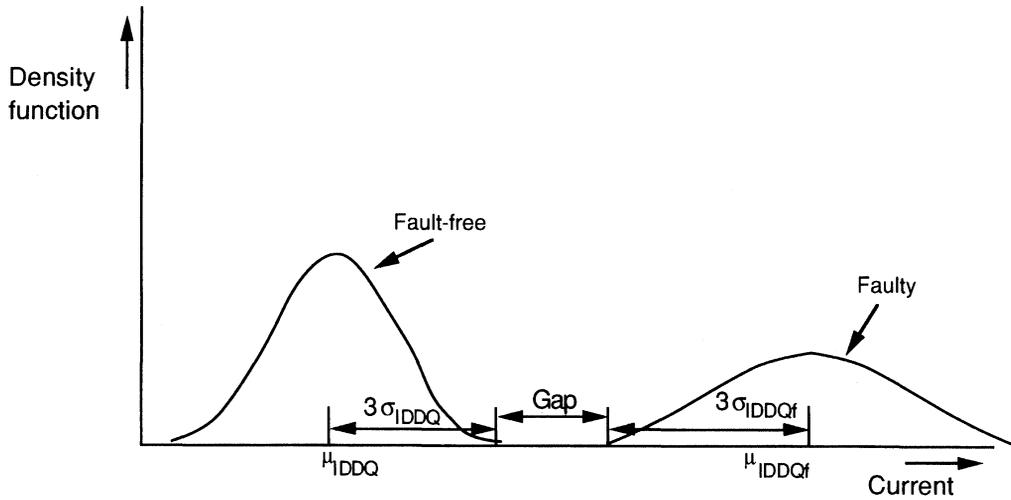


FIGURE 2 The 'gap' between fault-free and faulty value of I_{DDQ}

the distributions between normal and faulty I_{DDQ} are well separated and thus the fault is detectable. The separation or *gap* between the distributions for normal and faulty I_{DDQ} is given below [30, 31]. The same equation for the gap applies for each module:

$$gap = \mu_{if} - 3(\sqrt{n\sigma_{iADDQ}^2 + \sigma_{if}^2} + \sqrt{n}\sigma_{iADDQ}) \quad (1)$$

where n is the number of cells in one module, μ_{if} and σ_{if} are the mean and standard deviation of the additional quiescent supply current (i_p), and σ_{iADDQ} is the standard deviation of the current through an average cell. Figure 2 shows the gap or the separation between the two distributions.

As the number of gates in a circuit increases, the spread of the current distributions, both faulty and fault-free, increase making the distributions overlap. The spreading of the distributions occurs due to the variations in circuit parameters over different gates in an IC [30]. The above expression illustrates the basic problem in testing large devices. To use I_{DDQ} testing in the presence of this phenomenon, the size of each module connected to a BICS has to be such that the faulty and fault-free distributions within each module can be distinguished.

Monte Carlo simulations of CMOS circuits with 10, 50, 100 and 1000 gates were obtained. T_{ox} (oxide thickness) and $NSUB$ (substrate doping) were used as the random variables for the Monte Carlo simulations with a variation of $\pm 10\%$ and a normal distribution. Monte Carlo simulations for a circuit of 1000 inverters with 100 runs is shown in Figure 3. In the follow-

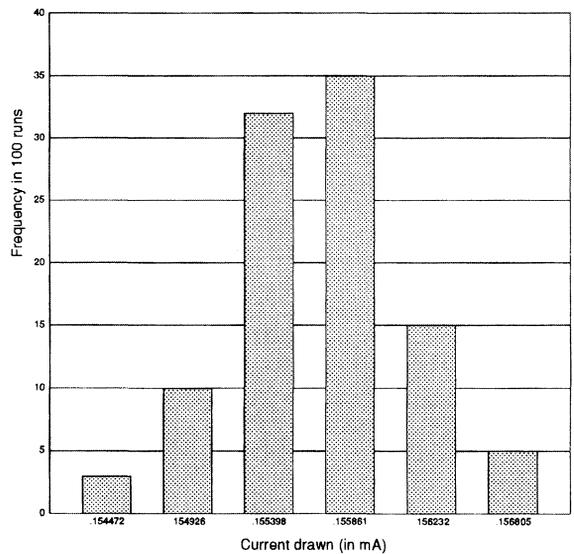


FIGURE 3 Histogram of faulty current with 1000 gates.

ing analysis, we approximate the distribution using a gaussian distribution.

Let us assume that the maximum size of each module is determined by letting *gap* be 0. Although we have to use numerical methods to obtain the exact value of *n*, we can derive the upper bound of *n* as follows:

$$\mu_{if} = 3(\sqrt{n\sigma_{iADDQ}^2 + \sigma_{if}^2} + \sqrt{n}\sigma_{iADDQ}) \geq 6\sqrt{n}\sigma_{iADDQ} \tag{2}$$

From the above equation, the upper bound of the maximum *n*, denoted by *n_b* is given as:

$$n_b = \left(\frac{\mu_{if}}{6\sigma_{iADDQ}}\right)^2, \tag{3}$$

where *n_b* is the number of cells covered by a current sensor. Hence, the device can be partitioned into modules whose sizes will not exceed *n_b*, and all the modules will have approximately the same number of

cells. The above criterion ensures that the distributions of the normal and faulty *I_{DDQ}* are separated and distinguishable.

Here, we are not considering the sensitivity of Built-in Current Sensors, which depends on the test frequency being used [32]. A higher test frequency will result in lower available resolution of the current sensor which will affect the partitioning size [33].

4.2 Effects of BICS on Test Speed

Another reason for partitioning the device into several modules is that the larger the device or circuit becomes, the larger the capacitance seen at the current sensor input (node *VG* in Figure 1). So, it will take a longer period for the current sensor to respond to the value of the current flow in the circuit. The speed is limited due to the fact that the current monitoring has to be done after the transients have settled. The duration of the transients will depend, among other things, on the capacitance associated with mea-

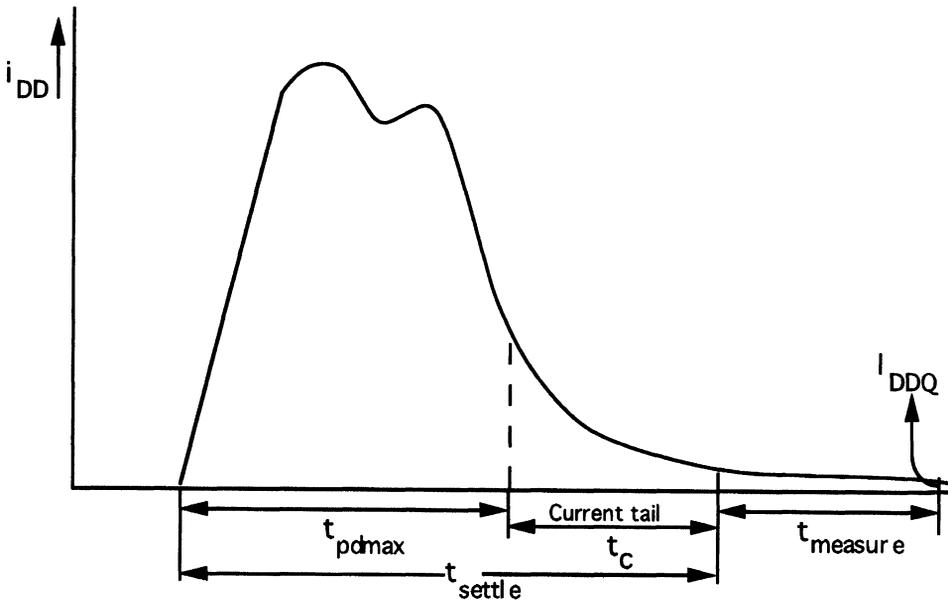


FIGURE 4 Plot illustrating Power Supply Current vs. Time for a CMOS circuit.

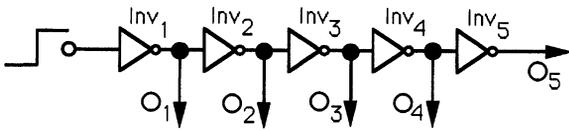


FIGURE 5 An inverter chain with 5 inverters.

surement points. Thus, the larger the circuit that is covered by a current monitor, the longer the settling time of the transient.

For I_{DDQ} monitoring, the measurement of the supply current has to be performed by the current sensor after the initial transients have settled. Figure 4 shows a plot of I_{DD} vs. Time for a typical CMOS circuit. t_{pdmax} is the maximum propagation delay of the circuit under test. t_{pdmax} is caused due to the initial transients in the supply current due to switching in the various gates of the CMOS circuit. It takes a certain amount of time (t_c) for the current tail to end, i.e., the current to settle to an almost constant value of the order of pico or nano Amps in a fault-free CMOS circuit. In a faulty CMOS circuit, the value of I_{DDQ} can be a few orders of magnitude greater than the fault-free I_{DDQ} value. The total time taken for the current to settle, t_{settle} , is the sum of t_{pdmax} and t_c .

Consider the inverter chain consisting of five inverters shown in Figure 5. Input/Output waveforms

along with the current waveform, I_{DD} , obtained using SPICE simulations are shown in Figure 6. The input pulse applied to the inverter chain is marked on the plot. Output signals O_1, O_2, \dots, O_5 are the respective output signals of inverters $inv_1, inv_2, \dots, inv_5$. The current drawn by the circuit is shown by dark line with the axis on the right side of the plot. The current waveform shows almost $\approx 0.4\text{mA}$ current drawn by the 5 inverter chains when the gates are switching. The last gate, Inv_5 , switches around 9.2ns , shown as t_{pd} in the plot. After the last gate switches, the current goes to a steady, low current in a fault-free CMOS circuit. The time from when the last gate switches, t_{pdmax} , until the current reaches the steady low current value is termed as t_c . The sampling of the supply current can be done any time after the current tail has reached the almost fixed, very low value of current in the fault-free CMOS circuit. If the CMOS circuit is faulty, then the current at this time would be elevated and hence the BICS would be able to detect the fault. This results in a settling time of $t_{settle} = t_{pdmax} + t_c$.

One of the important parameters to be obtained is the sampling time for a given circuit partition for I_{DDQ} measurement by the BICS. If the sampling of current by BICS is done before the transients have settled, then the BICS would be measuring incorrect, elevated values of switching current. Conversely, if the sam-

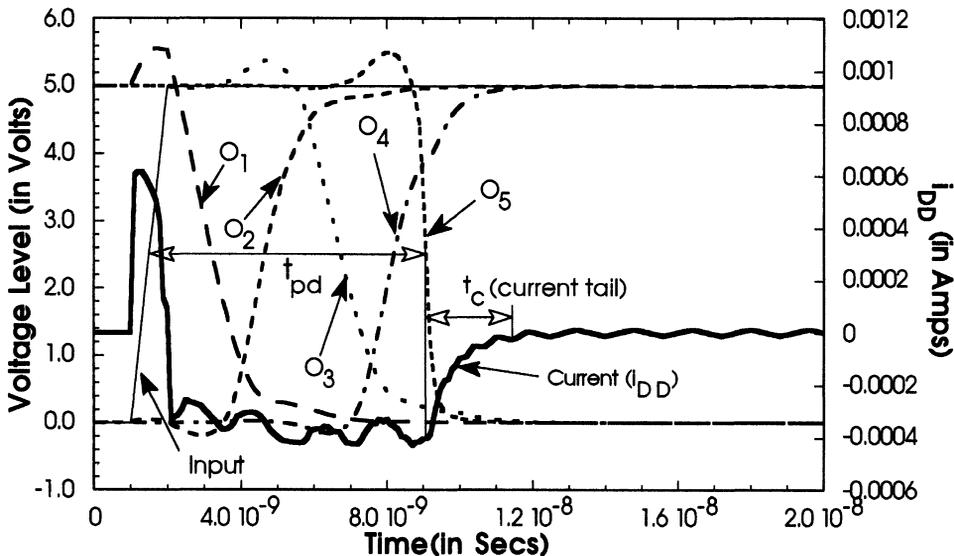


FIGURE 6 Input/Output & current waveforms for inverter chain with 5 inverters.

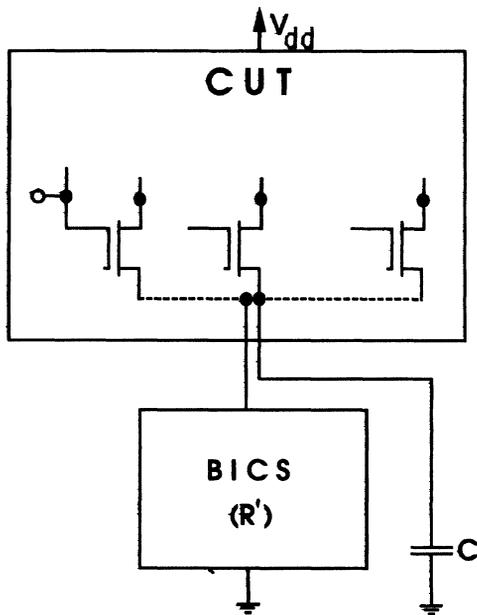


FIGURE 7 CMOS circuit with BICS.

pling is done well after the current has settled to a steady-state value, then the measurement becomes slow. An ideal sampling time for I_{DDQ} would be when the current is within about 5% of the steady-state value. Here, we consider the parameters that govern the settling time of I_{DD} .

One of the components of the settling time, t_{settle} , is t_{pdmax} and the other component is t_c , caused by the current tail. t_{pdmax} can be obtained directly from the maximum propagation delay of the complete chain of gates in a given circuit. The second component, t_c , of the settling time, caused by the current tail, depends on the rise-time (t_r) and fall-time (t_f) of the last few gates of the circuit.

CMOS circuits with varying numbers of gates and levels were simulated using a built-in current sensor (BICS) [3], as shown in Figure 7, to study the settling time of the power supply current. It may be noted that when BICS are implemented, the transistor terminals (source or drain) in a CMOS circuit, which otherwise would have been connected to ground is connected to the BICS. The transistor terminal (source or drain) capacitance of all the transistors appears as one lumped capacitance (C) at the input of the BICS. The

larger the circuit under test (*CUT*), the larger the capacitance seen by the BICS. In the absence of BICS, C is always grounded and therefore has no effect on the performance.

In order to study the effects of varying circuit size on i_{DD} settling time and propagation delay, CMOS circuits having different number of levels of gates (1, 3, 5 and 10) were chosen for simulation with BICS (Built-in Current Sensor). The maximum number of gates cascaded in series between a network input and output is referred to as the number of levels of gates [34], hereafter referred to as the number of levels of the circuit. For example, simulation for 5 levels totaling 1000 gates has 5 gates connected in series with 200 such series of gates in parallel.

Figure 8 shows plots for i_{DD} settling time vs. total number of gates for CMOS circuits having different number of gate levels. In Figure 8, the i_{DD} settling time shown also includes the propagation delay (t_{pd}) for circuits with different number of levels and the time for the current tail (t_c) to settle. It may be noted that i_{DD} settling time for a circuit with 10-levels is greater than that of a circuit with 5-levels, both with the same number of gates, due to the greater amount of propagation delay in the former. Simulation results for up to 1000 gates are shown in Figure 8.

Figure 9 shows plots for i_{DD} settling time vs. number of gate levels for circuits with various gate counts. In practice, the current is sampled by the BICS only after all the transients due to switching have died down and the current has settled to a steady, low current value [3]. The settling time shown in Figure 9 shows the time when the current has settled to within 5% of the steady, low current value for sampling by the BICS. The settling time for a 10-level circuit, for example, is greater than that of a 5-level circuit with the same number of gates due to the larger propagation delay in the former. For a circuit with a given number of gates, the settling time increases with the increase in the number of levels. For example, for a circuit with 100 gates, the settling time for 3 levels is 10.21 ns and the settling time for 5 levels is 17 ns. The settling time thus has two components, one due to the propagation delay, and the other due to the capacitance at the node to which the current sensor is connected. Thus the

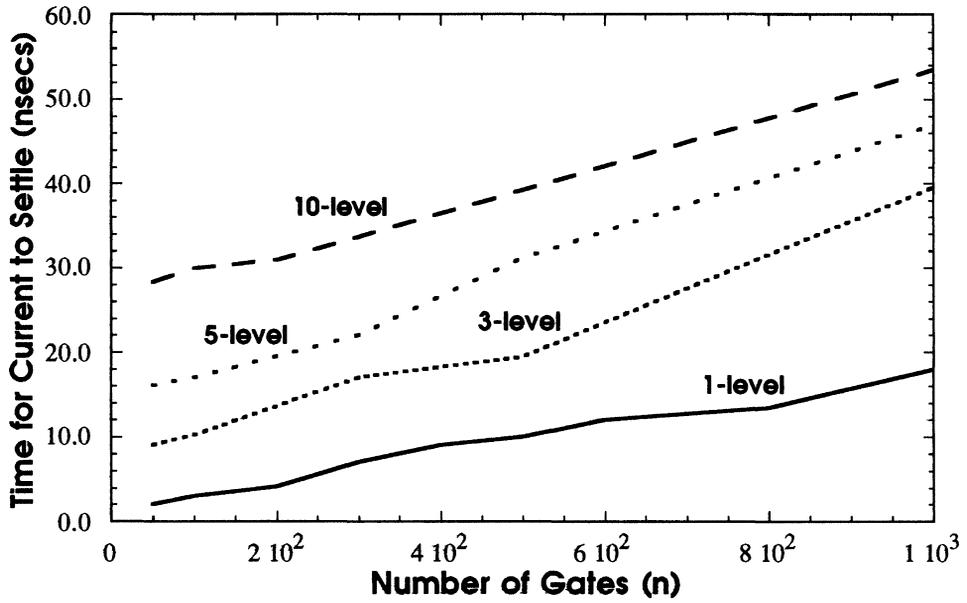


FIGURE 8 i_{DD} settling time vs. Number of gates for different levels.

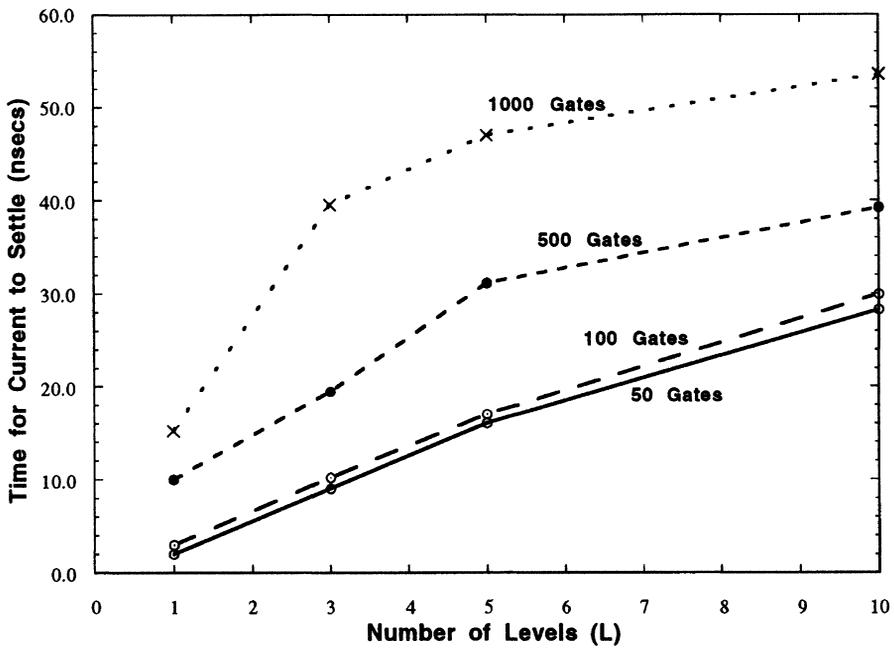


FIGURE 9 i_{DD} settling time vs. Number of Levels for various gate counts.

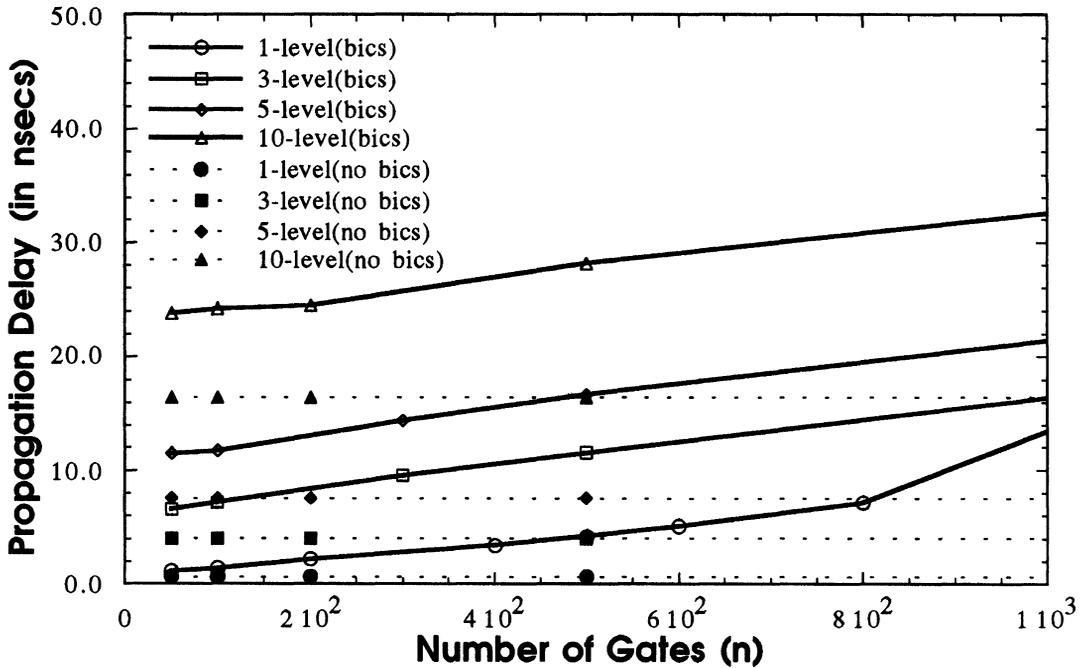


FIGURE 10 Propagation delay t_{pd} vs. Number of gates for different levels.

larger the circuit that is covered by a current monitor, the longer the second component of the transient time will be. Another advantage of partitioning is the reduction of this component of settling time due to the total capacitance.

4.3 Effects of BICS on Circuit Performance

The bypass circuit of the BICS offers a finite resistance (R') which effectively appears in series with the circuit under test (CUT). This may not cause a significant problem under test conditions. However, under normal operation, the resistance of the BICS appears in series with the CUT and causes an IR' voltage drop across the BICS. The voltage drop in the BICS causes the effective ground potential of the CUT to be higher than the physical ground, especially during the transitions, thus slowing down the circuit operation.

The propagation delay (t_{pd}) component from the input to the output of circuits with different levels (1, 3, 5 and 10 levels) with different gate count with the

implementation of BICS and without the implementation of BICS is shown in Figure 10. The propagation delay (t_{pd}) for circuits with different numbers of gate levels (1, 3, 5 and 10) remains fixed with increasing number of gates in the circuit, when BICS is not implemented. For example, the propagation delay (t_{pd}) for 1-level, 3-level, 5-level and 10-level (shown dotted in Figure 10) are 0.66ns, 4.04ns, 7.58ns and 16.4ns respectively even with increasing number of gates (n), for the case without BICS.

The propagation delay (t_{pd}) for the different levels (1, 3, 5 & 10 levels) with BICS implementation is shown in Figure 10 as solid lines. It may be noted that the propagation delay (t_{pd}) for a given circuit with BICS implementation is greater than that when BICS is not implemented. Also, the propagation delay (t_{pd}) increases with increase in the number of gates as the capacitance seen by BICS increases with increasing number of gates (transistors). Table I summarizes the settling time (t_{settle}), propagation delay (t_{pd}) and time for the current tail to settle (t_c) for 1, 3, 5 and 10-levels for different gate counts, with and without BICS implementation. The settling time

TABLE I i_{DD} settling time vs. # of levels for various gates

| # of levels | Total Number of Gates | | | | | | | | | | | |
|------------------------|-----------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| | 50 | 50 | 50 | 100 | 100 | 100 | 500 | 500 | 500 | 1000 | 1000 | 1000 |
| | t_p (ns) | t_c (ns) | t_s (ns) | t_p (ns) | t_c (ns) | t_s (ns) | t_p (ns) | t_c (ns) | t_s (ns) | t_p (ns) | t_c (ns) | t_s (ns) |
| 1-Level(with BICS) | 1.15 | 0.877 | 2.0 | 1.41 | 1.59 | 3.0 | 4.22 | 5.79 | 10.01 | 13.46 | 4.50 | 15.23 |
| 1-Level(without BICS) | 0.66 | | | 0.66 | | | 0.66 | | | 0.6 | | |
| 3-Level(with BICS) | 6.6 | 2.42 | 9.02 | 7.22 | 2.99 | 10.21 | 11.57 | 7.89 | 19.46 | 16.4 | 23.16 | 39.56 |
| 3-Level(without BICS) | 4.04 | | | 4.04 | | | 4.04 | | | 4.04 | | |
| 5-Level(with BICS) | 11.51 | 4.55 | 16.06 | 11.76 | 5.24 | 17.0 | 16.71 | 14.41 | 31.12 | 21.42 | 25.58 | 47.0 |
| 5-Level(without BICS) | 7.56 | | | 7.56 | | | 7.56 | | | 7.56 | | |
| 10-Level(with BICS) | 23.8 | 4.46 | 28.26 | 24.19 | 5.73 | 29.92 | 28.19 | 11.02 | 39.21 | 32.62 | 20.88 | 53.5 |
| 10-Level(without BICS) | 16.4 | | | 16.4 | | | 16.4 | | | 16.4 | | |

(t_{settle}) of current for a given CMOS circuit as shown in Figure 8 is a function of the following:

$$t_{settle} = mt_{pd} + f(R', C, D_{pd}, t_r, t_f)$$

where

- t_{pd} = propagation delay per gate,
- m = the maximum number of levels in a given CMOS circuit,
- C = total capacitance of the V_{DD} or Ground rail of CUT connected to BICS,
- R' = denotes the effect due to BICS resistance,
- t_r, t_f = rise-time, fall-time of the gate switching towards the end.

With the above results, the partitioning of a given circuit becomes very critical as the capacitance at the input of BICS also needs to be considered, in addition to the voltage drop across the BICS and resolution of the BIC sensor. Partitioning the circuit under test into smaller modules reduces the amount of capacitance seen by the BICS. Partitioning reduces the settling time, which in turn helps in performing faster sampling of I_{DDQ} measurements. The effect of the increase in settling time (t_s) with increasing numbers of gates for a given level due to the capacitance (C) is a problem for all BICS designs which rely on virtual ground.

The effect of the lumped capacitance (C) of the circuit and the non-linear resistance (R') of the BICS results in additional propagation delay for the CMOS circuit. This is a problem affecting the operational performance of the circuit caused by BICS. This can

be avoided by providing a physical ground pin in addition to the virtual ground pin. This allows the ground pin to be connected to the ground terminal of the system and hence avoids the propagation delay introduced in the circuit by the BICS. This scheme provides for off-line BICS, wherein whenever current sensing is required to be carried out, the BICS is introduced into the circuit by disabling the ground pin and making it a virtual ground. The BICS in this scheme is disabled by connecting the virtual ground terminal to the physical ground, thus avoiding the additional propagation delay introduced due to the capacitance (C). In this scheme, BICS is introduced only during test mode. The off-line BICS scheme suffers the disadvantage of switching the circuit into test and normal modes of operation, thus the inability to monitor the I_{DDQ} drawn by the circuit on-line. For large circuits with many partitions, it may not be practical to add an additional pin for each partition. For example, for a circuit with 10 partitions, at least 10 extra physical ground pins need to be added.

5. BUILT-IN CURRENT TESTING OF PARTITIONED ICS

Since each module or subcircuit has its own current sensor, it is impractical to observe the output of every current sensor. One solution to this problem is to propagate the outputs of all the sensors to one observable output pin which is designed solely for the signature extractor or information compression unit.

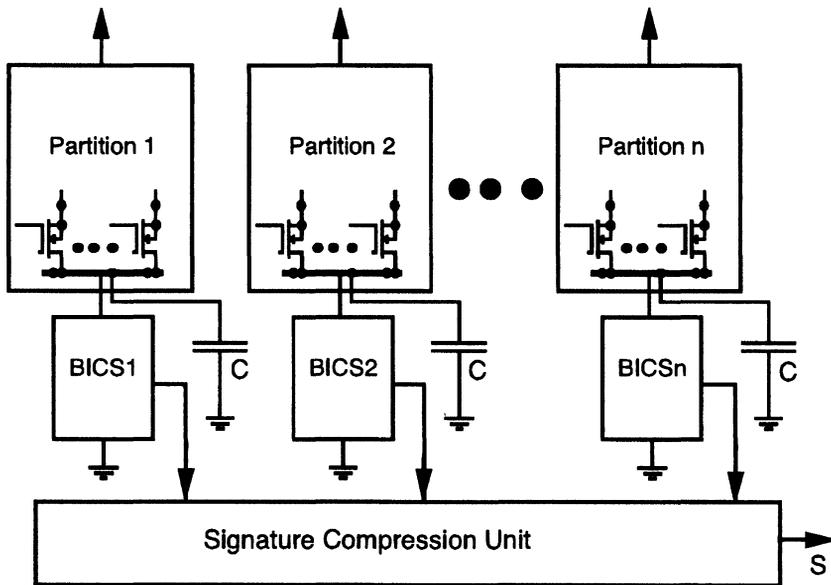


FIGURE 11 Partitioning and information compression.

This information compression unit may be implemented simply by an OR gate. The outputs from all the current sensors are fed to the OR gate. A counter is connected to the output of the OR gate, as shown in Figure 11, to calculate the total number of times that the detected current I_{DDQ} exceeds I_{DDQ}^{th} , which is nothing but the signature S . This signature extractor also works correctly if there is more than one faulty module, since in that case S will be even greater than that when there is only one faulty module.

Figure 11 shows the circuit under test partitioned into n partitions with a BICS for each partition. Capacitor C is the lumped capacitance of the source terminal of all the transistors which otherwise would have been connected to the ground terminal if BICS is not implemented. The capacitance (C) plays a crucial role in affecting both the operational and test performance when BICS is implemented.

6. CONCLUSIONS

Testing of larger ICs using I_{DDQ} monitoring requires larger test times and provides lower resolution between faulty and fault-free devices. Most of the

Built-In Current Sensor (BICS) designs transform the ground terminal of the circuit under test to a virtual ground. It is shown that this causes increased delay with increasing number of gates. Performance degradation of the circuit under test due to increased delay with increasing gates is shown. Careful partitioning of large circuits may be required to reduce the effects of virtual ground caused by BICS. An expression for upper bound of the maximum cells (n_b) covered by a current sensor is given. Partitioning of large circuits as well as forcing the virtual ground to physical ground using an additional pin may help minimize the limitations of BICS on the performance of circuit under test. Monte Carlo simulation suggests that we can approximate the distribution for the current drawn by the device using a Gaussian distribution.

Acknowledgements

This research was supported by a SDIO/IST funded project monitored by the ONR.

References

- [1] Malaiya, Y. K. and Su, S. Y. H. (1982). "A new fault model and testing technique for CMOS devices," *Proc. Int. Test Conf.*, pp. 25–34.

- [2] Hawkins, C. F., Soden, J. M., Fritzscheier, R. R. and Homing, L. K. (1989). "Quiescent power supply current measurement for CMOS IC defect detection," *IEEE Trans. Industrial Electronics*, (May), pp. 211–218.
- [3] Maly, W. and Nigh, P. (1988). "Built in Current Testing—Feasibility Study," *Proc. ICCAD*, pp. 340–343.
- [4] Perry, R. (1992). " I_{DDQ} testing in CMOS digital ASIC's—Putting it all together," *Proc. Int. Test Conf.*, pp. 151–157.
- [5] Baker, K. and Verhelst, B. (1990). "IDDQ testing because 'Zero Defects isn't Enough: A Philips Perspective,'" *Proc. IEEE Int. Test Conf.*, pp. 253–254.
- [6] McEuen, S. (1991). "IDDQ Benefits", *Proc. IEEE VLSI Test Symp.*, pp. 285–290.
- [7] Barrett, C. R. and Smith, R. C. (1976). "Failure Modes and Reliability of Dynamic RAMs," *Proc. Int. Electron Devices Conf. (IEDM)*, (December), pp. 319–322.
- [8] Hawkins, C. F. and Soden, J. M. (1986). "Reliability and Electrical Properties of Gate Oxide Shorts in CMOS ICs," *Proc. IEEE Int. Test Conf.*, pp. 443–451.
- [9] Holland, S., Chen, I., Ma, T. and Hu, C. (1984). "On Physical Models for Gate Oxide Breakdown," *IEEE Electron Dev. Ltr.*, (August), pp. 302–305, Vol. EDL-5, No. 8.
- [10] Hu, C. (1985). "Thin Oxide Reliability," *Int. Electron Devices Conf. (IEDM)*, (December), pp. 368–371.
- [11] Soden, J. M. and Hawkins, C. F. (1989). "Electrical properties and detection methods for CMOS IC defects," *Proc. 1st European Test Conf.*, (April), pp. 159–167.
- [12] Acken, J. M. (1983). "Testing for Bridging Faults (Shorts) in CMOS Circuits," *Proc. IEEE/ACM Design Automation Conf.*, (June), pp. 717–718.
- [13] Ferguson, F. J., Taylor, M. and Larrabee, T. (1990). "Testing for Parametric Faults in Static CMOS Circuits," *Proc. IEEE Int. Test Conf.*, pp. 436–443.
- [14] Malaiya, Y. K., Jayasumana, A. P. and Rajsuman, R. (1986). "A Detailed Examination of Bridging Faults," *Proc. IEEE Int. Conf. on Computer Design*, pp. 78–81.
- [15] Millman, S. D. and McCluskey, E. J. (1988). "Detecting Bridging Faults with Stuck at Test Sets," *Proc. IEEE Int. Test Conf.*, pp. 773–783.
- [16] Rajsuman, R., Jayasumana, A. P., Malaiya, Y. K. and Park, J. (1991). "An analysis and testing of operation induced faults in MOS VLSI," *Proc. VLSI Test Symp.*, pp. 137–142.
- [17] Frenzel, J. F. and Marinos, P. N. (1987). "Power supply current signature analysis: A new approach to system testing," *Proc. Int. Test Conf.*, 125–129.
- [18] Santoni, A. (1987). "Mixed-Signal Devices Create Testing Headaches," *Electronic Test*, (February).
- [19] Meershoek, R., Verhelst, B., McInerney, R. and Thijssen, L. (1990). "Functional IDDQ Testing on a Static RAM," *Proc. IEEE Int. Test Conf.*, pp. 929–937.
- [20] Syrzycki, M. (1988). "Modeling of gate oxide shorts in MOS transistors," *Res. Rep. CMU CAD-88-22*, Carnegie Mellon University, (April).
- [21] Crapuchettes, C. (1987). "Testing CMOS IDD on large devices," *Proc. Int. Test Conf.*, pp. 310–315.
- [22] Malaiya, Y. K. (1984). "Testing stuck-on faults in CMOS integrated circuits," *Proc. Int. Conf. on Computer Aided Design*, pp. 248–250.
- [23] Jha, N. K. and Tong, Q. (1990). "Detection of multiple input bridging and stuck-on faults in CMOS logic circuits using current monitoring," *Computers & Elec. Engg.*, Vol. 16, No. 3, pp. 115–124.
- [24] Fritzscheier, R. R., Soden, J. M. and Treece, R. K. (1990). "Increased CMOS IC Stuck-at Fault Coverage with Reduced IDDQ Test Set," *Proc. Int. Test Conf.*, pp. 427–435.
- [25] Hashizume, M., Yamada, K., Tamesada, T. and Kawakami, M. (1988). "Fault detection of combinational circuits based on supply current," *Proc. Int. Test Conf.*, pp. 374–380.
- [26] Dorey, A. P., Jones, B. K., Richardson, A. M., Russell, P. C. and Xu, Y. Z. (1988). "Reliability testing by precise electrical measurement," *Proc. Int. Test Conf.*, 369–373.
- [27] Keating, M. and Meyer, D. (1987). "A new approach to dynamic IDD testing," *Proc. Int. Test Conf.*, pp. 316–321.
- [28] Miura, Y. and Kinoshita, K. (1992). "Circuit design for built-in current testing," *Proc. Int. Test Conf.*, pp. 873–881.
- [29] Rubio, A., Figueras, J. and Segura, J. (1990). "Quiescent Current Sensor Circuits in Digital VLSI CMOS Testing," *Electronics Letters*, (July), pp. 1204–1206.
- [30] Malaiya, Y. K., Jayasumana, A. P., Tong, Q. and Menon, S. M. (1991). "Enhancement of resolution in supply current based testing for large ICs," *Proceedings of IEEE VLSI Test Symposium*, pp. 291–296.
- [31] Malaiya, Y. K., Jayasumana, A. P., Tong, Q. and Menon, S. M. (1992). "Enhancement of resolution in supply current based testing for large ICs," *Tech. Rep.*, Dept. of Computer Science, Colorado State University, Fort Collins CO.
- [32] Hawkins, C., Gulati, R. and Soden, J. (1991). "Current Monitoring for Efficient Detection of CMOS Defects and Faults," *Tutorial 14*, Presented at the International Test Conference, (October).
- [33] Maly, W. and Patyra, M. (1992). "Built-in Current Testing," *IEEE Journal of Solid-State Circuits*, (March), pp. 425–428.
- [34] Roth, C. H. (1992). *Fundamentals of Logic Design*, pp. 173–208, West Publishers, Fourth Edition.
- [35] Parzen, E. (1960). *Modern Probability Theory and Its Applications*, Wiley.

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