Guest Editorial

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This special issue of the VLSI DESIGN: an International Journal of Custom-chip Design, Simulation and Testing is devoted to the special issue of “High-Performance Design Automation of VLSI Interconnects”. The explosion in complexity of VLSI interconnections has made it increasingly difficult for designers to manually carry out the chip and systems design. Automated synthesis of interconnection behaviours is emerging as a most promising approach to the implementation of large scale systems. Current interconnection level design models lack the capability of capturing important physical design effects such as signal integrity, power, clock, crosstalk, and timing issues which are first order factors in chip performance (especially for large scale deep-submicron designs). Thus, in order to approximate a realistic layout model of signals, the designer must rely on efficient but accurate estimates of the various design matrices throughout the design process. This way, the physical effects can be properly accounted for without incurring an unacceptable penalty in runtime. In order to develop such models of layout, there is a need to address research problems both in synthesis and physical design of interconnects. The purpose of this special issue is to further investigate recent developments in algorithm design and

combinatorial structures to VLSI interconnection applications. Those contributors in this special issue have either been applying algorithmic techniques to cope with the complexity of VLSI systems, or they have been working on algorithmic graph theory and combinatorics and have found a new source of problems in VLSI domain. Specifically, the topics of interest for this special issue include module clustering to improve interconnection delays, performance-driven interconnection, clock network synthesis and physical design, power and ground network synthesis, signal crosstalk minimization transmission line analysis, multilayer wirability and performance-driven FPGA layout designs.

This kind of problems arisen in VLSI interconnection designs are described and their up-to-date techniques are demonstrated in the following 8 papers.

The first paper of this special issue discusses the recent progress in the problem of clustering with more than one implementation per module, which has practical importance. *Karayiannis* and *Tragoudas* propose an approach such that each module has a set of possible implementations with the area and delay of each implementation being different. The authors show the problem is NP-hard. They present a pseudo polynomial time algorithm for the

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case where the network is a tree. The algorithm resembles the classical dynamic programming algorithm for library-based technology mapping of tree networks.

Performance-driven routing has received increasing attention in the last half decade. For a given signal net, the goal of performance-driven routing is to route a net while minimizing average or maximum source to sink delay with allowing tolerable amount of wirelength increase. The second paper by *Tellez* and *Sarrafzadeh* explores such a problem and proposes a effective heuristic that computes a so-called *rectilinear distance preserving tree*. Their algorithm partitions the problem into sub-problems which can be solved optimally in polynomial time.

The third paper, automatic synthesis of high performance clock distribution networks, is proposed by *Neves* and *Friedman*. This paper represents a uniform framework for clock tree synthesis through four design steps: (1) Determine optimal skew schedule using previous algorithms; (2) Given a timing specification, solve a LP to determine optimal localized skews of different clocked elements, and zero clock skew is maintained between chip I/O; (3) Design tree topology based on hierarchical information and use the skew schedule to compute branch delays; (4) Derive a formula to relate load capacitance and slope factor to inverter geometry, then use this formula with the branch delay to determine the inverter geometry.

The synthesis of the power distribution network is an important problem. The fourth paper, power distribution synthesis for VLSI, by *Vittal* and *Marek-Sadowska*, addresses an algorithm constructing a minimal area power distribution net topology, while satisfying voltage drop and electromigration constraints. The area required by their methods on typical instances is significantly smaller than those obtained using previous methods.

As the speed increases, parasitics induced by wires degrade the high-speed performance. The effect of increased parasitic couplings not only increases signal delays, but also decreases signal

integrity due to transmission line behaviour. The fifth paper by *Tharkur* and *Wong* presents an approach for vertical crosstalk minimization problem. The vertical crosstalk problem is to minimize the crosstalk between vertical wires by finding an optimal vertical layer assignment for them. The problem is transformed it into an optimal shortest path problem.

The sixth paper by *Jhang*, *Ha*, and *Jhon* also addresses the minimization of coupling effects. A simulated annealing approach to crosstalk minimization in gridded channel routing is presented. The idea is based on the net wire rearrangement to crosstalk minimization. An experiment shows that the net-based permutation approach performs better than the previous track-oriented permutation approaches.

Field-programmable gate arrays (FPGAs) are flexible and reusable high-density chips that can be easily reconfigured. The seventh paper by *Alexander*, *Cohoon*, *Ganley* and *Robins* addresses a placement and routing for performance-driven FPGA layout. The algorithm is based on a recursive geometric strategy for simultaneous placement and global routing, with a graph-based strategy for detailed routing. The algorithm minimizes total wirelength, maximum channel width, and source-sink pathlengths, simultaneously.

The final paper by *Dehon* and *Knight, Jr.* addresses the issue of high-performance, point-to-point transmission-line signaling. The objective is to achieve low transmission latency and high signaling bandwidth.

In conclusion, the above commissioned papers in this special issue are intended of current issues and future applications of VLSI interconnections. The trend helps to further improve the high speed systems, but much work may remain to be done to improve such techniques to be more practical.

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Guest Editor's Biography

Jun-Dong Cho was born in Seoul, Korea. He received the B.S. degree in electronics from Sung Kyun Kwan University, Seoul, Korea, in 1980, the M.S. degree from Polytechnic University, Brooklyn, NY, in 1989, and the Ph.D.

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