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Modeling of Thermal Effects in Semiconductor Structures*

CHRISTOPHER M. SNOWDEN

Institute of Microwaves and Photonics, School of Electronic and Electrical Engineering, University of Leeds, Leeds, LS2 9JT, UK

A fully coupled electro-thermal hydrodynamic model is described which is suitable for modelling active devices. The model is applied to the non-isothermal simulation of pseudomorphic high electron mobility transistors (pHEMTs). A large-scale surface temperature model is described which allows thermal modelling of semiconductor devices and monolithic circuits. An example of the application of thermal modelling to monolithic circuit characterization is given.

Keywords: Thermal, modeling, semiconductor, electro-thermal, pseudomorphic, HEMT, transistors

INTRODUCTION

Until relatively recently very little effort has been devoted to thermal considerations associated with most semiconductor devices, yet in many cases the temperature of the device and self-heating have a very strong impact on their performance. The high power densities associated with modern microwave transistors makes this class of active device particularly sensitive to temperature effects and dependent on good thermal management. Compound semiconductors such as GaAs generally have a far lower thermal conductivity than Si, which can in turn lead to high operating temperatures and poor thermal stability.

Thermal analysis of semiconductor devices can be considered in two broad categories-solutions in the proximity of the active device (usually restricted purely to a local hydrodynamic treatment for a cross-section of a few square microns) [1, 2], and solutions which encompass the whole die, which may have many active devices or elements that are interacting thermally [3, 4, 5]. Most simulations that follow the latter large-scale thermodynamic approach deal with steady-state heat sources and do not encompass the active device aspects. In practice, it is desirable to link the behaviour on the microscopic device level to the macroscopic scale, since this would allow a self-consistent thermal solution to be obtained.

* Invited paper.

Contemporary semiconductor devices often have complex geometries, incorporating air bridges and heat shunts in a highly three-dimensional structure. There is generally very limited control over the local device temperature and it is often very difficult to measure. Experimental characterization usually draws on temperature-sensitive liquid crystal paints for large-scale devices and infra-red scanning for more accurate results. The thermal time constants associated with most practical semiconductor devices lie in the range 10 μs to 10 ms. These relatively long time-constants are in contrast to the time-scales over which most carrier dynamics occur (typically in the range 0.1ps to 1 ns). A consequence of the large difference in time constants is that it is not usually practicable to follow to the steady-state the evolution of full time domain electro-thermal simulations of semiconductor devices, where the time-dependent heat flow equation is solved self-consistently with the carrier transport equations.

THERMAL AND ELECTRO-THERMAL MODELING

This paper addresses the modeling of thermal effects in semiconductor structures, examining the basis electro-thermal simulation and then considers the impact on transport modelling and finally large-scale thermal modelling of complete structures (e.g. a full die). Self-heating has a significant impact on parameters such as mobility, gneration-recombination and trap occupancy. A rigorous electro-thermal solution is described here with a multi-cell coupled thermal and transport model. This is achieved by solving a set of hydrodynamic equations derived from the Boltzmann transport approximation (utilizing four moments), coupled to an accurate solution of the heat flow equation.

$$\frac{\partial n}{\partial t} + \nabla \cdot (n\mathbf{v}) = 0 \tag{1}$$

$$\frac{\partial \mathbf{v}}{\partial t} + \mathbf{v} \cdot \nabla \mathbf{v} = \frac{q}{m^*}\mathbf{E} - \frac{2}{3m^* n}\nabla(nw) + \frac{1}{3n}\nabla(nv^2) - \frac{\mathbf{v}}{\tau_p} \tag{2}$$

$$\frac{\partial w}{\partial t} + \mathbf{v} \cdot \nabla w = q\,\mathbf{v} \cdot \mathbf{E} - \frac{2}{3n}\nabla \cdot \left[n\mathbf{v}\left(w - \frac{m^*}{2}v^2\right)\right] - \frac{1}{n}\nabla \cdot \mathbf{Q} - \frac{w - w_0}{\tau_w} \tag{3}$$

$$c_L \rho_L \frac{\partial T}{\partial t} = \nabla \cdot (\kappa_L \nabla T) + H_S \tag{4}$$

$$H_S = \mathbf{J} \cdot \mathbf{E} + qE_g G \tag{5}$$

Here q represents the charge on an electron and $\nabla \cdot \mathbf{Q}$ represents the energy flow, n is the electron density, $\mathbf{v}$ the electron velocity, E electric field, m^* effective mass, τ_p and τ_w momentum and energy relaxation times respectively, and w average electron energy, c_L specific heat, ρ_L density, κ_L lattice thermal conductivity, T lattice temperature, and G generation-recombination rate. The transport parameters are assumed to be temperature-dependent and are obtained from bulk Monte Carlo simulations. The average electron energy is expressed in terms of kinetic energy and electron temperature T_e, as,

$$w = \frac{1}{2}m^* v^2 + \frac{3}{2}k\,T_e \tag{6}$$

where T_e is the average electron temperature and k is Boltzmann's constant. The energy assumptions behind this model are discussed in [6].

The numerical solution of the heat flow equation (equation 4) requires careful consideration to obtain an accurate solution, with a third-order boundary condition. Ghione *et al.*, have suggested that to obtain accurate results for MESFETs, the simulation domain for analysis should be extended horizontally for up to three times the source-drain contact spacing and to a depth of up to ten times the active layer thickness of the device [2].

Thermal modelling of semiconductor devices requires that the transport and material parameters are well characterized as a function of temperature. In the case of GaAs the following set of temperature-dependent material parameters are required:

$$\text{Low field mobility} \quad \mu_0(T) = \mu_0(300)\left(\frac{300}{T}\right)^{2.3} \tag{7}$$

$$\text{Permittivity} \quad \varepsilon_r(T) = \varepsilon_r(300)[1 + B_\varepsilon(T - 300)] \tag{8}$$

$$\text{Schottky barrier height} \quad V_{Bi}(T) = V_{Bi}(T_0) - k_T(T - T_0) \tag{9}$$

$$\text{Thermal conductivity} \quad \kappa_L = 108.0(T - 273.15)^{-0.26} \tag{10}$$

where $\mu_0(300)$ is the low field mobility at 300 K, $\varepsilon_r(300)$ is the permittivity at 300 K, k_T is the temperature coefficient of the barrier height (in the range -0.26 to -1.6×10^{-3} VK^{-1} depending on temperature), T_0 is the reference temperature, B_ε is the permittivity temperature coefficient (in the range 0.9 to 1.2 $\times$ 10^{-4} K^{-1}).

Local iso-thermal and non-isothermal models have been developed for a wide variety of semiconductor devices including BJTs, HBTs, MESFETs and HEMTs (for example [7, 8, 9]). The quasi-two-dimensional pHEMT model described in [8, 9] and illustrated in Figure 1 is well suited to electro-thermal modelling because of its very high speed of solution. Examples of isothermal and non-isothermal DC characteristics obtained using this approach are shown in Figure 2 for a 0.2 micron gate length pHEMT. It should be noted that this pHEMT model also includes a self-consistent solution of the Schrödinger equation with the Poisson and transport equations. A comparison of measured and simulated non-isothermal DC characteristics for a similar pHEMT

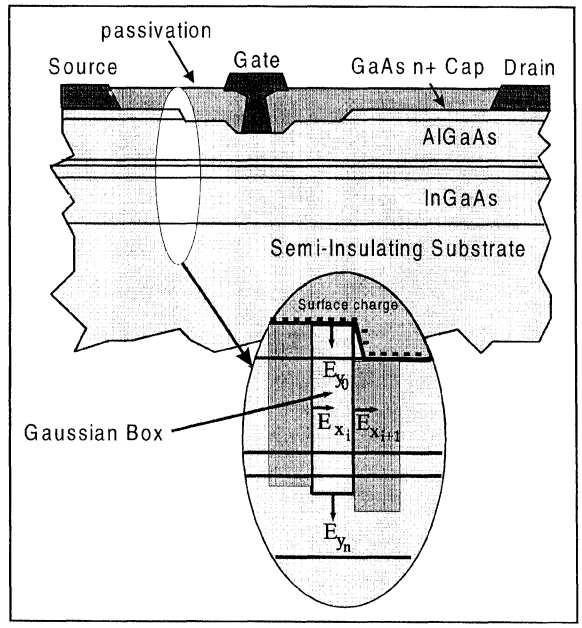
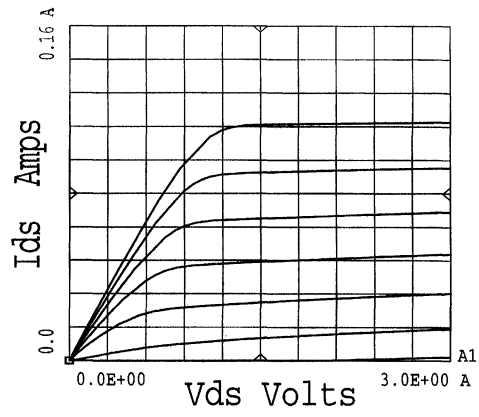


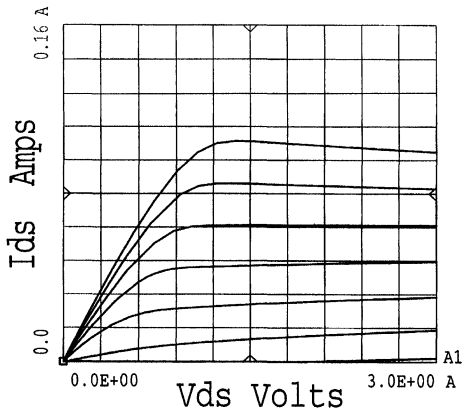
FIGURE 1 Quasi-two-dimensional model for a pseudomorphic high electron mobility transistor, illustrating the Gaussian box technique as described in [8] and [9].

are shown in Figure 3. Differences between the two DC characteristics are largely attributable to uncertainties in the exact density of the pulse-doped layer in the device (there is no fitting of the data between measured and simulated results).

A three-dimensional thermal analysis technique has been developed which allows full-scale analysis of large device and die structures, Figure 4. The steady-state heat flow equation $\nabla \cdot \kappa(T)\nabla T = 0$ is solved for a three-dimensional temperature distribution $T(x, y, z)$ using the method of Liou [4] and Gao *et al.* [5]. Since in practice most semiconductor devices are located very close to the surface of most die, it is generally only required to obtain the temperature at or close to the surface. In these circumstances it is sufficient to calculate only the surface temperature $T(x, y, 0)$. Liou and Gao's method uses a double Fourier expansion method to speed up the solution. An initial estimate of the temperature T', is first obtained by assuming that the temperature-dependent



(a)



(b)

V_{GS}: 0.5 to -2.5 V steps of -0.5 V

FIGURE 2 Simulated DC characteristics for (a) isothermal and (b) non-isothermal pHEMT models, implemented using the quasi-two-dimensional model.

thermal conductivity $\kappa(T)$ is equal to the thermal conductivity κ_0 at the mounting (heat sink) temperature T_0,

$$T'(x,y,0) = \sum_{i=1}^{N} \left\{ \frac{Q_i t \Delta x \Delta y}{\kappa_0 L_x L_y} + \sum_{m,n=0}^{\infty} \left[C_{m,n} Q_i \frac{\tanh(\gamma_{m,n} t)}{\kappa_0 \gamma_{m,n}} \cos\frac{m\pi x_i}{L_x} \cos\frac{n\pi y_i}{L_y} \right] \cos\frac{m\pi x}{L_x} \cos\frac{n\pi y}{L_y} \right\} + T_0. \tag{7}$$

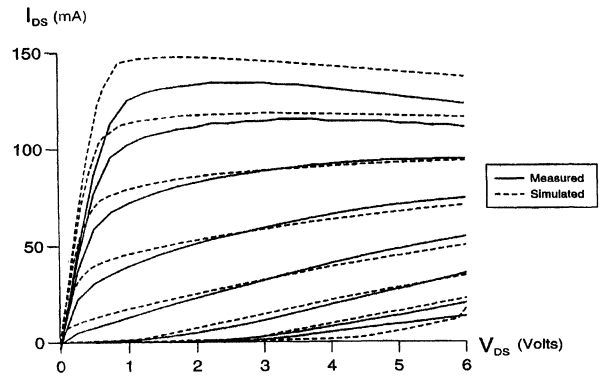


FIGURE 3 Measured and simulated DC non-isothermal characteristics for a 0.2 micron gate length pHEMT.

where,

$$\gamma_{m,n} = \pi \left[\left(\frac{m}{L_x}\right)^2 + \left(\frac{n}{L_y}\right)^2 \right]^{0.5} \tag{8}$$

$$C_{m,n} = \frac{16}{mn\pi^2} \sin\frac{m\pi\Delta x}{2L_x} \sin\frac{m\pi\Delta y}{2L_y}, \quad m \neq 0, n \neq 0 \tag{9}$$

$$C_{m,n} = \frac{4\Delta y}{m\pi L_y} \sin\frac{m\pi\Delta x}{2L_x}, \quad m = 0, n = 0 \tag{10}$$

$$C_{m,n} = \frac{4\Delta x}{n\pi L_x} \sin\frac{n\pi\Delta y}{2L_y}, \quad m = 0, n \neq 0 \tag{11}$$

where t is the thickness of the substrate, m and n the Fourier coefficients. The active region of the die where the devices are located is subdivided into regions of area $\Delta x \Delta y$ and are treated at heat sources where $Q_i \Delta x \Delta y$ is the heat generated at the i^{th} unit area located at (x_i, y_i). N is the number of unit areas on the surface. The upper limit of the coefficients m and n must be as large as possible and in practice values in excess of 70 ensure a local accuracy of better than 1 K. The heatsink is assumed to be attached to the bottom of the substrate (at $T = T_{\text{mount}}$), whilst all other surfaces except the heat sources (the active region of the semiconductor devices) are assumed to be adiabatic. The temperature T' is corrected for the temperature-dependent thermal conductivity using Kirchhoff's transform, yielding,

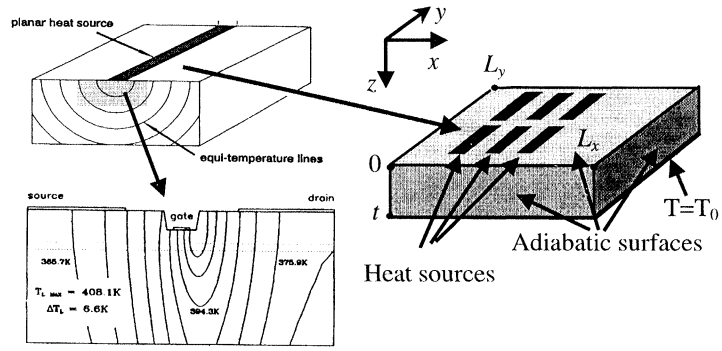


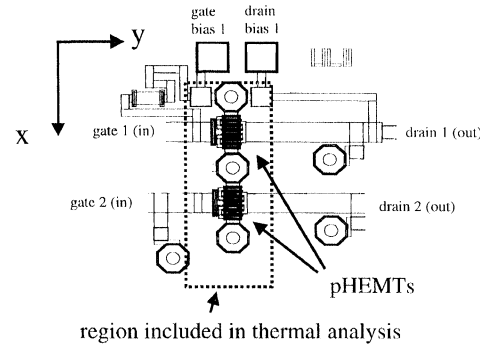
FIGURE 4 Three-dimensional temperature distribution and model based on 'line' heat sources associated with the local heat generation within the active channel of the device.

$$T(x,y,0)=\left[\frac{1}{T_0^{b-1}}-\frac{(b-1)(T'-T_0)}{T_0^{b}}\right]^{-(1/b-1)} \tag{12}$$

which assumes that the thermal conductivity is proportional to $(T/T_0)^{-b}$. In the case of GaAs $b=1.22$.

The heat sources may be treated locally using the coupled electro-thermal model, and the solution is iterated between the local transport model and the full die model. The temperature obtained from the 3D die model may be used as an initial estimate in the local transport model. The power density obtained from the solution of the transport model can in turn then be used to set Q_I in the 3D die model. It should be noted that it is necessary to minimise the number of cells since a separate transport model must be solved for each cell. This does not present a significant computational burden since the quasi-two-dimensional models can be solved in less than 0.01 cpu seconds on a typical workstation and in practice the surface temperature calculation time is the dominant factor.

An example of the application of thermal modelling is shown in Figure 5, where the surface temperature distribution is calculated for a pHEMTs 38 GHz monolithic power amplifier design. A partial view of the monolithic die layout in the vicinity of the pHEMTs is shown in Figure 5(a) and the region chosen for thermal analysis is outlined (an area of 800 × 400 microns). The die is



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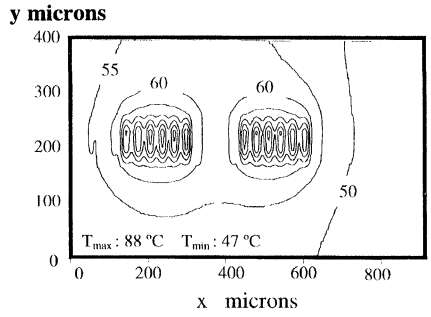

(b)

FIGURE 5 Application of thermal modelling to monolithic pHEMT amplifier design. (a) partial view of layout of a balanced 38 GHz monolithic pHEMT power amplifier (b) surface temperature distribution for the area defined by the dashed line.

400 microns thick and the mounting temperature at the back of the GaAs substrate is 40 °C. The results of the thermal simulation are shown in

Figure 5(b), where the higher temperatures surrounding the pHEMT finger regions are evident. The 3D thermal simulator utilized over 20,000 unit cells in the x, y plane to obtain the surface temperature distribution. This technique has also been applied to the coupled electro-thermal modelling of heterojunction bipolar transistors [10]. These results have been compared with infra-red measurements and were found to show good agreement (better than 6% over the whole die).

CONCLUSIONS

An electro-thermal model has been presented for semiconductor devices capable of describing the interaction between the lattice temperature, carrier transport and the observed electrical behaviour. A coupled hydrodynamic-thermal model has been used to represent the carrier transport in the vicinity of the active region of the device. Large-scale assessment of surface temperature has been achieved using a steady-state electro-thermal model. The significance of thermal effects in small-scale devices has been illustrated for the case of the short gate-length pHEMT both as a discrete device and integrated into a practical monolithic circuit.

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Authors' Biography

Christopher M. Snowden received the B.Sc, M.Sc and Ph.D. degrees from the University of Leeds. He currently holds the Chair of Microwave Engineering in the Institute of Microwaves and Photonics at the University of Leeds where he is also Head of the School of Electronic and Electrical Engineering. He was a Visiting Research Associate at the California Institute of Technology in 1987 and during the period 1990–91 he represented M/A-COM Inc. as Senior Staff Scientist. He is a Member of the MIT Electromagnetics Academy and is a Fellow of the IEEE and a Fellow of the IEE. He is a Distinguished Lecturer for the IEEE (Electron Devices Society).