Guest Editorial

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This special issue of *VLSI Design* is dedicated to Reconfigurable Computing. Reconfigurable computing technologies, such as field-programmable gate arrays (FPGAs), offer the flexibility of general-purpose processors and the high performance of application-specific integrated circuits (ASICs). FPGAs support static reconfiguration, but recently, there has been interest in exploring dynamic reconfiguration techniques. In addition to providing higher performance than general-purpose processor solutions, these emerging technologies provide new opportunities in the development of systems that can adapt to changing conditions.

The areas addressed by this special issue span architecture, software, and applications, all of which play an important role in the development of reconfigurable computing systems. New architectures are emerging that support higher gate capacities and faster speeds, allowing more complex algorithms to be implemented in “hardware” than was previously possible. In addition, to address the high reconfiguration times found in some FPGAs, architectures are being developed to support fast reconfiguration through the use of on-chip memory for storing configurations and partial reconfiguration. Software includes computer-aided design (CAD) tools to support partitioning, programming, analysis, and development of reconfigurable computing systems. It also encompasses run-time support for dynamic reconfiguration and application programming interfaces (APIs) to ease the process of implementing applications. Applications, such as those found in signal and image processing, provide a way of understanding and assessing the benefits of reconfigurable computing technology.

The first paper “An Edge-Endpoint-Based Configurable Hardware Architecture for VLSI CAD Layout Design Rule Checking” authored by Zhen Luo, Margaret Martonosi, and Pranav Ashar addresses the implementation of design rule checking (DRC) for VLSI design using configurable hardware. As integrated circuit die sizes have increased, DRC has become extremely time-consuming and compute-intensive. Although hardware accelerators for DRC have been proposed, these approaches are inflexible, requiring re-design as fabrication processes evolve over time. The authors present a DRC approach based on configurable hardware that provides a 25X or more speedup over software approaches.

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The next paper “Reconfigurable Architectures for Systems Level Applications of Adaptive Computing” authored by Brian Schott, Steve Crago, Chen Chen, Joe Czarnaski, Matt French, Ivan Hom, Tam Tho, and Terri Valenti discusses platforms being developed to support open, distributed, scalable reconfigurable computing. The authors describe the Systems Level Applications of Adaptive Computing (SLAAC) project, which is attempting to develop such an architecture. The SLAAC-1 and SLAAC-2 accelerators being developed under this effort are presented. A mapping of a Synthetic Aperture Radar/Automatic Target Recognition (SAR/ATR) application onto SLAAC-2 is discussed as well.

In the paper “Model-Integrated Tools for the Design of Dynamically Reconfigurable Systems” authored by Ted Bapty, Sandeep Neema, Jason Scott and Janos Sztipanovits, an environment for the design, analysis, and synthesis of adaptive computing applications is described. The authors discuss tools that support formal analysis for analyzing the design space, hardware/software co-simulation, and hardware/software synthesis to implement a multi-modal, dynamically adaptive application. The specific application used to illustrate the tools being developed is automatic target recognition for missiles.

The paper “Implementation of Multi-Spectral Image Classification on a Remote Adaptive Computer” authored by Marco A. Figueirido, Clay S. Gloster, Mark Stephens, Corey A. Graves and Mouna Nakkar presents an implementation for the automatic classification of space borne multi-spectral imaging. The authors demonstrate that a reconfigurable hardware approach provides better performance than a software approach implemented on a general-purpose computer. The reconfigurable computing implementation utilizes JAVA client/server programs to access the implementation from a remote site.

The last paper “Testing and Diagnosing Dynamic Reconfigurable FPGA” authored by Chi-Feng Wu and Cheng-Wen Wu discusses how the dynamic reconfiguration capability of FPGAs can be used to reduce the testing time and diagnosis of these FPGAs. The authors present a test methodology, and universal test and diagnosis approaches for dynamically reconfigurable FPGAs, which include configuring the FPGA into an easily testable array and applying test patterns. The approach is illustrated using a Xilinx XC6200 FPGA.

We hope that you enjoy this special issue. We believe that the collection of articles assembled provides insight into the potential that reconfigurable computing technology has to offer, and we hope that these articles will encourage you to further explore topics in this area. We would like to thank the numerous reviewers who provided valuable feedback and commentary on the articles. We would also like to thank Professor George Zobrist for allowing us to develop a special issue on reconfigurable computing. Finally, we would welcome any questions or comments that you may have.