

Configurable 2-D Linear Feedback Shift Registers for VLSI Built-in Self-test Designs

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Recently a multiple-sequence test generator was presented based on two-dimensional linear feedback shift registers (2-D LFSR). This generator can generate a set of pre-computed test vectors obtained by an ATPG tool for detecting random-pattern-resistant faults and particular hard-to-detect faults. In addition, it can generate better random patterns than a conventional LFSR. In this paper we describe an optimized BIST scheme which has a configurable 2-D LFSR structure. Starting from a set of stuck-at faults and a corresponding set of test vectors detecting these faults, the corresponding test pattern generator is determined automatically. A synthesis procedure of designing this test generator is presented. Experimental results show that the hardware overhead is considerably reduced compared with 2-D LFSR generators.

Keywords: Linear feedback shift registers (LFSR); built-in self-test (BIST); pseudo-random testing; deterministic testing; fault detection and fault coverage

1. INTRODUCTION

Ever-increasing VLSI circuit density has made today's chip testing more complicated and costly. Built-in self-test (BIST) has been proven to be an effective approach to achieve sufficiently high, if not complete, fault coverage without any external automatic test equipment on site. It has revolutionized the way the integrated circuit chips can be tested by (1) reducing the cost of manufacturing testing by shortening the test application time, (2) minimizing the amount of test data stored, and (3) lowering the cost of test equipment. The

implementation of BIST can result in a reduction of the product development cycle and cost, and the cost of system maintenance can be significantly reduced by testing chips, boards, and the entire system virtually using BIST.

Typical BIST architecture consists of a test pattern generator and a test response analyzer. The efficiency of BIST implementation can be characterized by test length and hardware overhead for a given fault coverage requirement which is defined as the ratio of the number of faults that can be detected to the total number of faults in the assumed fault domain. It is expected that BIST

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insertion to integrated circuit chips will result in high fault coverage, small volume of test data, at-system test speed, and compatibility with the design for testability techniques. High fault coverage can be achieved only if all faults of interest are detected and their effects are retained in the test response analyzer.

There have been various BIST techniques based on pseudo-random testing [1, 9], pseudo-exhaustive testing [2, 10, 11], weighted random testing [3, 12, 13], and reseeding of LFSR [5–7]. These approaches offer different trade-off among test data volume, test application time, hardware overhead and fault coverage. One of the most popular approaches is the pseudo-random BIST, which employs an LFSR to generate a large number of test patterns with small hardware overhead. The major limitations with this method are the long test time and low fault coverage. Several approaches have been proposed to overcome these disadvantages, most of which embed a set of pre-computed test vectors, called deterministic patterns, to reach high fault coverage within a shorter time. Such deterministic patterns can be obtained by an automatic test pattern generation (ATPG) and implemented with a ROM to store the patterns, or the traditional LFSRs with pre-designed seeds to generate the patterns.

Recently, another method was presented to realize both pseudo-random pattern generation and deterministic pattern embedding using a 2-D LFSR [8]. With the two-dimensional feedback algorithm, it can achieve higher fault coverage than the conventional LFSR due to improved randomness. However, the hardware overhead is much higher than conventional LFSR for some practical circuits. In this paper, our focus is to reduce the hardware overhead by proposing a configurable 2-D LFSR based BIST scheme.

2. 2-D LINEAR FEEDBACK SHIFTER REGISTERS

A conventional LFSR can be used to generate a large number of pseudo-random test patterns with

very small area overhead that is composed of exclusive-or gates (XORs) and flip-flops (FFs). The general structure is shown in Figure 1, which can be expressed with the polynomial in Eq. (1).

$$P(V) = 1 + C_1V + C_2V^2 + \dots + C_{M-1}V^{M-1} + V^M \quad (1)$$

The coefficients $C_i (i = 1 \sim M - 1)$ are zero or one. An LFSR goes through a cyclic sequence of states and the outputs produced are also periodic. The maximum length of this period is $2^M - 1$, where M is the number of stages. So the patterns generated by an LFSR are pseudo-random and the random properties depend on its initial state and its generating function $P(V)$. Once the generating function and the initial state are fixed, the patterns produced are also determined and in one period there is no recurrent patterns. It cannot produce a sequence of deterministic ordered patterns. The fault coverage is usually low because the random-pattern-resistant faults exist in some logic structures that can be detected only by deterministic ordered patterns. A number of the LFSR based techniques [5–7] have been developed to generate deterministic ordered test patterns to detect the random-pattern-resistant faults, but the encoding and decoding procedures and the implementation of control logic are relatively complex. A 2-D LFSR structure was presented in [8], which can first generate a deterministic sequence used to detect random-pattern-resistant faults, followed by random patterns used to detect a large percentage of easily testable faults. Figure 2 shows the general representation of a 2-D LFSR based on N primitive polynomials:

$$V_i = \sum_{j=1}^N \sum_{k=1}^M a_{ijk} V_j D^k + C_i, \quad i = 1 \sim N \quad (2)$$

This circuit consists of N shift registers, each of which has M stages. $V_i (i = 1 \sim N)$ represents an N -bit vector, and $V_i D^k (k = 1 \sim M)$ represents the k th delay of a vector V_i . V_i is generated by the feedback network given by Eq. (2). If $a_{ijk} = 1$, the


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if ( $V_i$  is not SOLVED ) {
    Build_Inverted_Equations; /* For-
    mulate Eq. (3) and set  $C_i=1$  */
    Assign a set of  $a_{ijk}$  values to Eq. (3);
    if ( $a_{ijk}$  values are valid)
        mark signal  $V_i$  SOLVED;
    else {
        use branch & bound method to
        obtain a new set of  $a_{ijk}$  values;
        if ( $a_{ijk}$  values are valid) {
            mark signal  $V_i$  SOLVED;
        }
    }
} /* next unsolved signal */
M = M + 1;
Set initial states of 2-D LFSR;
} /* next time frame */
} /* end */

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Besides embedding the deterministic sequence, the 2-D LFSR can generate better pseudo-random patterns than a conventional LFSR according to the experimental results in [8]. The longer the deterministic sequence is, the more stages of a 2-D LFSR are required, which means more hardware required. For some practical circuits, a large overhead is unacceptable. In the next section, a feasible configuration scheme based on a 2-D LFSR to reduce the overhead is proposed.

3. CONFIGURABLE 2-D LFSR BASED TEST PATTERN GENERATOR

A configurable 2-D LFSR based test pattern generator is proposed to generate an embedded deterministic sequence of test patterns followed by pseudo-random patterns. The generator mainly consists of four types of function blocks—the flip–flop array (FFA), the configuration network (CN), the multiplexers (MUXs), and the control unit (CU) as shown in Figure 3. The FFA is an $N \times M$ flip–flop array, where N is the number of inputs of a circuit under test (CUT) and M is the number of

stages of the 2-D LFSR. In order to reduce the hardware, M is usually a small number. If Eq. (3) cannot be solved with a small value of M , the embedded test sequence is then partitioned into subsequences for obtaining solutions for a configurable scheme. Each CN consists of XOR gates and an inverter if necessary. The MUX block selects one of the p configuration networks and feeds the feedback signal to the N -input FFA, where p is the number of configurations. The MUX block is controlled by $\lceil \log_2 p \rceil$ signals as shown in Figure 3. A relatively simple CU generates these signals for the MUX and a reset signal for the FFA. When resetting the generator, the initial states of FFA are set to $\langle 1010 \dots \rangle$ in each column of the FFA.

The synthesis procedure for a configurable 2-D LFSR is shown in Figure 4 with two main tasks: (1) find a set of deterministic ordered patterns and (2) embed these patterns in the configurable 2-D LFSR. The HITEC [4] is used as an ATPG tool to generate a set of test patterns for detecting random-pattern-resistant faults. For some circuits, however, it is hard to find test patterns to detect random-pattern-resistant faults only. Therefore, all faults including random-pattern-detectable and random-pattern-resistant faults are considered in ATPG. With the test patterns generated by the ATPG, the coefficients a_{ijk} 's in Eq. (3) is solved so as to generate the sequence of test patterns. The number of stages, M , in the 2-D LFSR reflects the hardware complexity. Given a small number of M , Eq. (3) is sometimes not solvable; therefore, a modified algorithm is needed. For example, partitioning the original sequence of test patterns into consecutive subsequences of test patterns and then solving Eq. (3) for each subsequence becomes a feasible solution. As the length of each subsequence decreases, Eq. (3) can be solved with an acceptable small number of stages. While the number of LFSR stages decreases by the partitioning sequence, the complexity of the configuration network increases. Hence, it is necessary to optimize the configuration network for a less cost.

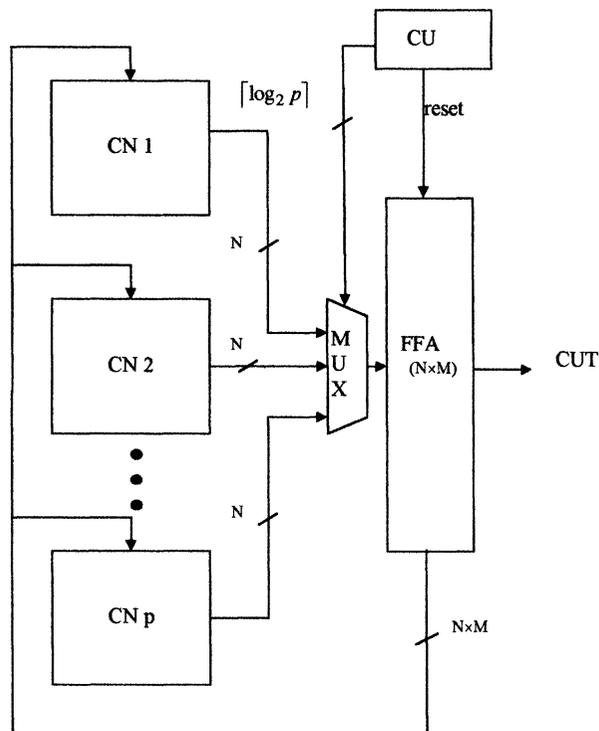


FIGURE 3 Configurable 2-D LFSR based BIST scheme.

The following is an example to show the effectiveness of the configurable 2-D LFSR based generator. Given a deterministic ordered sequence with 18 6-bit patterns with the initial seed $\langle 101010 \rangle$,

number will be 5 without the configuration structure as shown in Figure 6. The initial patterns of both generators are shown in Figures 5 and 6. The first test pattern $\langle 101001 \rangle$ in this example is generated with the initial pattern $\langle 101010 \rangle$ feeding

	\xrightarrow{t}																	
	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}	t_{16}	t_{17}	t_{18}
1:	1	0	1	0	0	0	0	1	1	1	0	0	1	0	1	1	1	0
2:	0	1	1	0	1	0	1	1	1	0	0	0	1	0	0	0	0	1
3:	1	1	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0
4:	0	1	1	1	1	0	0	0	1	0	0	1	1	0	0	0	1	0
5:	0	0	1	1	1	0	1	1	0	1	0	1	1	1	0	0	1	0
6:	1	0	1	1	1	1	0	0	0	1	1	1	1	1	0	1	0	1

both a configurable generator and a non-configurable generator are designed. Figure 5 shows the schematics of the generator with 1-stage registers and two configuration networks, whereas the stage

through the configuration network CN1, and then is shifted into the 2-D LFSR. Other patterns are generated in sequence by following the same procedures until the ninth pattern $\langle 110100 \rangle$ is

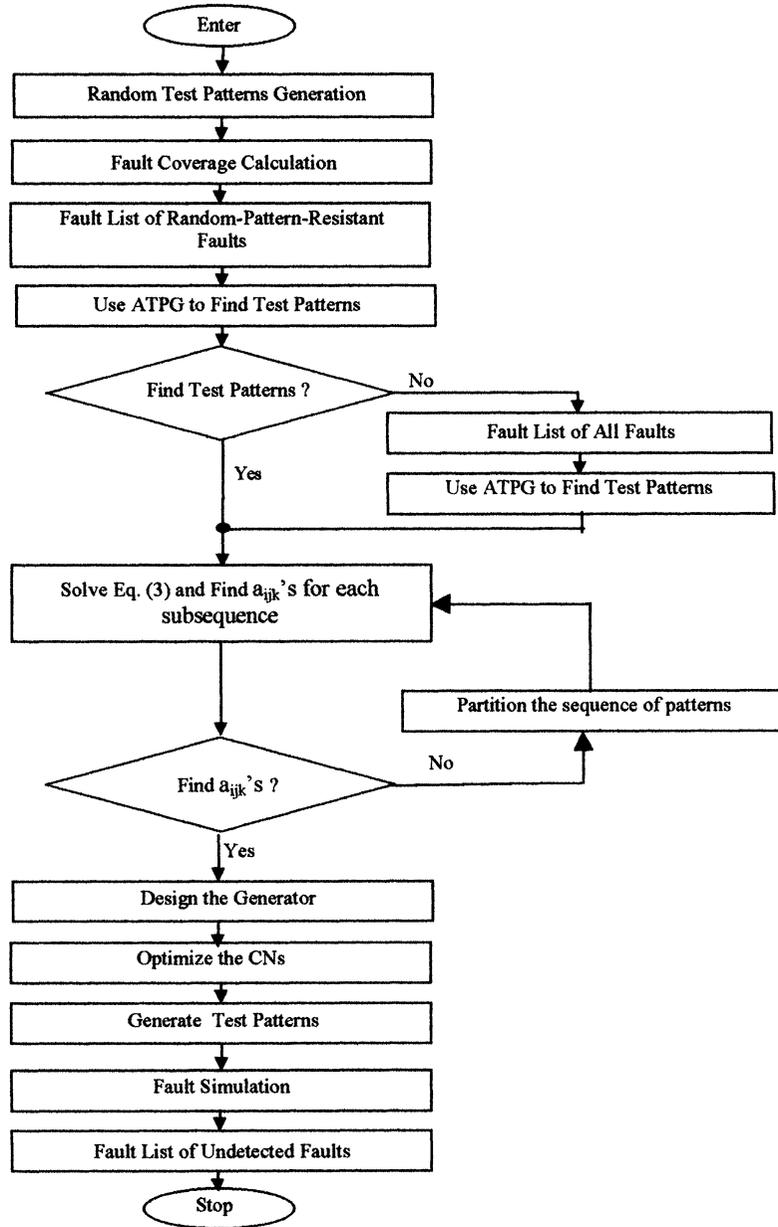


FIGURE 4 Synthesis procedure of a configurable 2-D LFSR.

generated. In this configurable generator, the CN1 generates the first 9 patterns, $\langle 101001 \rangle$, $\langle 011100 \rangle$, $\langle 111111 \rangle$, $\langle 001111 \rangle$, $\langle 010111 \rangle$, $\langle 000001 \rangle$, $\langle 010010 \rangle$, $\langle 111010 \rangle$ and $\langle 110100 \rangle$. The CN2 generates the other 9 patterns, $\langle 100011 \rangle$, $\langle 001001 \rangle$, $\langle 001111 \rangle$, $\langle 110111 \rangle$, $\langle 000011 \rangle$, $\langle 100000 \rangle$, $\langle 101001 \rangle$, $\langle 100110 \rangle$

and $\langle 010001 \rangle$. The tenth pattern is generated with the ninth pattern $\langle 110100 \rangle$ feeding through the CN2. The CU with a modulo-9 counter controls this switch. With the optimization on the feedback network of Figure 5, an optimized configurable 2-D LFSR is shown in Figure 7.

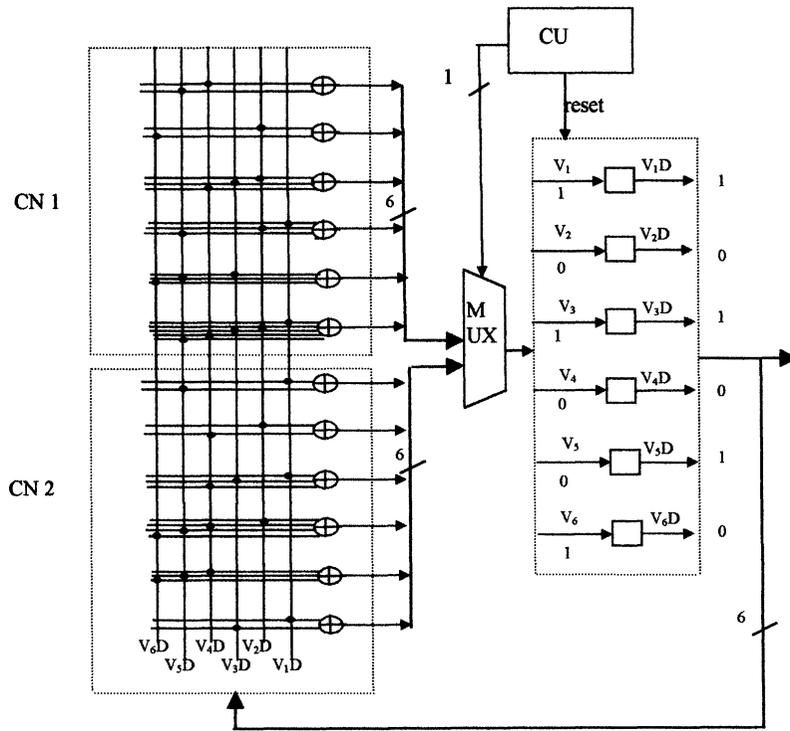


FIGURE 5 A configurable 2-D LFSR based test pattern generator.

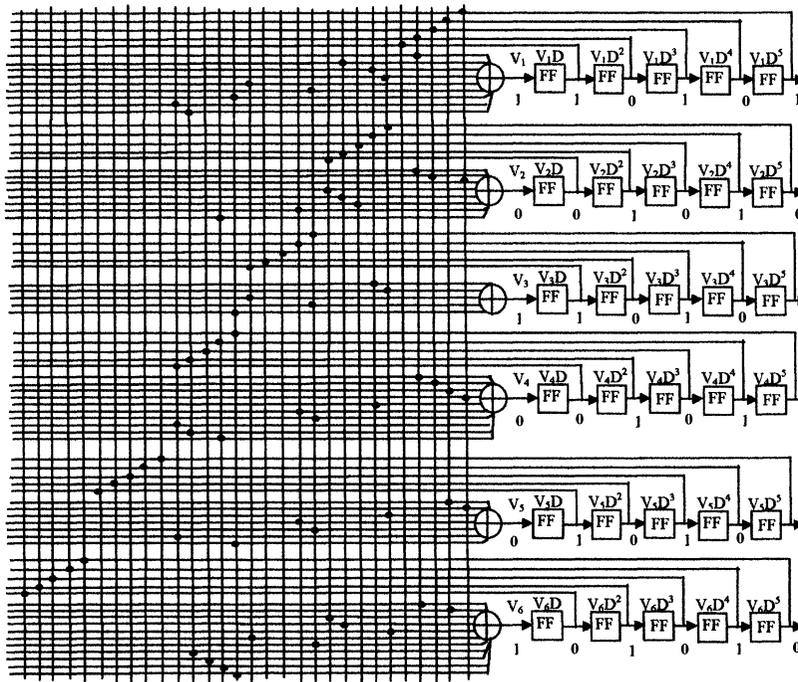


FIGURE 6 A 2-D LFSR test pattern generator.

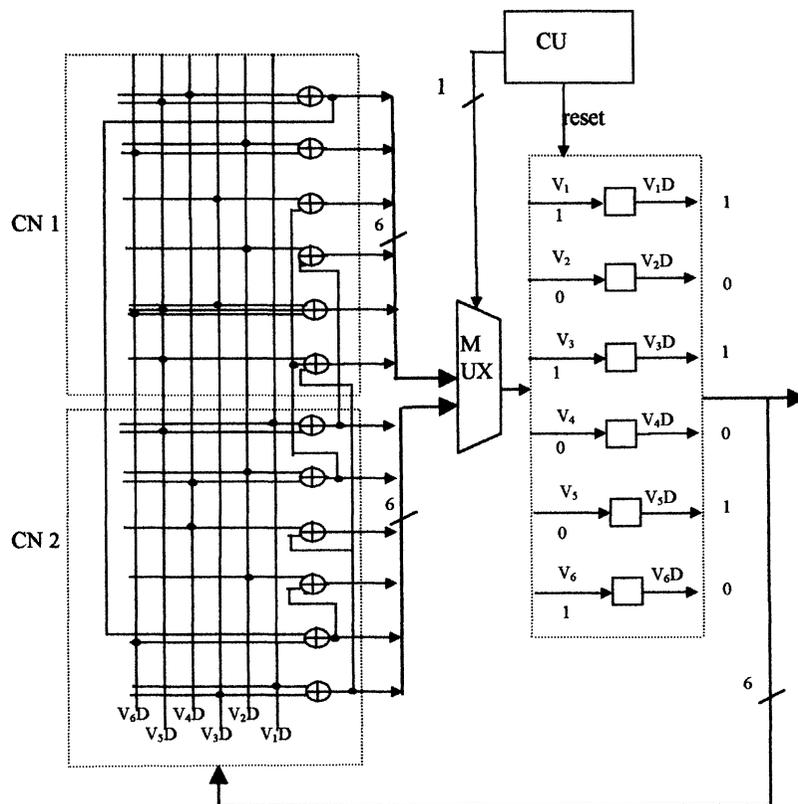


FIGURE 7 An optimized configurable 2-D LFSR based test pattern generator.

4. EXPERIMENTAL RESULTS

Five synthesized circuits are used as benchmark circuits to evaluate the configuration structure in the 2-D LFSR scheme. The characteristics of the five circuits are summarized in Table I. *Am2910* is a 12-bit microprogram sequencer, which has a stack of depth 5, a stack pointer, a microprogram counter, and a register counter (down counter). A 4-to-1 multiplexer selects the next microprogram

TABLE I Characteristics of five synthesized circuits

Circuits	Seq. depth	FFs	PIs	POs
<i>am2910</i>	4	87	20	16
<i>mult16</i>	9	55	18	33
<i>div16</i>	19	50	33	34
<i>pcont2</i>	3	24	9	8
<i>piir8</i>	5	56	9	8

address from either the input data bus, the stack, the register counter, or the microprogram counter. *Mult16* is a 16-bit 2's complement multiplier, which uses a shift-and-add algorithm. The control unit has been implemented using 3-bit and 4-bit counters. There is one start instruction. *Div16* is a 16-bit divider that uses repeated subtraction to perform division. A zero-detect unit checks for the divide-overflow condition and flags the termination of the repeated subtraction loop. There is one control instruction: Start. *Pcont2* is an 8-bit parallel controller used in DSP applications. This circuit is composed of 8 adders, 2 fixed-point multipliers, and 3 MUXs – all combinational logic. Three registers serve as delay elements. A global reset line resets all the registers, and new data is input at every clock cycle. There is no control unit. *Piir8* is an 8-point infinite impulse

response filter for DSP applications. It has a very regular structure with 7 adders, 8 fixed-point multipliers, 7 8-bit registers, and 7 2-to-1 MUXs. The data input and output buses are 8 bits wide. There is no control unit. A global reset line is the only control signal. In Table II, the configuration and the original non-configuration results of the five benchmark circuits are compared. The first column is the number of embedded deterministic patterns detecting the random-resistant faults for each circuit. The second and third columns give the stage number of shift registers and the total number of flip-flops for the non-configurable test generator. The number of configurations, the stage number of shift registers and the total number of flip-flops for the configurable 2-D LFSR based generator are given in the fourth, fifth and sixth columns. For the *am2910* and *mul16* the flip-flops are reduced significantly to 15% and 14% respectively. Because the number of embedded patterns for *div16*, *pcont2* and *piir8* is small, the synthesis procedure results in no reconfiguration. Compared with the other four circuits, *div16* has the largest FFA due to its large number of inputs. The minimum stage number of M can be obtained

by increasing the loop times in the branch and bound algorithm while solving Eq. (3) at a cost of CPU time. Table III shows the comparison of the fault. The test patterns generated by HITEC can be either stored in a ROM or scanned in. The results of the conventional LFSR generator are listed in the third column. Column four gives the results from a combination of the conventional LFSR and the additional deterministic ordered patterns. The data in the fifth and last columns are obtained by the 2-D LFSR and the configurable 2-D LFSR based generators respectively. The average number of equivalent faults of five circuits is 9,441 where 3,955 faults are detected by "HITEC" and 6,054 faults are detected by "Random Patterns". Comparing "LFSR", "LFSR+Add", and "2-D LFSR", the experimental results show that the average detected faults by "2-D LFSR" is 5.08% higher than that of "LFSR+Add" and 8.65% higher than that of "LFSR". Note that the average number of faults detected by "2-D LFSR" is 5,952, which is only 1.76% less than that of "Random Patterns". The average number of faults detected by "Configurable 2-D LFSR" is 5,986, which covers about the

TABLE II Hardware comparison of 2-D LFSR and configurable 2-D LFSR

Circuits	Patterns	2-D LFSR		Configurable 2-D LFSR		
		Stages	Flip-flops	Config.	Stages	Flip-flops
<i>am2910</i>	30	13	260	2	2	40
<i>mul16</i>	72	14	252	4	2	36
<i>div16</i>	21	10	330	1	2	66
<i>pcont2</i>	7	2	18	1	2	18
<i>piir8</i>	19	3	27	1	3	27
Total	149	—	887	—	—	187

TABLE III Test generation and fault simulation for five synthesized circuits

Circuits	Total faults	HITEC		Random patterns		LFSR		LFSR+Add		2-D LFSR		Configurable 2-D LFSR	
		Det	Vec	Det	Vec	Det	Vec	Det	Vec	Det	Vec	Det	Vec
<i>am2910</i>	2391	2142	726	2155	2^{17}	2126	2^{17}	2166	$2^{17}+30$	2188	2^{17}	2179	2^{17}
<i>mult16</i>	1708	1568	89	1475	2^{17}	665	2^{17}	1395	$2^{17}+89$	1605	2^{17}	1605	2^{17}
<i>div16</i>	2147	1676	190	1718	2^{17}	1679	2^{17}	1702	$2^{17}+21$	1705	2^{17}	1719	2^{17}
<i>pcont2</i>	11272	3147	7	6815	2^{17}	6727	2^{17}	6727	$2^{17}+7$	6336	2^{17}	6518	2^{17}
<i>piir8</i>	29689	11234	19	18106	2^{17}	16195	2^{17}	16331	$2^{17}+19$	17925	2^{17}	17913	2^{17}
Avg.	9441	3955	209	6054	2^{17}	5478	2^{17}	5664	$\sim 2^{17}$	5952	2^{17}	5986	2^{17}

same number of detected faults as the 2-D LFSR generator, but the overall overhead of the FFA has been reduced by 79%.

5. CONCLUSION

A BIST scheme based on a configurable 2-D LFSR and a procedure to design a test pattern generator have been presented. Without storage of test patterns and seeds, the 2-D LFSR test pattern generator can generate a sequence of deterministic test patterns as well as pseudo-random patterns. The hardware overhead of this BIST scheme decreased considerably through configuration. The experiment result shows that compared with the non-configurable 2-D LFSR, the number of flip-flops is reduced by 79% for five synthesized circuits. The average number of faults detected by the configurable 2-D LFSR is 9.27% higher than that of the conventional LFSR and 0.57% higher than that of the non-configurable 2-D LFSR.

In order to improve the fault coverage of the configurable 2-D test pattern generator, a set of embedded deterministic patterns with high fault coverage is needed. Logic optimization tools are also necessary to further reduce the hardware overhead of the feedback networks.

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