A Probabilistic Power Estimation Method for Combinational Circuits Under Real Gate Delay Model*

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Our aim is the development of a novel probabilistic method to estimate the power consumption of a combinational circuit under real gate delay model handling temporal, structural and input pattern dependencies. The chosen gate delay model allows handling both the functional and spurious transitions. It is proved that the switching activity evaluation problem assuming real gate delay model is reduced to the zero delay switching activity evaluation problem at specific time instances. A modified Boolean function, which describes the logic behavior of a signal at any time instance, including time parameter is introduced. Moreover, a mathematical model based on Markov stochastic processes, which describes the temporal and spatial correlation in terms of the associated zero delay based parameters is presented. Based on the mathematical model and considering the modified Boolean function, a new algorithm to evaluate the switching activity at specific time instances using Ordering Binary Decision Diagrams (OBDDs) is also presented. Comparative study of benchmark circuits demonstrates the accuracy and efficiency of the proposed method.

Keywords: Low power design; Switching activity estimation; Power dissipation model; Markov chains; Temporal and spatial correlation; CMOS combinational circuits

1. INTRODUCTION

Power dissipation is recognized as a critical parameter in modern VLSI design field. The

development of competitive market sectors such as wireless applications, laptops, and portable medical devices, depend on the power consumption as the most important parameter, because the

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growth rate of the battery technologies is not so promising. In addition, problems such as chip overheating, electromigration and hot electrons are strongly-dependent on power dissipation [1, 2]. For these reasons low power design techniques at all levels of the design flow ranging from the layout level up to architectural and system level have been developed [1, 2]. However, an estimation of the power consumption at any design level, is required. Thus simultaneously with low power design techniques a large number of power estimation methods have been also developed [2, 3].

The power dissipation at gate level is proportional to the switching activity of the circuit nodes, because in the current technologies the dynamic power dissipation is by far the most dominated factor comparing with the power consumption coming from the short circuit and leakage current. According to their mathematical model, the power estimation methods of the combinational circuits are categorized as probabilistic methods and statistical ones. Moreover, considering the assumed gate delay model they are also characterized as zero- and real-gate delay methods. A survey of the power estimation methods for combinational logic circuits has been reported in [2, 3].

Assuming zero-gate delay model [4, 5] and real gate delay model [6–9], a number of probabilistic power estimation methods have been presented. In particular, a method for calculating the switching activity of the circuit nodes, using Order Binary Decision Diagrams (OBDDs) was proposed [4]. Modeling the behavior of the logic signal as an one step Markovian process the first order temporal correlation was captured. Moreover, structural correlation, which is coming from the reconvergent fanout nodes, was also considered by partitioning the circuit using techniques from the chip testing field. However, the input signals were assumed to be mutually-independent, making this method inaccurate for highly correlated input streams. In [5], a probabilistic method, which captures all the types of correlations was presented. Specifically, modeling the logic signal as a Markovian process,

the temporal correlation was considered, while the input pattern dependency was also captured by the concepts of the spatiotemporal transition correlation coefficient and the signal isotropy. Using OBDDs, the structural correlation was considered by propagating the estimated switching activities and spatiotemporal coefficients through the circuit nodes. In [6], the concept of the probability waveforms to estimate the average power dissipation was presented. The probability waveforms consist of the signal probability and the signal transition probability value. Given the probability waveforms of the primary inputs, an algorithm to estimate the probability waveforms of the internal nodes of the circuit has been introduced. However, both the structural and input dependencies were not taken into consideration. An extension of the probability waveforms is the tagged probabilistic simulation approach presented in [7]. In particular, at each node the transition probability is broken in four cases: stable to 0, stable to 1, perform a low to high transition ($0 \rightarrow 1$) and a high to low ($1 \rightarrow 0$) transition. Inertial delays, hazards, temporal correlation of the primary inputs and structural correlations were considered by this method. However, the primary inputs were assumed spatially uncorellated, while simultaneous transitions were not considered. In [8], a symbolic simulation algorithm has been proposed using OBDDs. The structural and the first-order temporal correlation were handled but the input pattern dependency was not considered. A new method for calculating the transition probabilities by performing symbolic polynomial simulation was proposed in [9]. It is based on the signal probability evaluation method of [11], which has been extended to handle temporal correlation and arbitrary transport gate delay models. The method was parameterized by a single factor, which determines the circuit levels over which the structural correlation is considered. A propagation algorithm of the estimated switching activities through the circuit nodes has also been presented. However, the input signals were also considered mutually-independent making this method inaccurate.

In this paper a novel probabilistic method for accurate power estimation of a combinatorial circuit is introduced. Taking into account the temporal, structural and input pattern dependency of the circuit signals and considering simultaneous transitions, the switching activity of any logic circuit node is calculated under a real delay gate model. Since the proposed method includes all the types of data correlations, it can be considered as an extension of the approach of [5]. Although the [5] can capture all the types of correlations, is valid only for zero delay model. In contrast, the proposed method derives accurate results because it captures all the possible signal transitions, *i.e.*, the functional transition and the spurious transitions (or glitches).

It is proved that under a proper formulation, the switching activity estimation problem assuming real gate delay model can be transformed to a zero delay switching activity estimation problem at specific time instances. For this reason a new Boolean function including time parameter and a proper mathematical model are established. The concepts of transition probability and spatiotemporal correlation coefficient, which are derived from the zero delay switching activity estimation field, are extended to estimate the switching activity under real delay model. Also, it is proved that the transition probabilities and transition correlation coefficients of the primary inputs at any time interval can be evaluated by the zero delay transition probabilities and transition correlation coefficients. Moreover, a method for the switching activity evaluation of circuit nodes in different time instances using OBDDs is also introduced. Employing a set of benchmark circuits, comparisons with a switch level simulation and the method of [9] prove the efficiency of the proposed method.

The paper is organized, as follows: in Section 2 the problem formulation is presented, the mathematical model is introduced in Section 3, while the switching activity evaluation algorithm is given in Section 4. The experimental results are presented in Section 5 while the

conclusions and future work are discussed in Section 6.

2. PROBLEM FORMULATION

The power estimation problem of a combinational logic circuit, under real gate delay model can be stated as:

“Given the gate level description of a combinational circuit with N inputs and M outputs and the inertial delays of its gates, and, assuming that the period of the applied input vectors is greater or equal to the settling time of the circuit, estimate the average power consumption of the circuit for an input vector stream through the calculation of the circuit average switching activity.”

The accuracy of the switching activity evaluation is strongly depended on the data correlation of the circuit signals and the assumed gate delay model. Concerning data correlation, it includes the temporal and spatial correlation. By temporal correlation we mean the dependency of a signal on its previous values. The spatial correlation is divided to the structural correlation, which is coming from the reconvergent fanout nodes, and the input pattern dependency coming from the sequence of the applied input vectors. In zero delay model, a gate perform at most one transition in a clock cycle, which is called *functional* or *useful transition*. However, under real delay model the gate may perform additional transitions called *spurious transitions* or *glitches*. Therefore, all types of signals correlations under real delay model have to be considered to estimate the power dissipation accurately.

The output of a gate generates a glitch, if two conditions are satisfied: (i) the *necessary condition*, which requires the difference of the transition arrival times of the input signals to be equal or greater than the inertial delay of the gate and (ii) the *sufficient condition*, which requires the appropriate transitions of the input signal(s) to switch the gate output. Consequently, the time parameter plays an important role in the glitch generation. For that purpose, a modified Boolean function including time parameter, which will describe the exact

behavior of a logic signal in time domain, is needed. Manipulating this modified logic function and considering the probabilistic properties of its variables the switching activity can be calculated accurately.

Example We assume a logic circuit with gate delay equals to one delay unit, d , as it shown in Figure 1. The logic behavior of the node f can be described in time domain as follows:

$$f = F(x_1, x_2, t) = x_1(t - 2d)x_2(t - 2d)x_2(t - d) \quad (1)$$

The signal f may switch in two time instances, i.e., $t_1^f = d$ and $t_2^f = 2d$. More specifically, the transition of the signal f at $t_1^f = d$ depends on the transitions of the primary inputs x_1 and x_2 at time points $t_1^{x_1} = -d$, $t_1^{x_2} = -d$, and $t_1^{x_2} = 0$, while the transition of f at $t_2^f = 2d$ depends on the transitions of the signals x_1 and x_2 at $t_2^{x_1} = 0$, $t_2^{x_2} = 0$, and $t_2^{x_2} = d$. The corresponding logic functions of f , which are derived by (1), of time instances t_1 and t_2 are: $f_1 = F(x_1, x_2, d) = x_1(-d)x_2(-d)x_2(0)$ and $f_2 = F(x_1, x_2, 2d) = x_1(0)x_2(0)x_2(d)$, respectively.

From the above example, we infer that the time parameter plays critical role in the generation of the switching activity. Additionally, the logic behavior of signal f is described entirely by the modified logic function of Eq. (1) at any time instance. The general form of this function

is given bellow:

$$f(t, x_1, x_2, \dots, x_n) = f(\tilde{x}(t - k_1), \dots, \tilde{x}_p(t - k_p)) \quad (2)$$

with $k_i = \sum_j d_j$

where, k_i is the delay of the path π_i and d_j is the delay of the j th gate, p is the number of paths, $\tilde{x}_k = x_i$ if π_k starts at input x_i . This function describes the logic behavior of a signal in time domain, while in the specific time instances it is reduced to an ordinary Boolean function, where the Boolean variables are the corresponding logic values of the input signals of these time points.

Having as starting point Eq. (2), a novel mathematical model, which describes the behavior of a logic signal in terms of time should be introduced. We aim at the development of a new method, which reduces the power estimation problem considering real delay model to a zero delay problem at certain switching time points. For that purpose, we introduce new concepts and formulas, which express parameters of real delay modeled power estimation problem in terms of zero delay parameters. Specifically, we provide the suitable material for temporal correlation modelling, extending the concept of transition probability for certain time intervals. Then, it follows a set of formally-proven new formulas of the generalised transition correlation coefficients, which describe the spatiotemporal correlation among different signals.

FIGURE 1 The logic circuit with Unit Delay AND gates.

3. MATHEMATICAL MODEL

The behavior of a binary signal, x , at a time point, t , i.e., $x(t)$, is modelled as a random variable of a time homogeneous, Strict Sense Stationary, lag-one Markov stochastic process having two states, s , with $s \in S = \{0, 1\}$ [10].

The *transition probability*, $p_{kl}^x(t)$, expresses the probability of a signal x to perform a transition from the state k to the state l within two successive time points $t-1$ and t . That is:

$$p_{kl}^x(t) = p(x(t-1) = k \wedge x(t) = l) \quad \forall k, l \in S \quad (3)$$

The *switching activity*, $E(x, t)$, of a signal x at time instance t is given by:

$$E(x, t) = p_{01}^x(t) + p_{10}^x(t) \quad (4)$$

where $p_{01}^x(t)$ (or $p_{10}^x(t)$) is the transition probability of the signal x to perform the transition from state 0 to 1 (or 1 to 0).

The above stochastic process models the behavior of an input signal at times $t=0$, $t=T$, $t=2T$, etc., where the input signal performs a transition. However, as it can be seen in Eq. (1), the transition probabilities $p_{kl}^x(t)$ of an input signal x at multiple time points $t = \pm ad$ ($a=1, 2$) (i.e., $p_{kl}^{x_1}(0)$, $p_{kl}^{x_1}(-d)$ and $p_{kl}^{x_1}(d)$), are needed.

DEFINITION 1 A *Signal Transition Probability Vector*, $\mathbf{P}^x(t)$, of a signal x at a time instance t , is defined as the vector of all transition probabilities $p_{kl}^x(t)$, with $k, l \in S$:

$$\mathbf{P}^x(t) = (p_{00}^x(t), p_{01}^x(t), p_{10}^x(t), p_{11}^x(t)) \quad (5)$$

We introduce the transition probability concept of an input signal in time intervals $(-T, 0)$ and $(0, T)$ as $p_{kk}^x(0^-)$ and $p_{ll}^x(0^+)$, respectively. It should be noticed that within these time intervals the input signal does not perform transition according to the problem formulation. Their corresponding values are computed by the next lemma.

LEMMA 1 The transition probability of an input signal, x , at a time point $t \in \{0, 0^+, 0^-\}$ is expressed

in terms of the transition probability at $t=0$ as follows:

$$\mathbf{P}^x(t) = f(\mathbf{P}^x(0)) \quad (6)$$

and are computed by:

$$p_{kk}^x(0^-) = p_{kk}^x(0) + p_{k(1-k)}^x(0) \quad \forall k \in S \quad (6a)$$

$$p_{ll}^x(0^+) = p_{ll}^x(0) + p_{(1-l)l}^x(0) \quad \forall l \in S \quad (6b)$$

$$p_{kl}^x(0^-) = p_{kl}^x(0^+) = 0 \quad \forall k, l \in S \wedge k \neq l \quad (6c)$$

Proof The proof of the above lemma is given in the Appendix I.

The above lag-one stochastic process and the one step transition probabilities (Eq. (3)) ensure that the first-order temporal correlation of a signal x can be described entirely. However, the accurate the power estimation implies that the spatial correlation among the circuit signals should be considered. Since we use a real delay gate model, the concept of Transition Correlation Coefficient, TC , [5] should be generalised for capturing the spatiotemporal correlation of two signals for any two certain time instances. The TC for a zero-delay model is [5]:

$$TC_{kl,mn}^{x_1, x_2} = \frac{p(x_1(t-1) = k \wedge x_1(t) = l \wedge x_2(t-1) = m \wedge x_2(t) = n)}{p(x_1(t-1) = k \wedge x_1(t) = l)p(x_2(t-1) = m \wedge x_2(t) = n)} \quad (7)$$

The dependency among three signals x_1 , x_2 and x_3 , is expressed by the pairwise coefficients of (6) as follows:

$$TC_{klo,mp}^{x_1, x_2, x_3} = TC_{kl,mn}^{x_1, x_2} TC_{ko,mp}^{x_1, x_3} TC_{lo,np}^{x_2, x_3} \quad \text{with } k, l, m, n, o, p \in \{0, 1\} \quad (8)$$

DEFINITION 2 A *Generalised Transition Correlation Coefficient*, $TC_{kl,mn}^{x_1, x_2}(t_1, t_2)$, between the signals x_1 and x_2 , which perform transitions from the states k to l and from m to n , at times t_1 and t_2 ,

respectively, is defined as:

$$TC_{kl,mn}^{x_1,x_2}(t_1, t_2) = \frac{p(x_1(t_1 - 1) = k \wedge x_1(t_1) = l \wedge x_2(t_2 - 1) = m \wedge x_2(t_2) = n)}{p(x_1(t_1 - 1) = k \wedge x_1(t_1) = l) p(x_2(t_2 - 1) = m \wedge x_2(t_2) = n)} \quad (9)$$

where $k, l, m, n \in S$.

Since the proposed method is a “global” one, we have to introduce appropriate generalized TCs between any two input signals, taking into account their spatiotemporal dependency. For that purpose, three time points for any input signal, *i.e.*, $t = 0^+$, $t = 0$, $t = 0^-$ (where $0^+/0^-$ denotes the time intervals $(-T, 0)/(0, T)$), are needed.

DEFINITION 3 The *Transition Probability Coefficient Vector*, $\mathbf{TC}^{x_1,x_2}(t_1, t_2)$, between two signals x_1 and x_2 at time instances t_1 and t_2 is defined as:

$$\begin{aligned} \mathbf{TC}^{x_1,x_2}(t_1, t_2) = & (TC_{00,00}^{x_1,x_2}(t_1, t_2), \\ & TC_{00,01}^{x_1,x_2}(t_1, t_2), \dots, TC_{11,11}^{x_1,x_2}(t_1, t_2)) \end{aligned} \quad (10)$$

According to Eq. (9), the transition probability coefficients vector at $t_1 = 0$ and $t_2 = 0$ contains the sixteen TCs of Eq. (7). That is:

$$\mathbf{TC}^{x_1,x_2}(0, 0) = (TC_{00,00}^{x_1,x_2}, \dots, TC_{11,11}^{x_1,x_2}) \quad (11)$$

LEMMA 2 The spatiotemporal correlation coefficients of two input signals x_1 and x_2 , at time points $t_1, t_2 \in \{0, 0^+, 0^-\}$ are expressed by:

$$\mathbf{TC}^{x_1,x_2}(t_1, t_2) = f(\mathbf{TC}^{x_1,x_2}(0, 0), \mathbf{P}^{x_1}(0), \mathbf{P}^{x_2}(0)) \quad (12)$$

and can be calculated by:

$$TC_{kk,mn}^{x_1,x_2}(0^-, 0) = \frac{TC_{kk,mn}^{x_1,x_2}(0, 0)p_{kk}^{x_1}(0) + TC_{k(1-k),mn}^{x_1,x_2}(0, 0)p_{k(1-k)}^{x_1}(0)}{(p_{kk}^{x_1}(0) + p_{k(1-k)}^{x_1}(0))p_{mn}^{x_2}(0)} \quad (12a)$$

$$TC_{ll,mn}^{x_1,x_2}(0^+, 0) = \frac{TC_{ll,mn}^{x_1,x_2}(0, 0)p_{ll}^{x_1}(0) + TC_{(1-l)l,mn}^{x_1,x_2}(0, 0)p_{(1-l)l}^{x_1}(0)}{(p_{ll}^{x_1}(0) + p_{(1-l)l}^{x_1}(0))p_{mn}^{x_2}(0)} \quad (12b)$$

$$\begin{aligned} TC_{kk,mn}^{x_1,x_2}(0^-, 0^-) = & \frac{TC_{kk,mn}^{x_1,x_2}(0, 0)p_{kk}^{x_1}(0)p_{mn}^{x_2}(0) + TC_{kk,m(1-m)}^{x_1,x_2}(0, 0)p_{kk}^{x_1}(0)p_{m(1-m)}^{x_2}(0)}{p_{kk}^{x_1}(0)p_{mn}^{x_2}(0) + p_{kk}^{x_1}(0)p_{m(1-m)}^{x_2}(0) + p_{k(1-k)}^{x_1}(0)p_{mn}^{x_2}(0) + p_{k(1-k)}^{x_1}(0)p_{m(1-m)}^{x_2}(0)} + \\ & + \frac{TC_{k(1-k),mn}^{x_1,x_2}(0, 0)p_{k(1-k)}^{x_1}(0)p_{mn}^{x_2}(0) + TC_{k(1-k),m(1-m)}^{x_1,x_2}(0, 0)p_{k(1-k)}^{x_1}(0)p_{m(1-m)}^{x_2}(0)}{p_{kk}^{x_1}(0)p_{mn}^{x_2}(0) + p_{kk}^{x_1}(0)p_{m(1-m)}^{x_2}(0) + p_{k(1-k)}^{x_1}(0)p_{mn}^{x_2}(0) + p_{k(1-k)}^{x_1}(0)p_{m(1-m)}^{x_2}(0)} \end{aligned} \quad (12c)$$

$$\begin{aligned} TC_{ll,mn}^{x_1,x_2}(0^+, 0^+) = & \frac{TC_{ll,mn}^{x_1,x_2}(0, 0)p_{ll}^{x_1}(0)p_{mn}^{x_2}(0) + TC_{ll,(1-n)n}^{x_1,x_2}(0, 0)p_{ll}^{x_1}(0)p_{(1-n)n}^{x_2}(0)}{p_{ll}^{x_1}(0)p_{mn}^{x_2}(0) + p_{ll}^{x_1}(0)p_{(1-n)n}^{x_2}(0) + p_{(1-l)l}^{x_1}(0)p_{mn}^{x_2}(0) + p_{(1-l)l}^{x_1}(0)p_{(1-n)n}^{x_2}(0)} + \\ & + \frac{TC_{(1-l)l,mn}^{x_1,x_2}(0, 0)p_{(1-l)l}^{x_1}(0)p_{mn}^{x_2}(0) + TC_{(1-l)l,(1-n)n}^{x_1,x_2}(0, 0)p_{(1-l)l}^{x_1}(0)p_{(1-n)n}^{x_2}(0)}{p_{ll}^{x_1}(0)p_{mn}^{x_2}(0) + p_{ll}^{x_1}(0)p_{(1-n)n}^{x_2}(0) + p_{(1-l)l}^{x_1}(0)p_{mn}^{x_2}(0) + p_{(1-l)l}^{x_1}(0)p_{(1-n)n}^{x_2}(0)} \end{aligned} \quad (12d)$$

where $k, l, m, n \in S$.

Proof The proof of the above lemma is given in the Appendix I.

4. SWITCHING ACTIVITY EVALUATION ALGORITHM

DEFINITION 4 We define as *Valid Time Points Vector*, $\mathbf{T}^x = (t_1, \dots, t_r)$, all the possible transition time points for a signal x .

These time points are derived by performing a traversal of the circuit from the primary inputs to primary outputs considering the delay of the gates. Consequently, the switching activity estimation problem is reduced to the estimation of $\mathbf{P}^x(t) \forall t \in \mathbf{T}^x$. The calculation procedure of switching activity (*i.e.*, estimation of $p_{kl}^x(t_i)$) is similar to the zero-delay method to [5] and consists of the following steps:

- Construct the OBDD for any time point $t_i \in \mathbf{T}^x$,
- Find the sets of all paths of the OBDD that results into the leaf node k , Π_k^x ,
- Find the sets of all paths of the OBDD that results into the leaf node l , Π_l^x and
- Combine any path of Π_k^x , with any path of the set Π_l^x :

$$p_{kl}^x = \sum_{\pi \in \Pi_k^x} \sum_{\pi' \in \Pi_l^x} \prod_{i=1}^v \left(p_{k_i l_i}^{x_i} \prod_{1 \leq i < j \leq v} TC_{k_i l_i, k_j l_j}^{x_i x_j} \right) \quad (13)$$

5. EXPERIMENTAL RESULTS

The proposed power estimation method is implemented by ANSI C language, while its efficiency is proved by a number of ISCAS'85 benchmark multilevel circuits. For technology mapping, a library of primitive gates up to 5 primary inputs, is used. All power estimations are measured in μW with 20 MHz clock frequency and 5 V power supply. Also, a gate capacitance is assumed to

be $C_g = 0.05$ pF, while a node with a fan-out F has capacitance $F * C_g$. For comparison reasons, three categories of input vectors: (i) without spatial correlation (column NO), (ii) with low spatial correlation (column LOW) and (iii) with high spatial correlation (column HIGH), are chosen. For each category and circuit and for reliability reasons, 15 input vector files of 20000 vectors are generated. These input vector files are used both for estimation and simulation.

For a signal x , we define as switching activity error the quantity $Err(x) = |E_{eff}(x) - E'_{eff}(x)| / E_{eff}(x)$, where $E_{eff}(x)$ is the real switched capacitance of signal x and $E'_{eff}(x)$ is the estimated one. For a combinational circuit with L signals and a specific input vector set V_j , we define as *Total Power Consumption* the quantity $Power(V_j) = (1/2)V_{dd}^2 \cdot f \cdot \sum_{i=1}^L E_{eff}(x_i)$, as *Total Error* the quantity $Total Error = |Power(V_j) - Power(V_j)'| / Power(V_j)$, as *Mean Error* the quantity $Mean Error(V_j) = \sum_{i=1}^L Err(x_i) / N$ and finally as *Maximum Error* the quantity $Max Error(V_j) = \max \{Err(x_1), Err(x_2), \dots, Err(x_L)\}$. Choosing K input vector sets the above formulas become as shown in the following: $Power^K = \sum_{j=1}^K Power(V_j)$, $Total Error^K = \sum_{j=1}^K Power(V_j) - \sum_{j=1}^K Power(V_j)'$, $Mean Error^K = \sum_{j=1}^K Mean Error(V_j) / K$, which is denoted as $MEAN^K$, and $Max Error^K = \max \{Mean Error(V_1), \dots, Mean Error(V_K)\}$, which is denoted as MAX^K . In our experimental procedure $K = 15$.

We compare the proposed method and the method [9], which to best of our knowledge is the most accurate real delay power estimation method, with Mentor's Graphics QUICKSIM II simulator. The power consumption differences between each method and switch level simulator are depicted in Tables I and II.

Table I gives the error in power estimation (%) of the proposed method. The average $TOTAL^K$ error is about 0.02% for NO spatial input correlation, 1.4% for LOW spatial correlation, and 1.5% for HIGH spatial correlation. The corresponding average $MEAN^K$ error values are 0.6%, 3.3% and 3.6%, while the average MAX^K

TABLE I Real power estimation errors of the prop. method

Circuit	Total ^K			Mean ^K			Max ^K		
	No	Low	High	No	Low	High	No	Low	High
c17	0,051	0,263	0,630	0,238	1,040	1,580	0,519	1,704	2,729
Cm163	0,018	0,915	0,394	0,704	3,192	3,249	1,298	4,307	4,463
Cm42	0,024	0,351	0,124	0,953	2,768	1,902	1,741	4,142	3,117
Cm82	0,027	3,600	3,603	0,223	5,192	6,009	0,391	10,186	11,833
cu	0,010	0,017	0,425	0,501	1,131	1,623	0,649	1,581	2,076
decod	0,010	0,635	0,065	1,472	4,137	3,274	3,665	7,009	5,266
Majority	0,017	0,765	2,133	0,349	3,224	4,910	1,004	4,531	6,125
pml	0,002	1,128	0,866	1,191	4,193	4,336	2,182	5,983	6,913
rca4	0,023	4,871	5,274	0,283	5,368	6,072	0,705	8,893	9,901
Average	0,020	1,394	1,502	0,657	3,361	3,662	1,350	5,371	5,825

TABLE II Real power estimation errors of method [9]

Circuit	Max ^K			Mean ^K			Max ^K		
	No	Low	High	No	Low	High	No	Low	High
c17	0,082	6,202	8,324	0,794	11,145	14,965	2,682	17,375	23,364
Cm163	0,007	5,564	7,560	1,179	14,534	19,934	3,067	21,379	29,597
Cm42	0,027	1,802	2,465	1,259	15,756	21,685	2,139	21,857	30,253
Cm82	0,018	23,117	31,10	0,550	32,19	43,232	0,965	76,959	103,31
cu	0,009	2,473	3,378	0,814	6,105	8,162	1,335	7,647	10,277
decod	0,020	7,264	9,920	2,162	20,535	28,694	5,952	33,511	47,048
Majority	0,032	4,638	6,289	0,687	12,851	17,288	1,312	19,682	26,461
pml	0,009	5,321	7,446	1,465	18,893	26,889	2,650	29,298	42,269
rca4	0,014	20,666	28,296	0,735	25,114	34,465	1,492	37,947	52,379
Average	0,024	8,561	11,642	1,072	17,458	23,924	2,399	29,517	40,552

errors are 1.3%, 5.3% and 5.8%. The input stream with NO spatial is derived by a pseudo random generator, the LOW spatial is derived by an LFSR and the HIGH spatial by the output of a counter.

The increased errors for LOW and HIGH spatial correlation input streams coming from the fact that we consider only the first order transition probabilities and the transition correlation coefficient is a pairwise coefficient. However, as it is shown in Table I, the maximum error is about 5%, while only in one case it exceeds 10%. Hence, the modeling of the switching behavior of a signal by the first order transition probabilities and the modeling of the signals correlation by the first order pairwise correlation coefficients are adequate for a gate level power estimation. In similar manner, we may consider higher order dependencies but the complexity of the problem is increased.

Table II shows the power estimation errors of [9] for the same input vectors and benchmarks. It can be seen that for NO spatial correlation, the error values are small, whereas the average errors of LOW and HIGH spatial correlation are large, *i.e.*, 8.5% and 11.6% for TOTAL^K power, 17.5% and 23.8% for MEAN^K power, and up to 30% and 40.7% for MAX^K power, respectively. The increased errors coming from the fact that the input pattern dependencies are not considered, because the input signals are assumed mutually independent.

Employing the proposed method and [9], the associated total power consumption of benchmarks circuits is shown in Table III. It can be seen that the lack of spatial correlations in the primary inputs increases the power estimation error (*e.g.*, for HIGH correlation, the MAX error of circuit

TABLE III Total power dissipation in μW

Circuit	Proposed			[9]		
	No	Low	High	No	Low	High
c17	935,000	937,938	929,588	934,950	993,350	1014,425
cm163	3310,488	3341,375	3324,125	3309,425	3495,113	3558,588
cm42	3444,600	3455,863	3448,050	3444,563	3505,338	3528,025
cm82	2023,088	2096,475	2096,538	2022,600	2493,463	2650,875
cu	12427,16	12430,51	12375,65	12409,75	12713,38	12822,60
decod	3415,038	3437,063	3413,150	3416,838	3665,025	3750,688
maj.	1048,438	1040,225	1025,888	1048,400	1097,625	1114,100
pm1	4183,313	4230,450	4219,463	4185,338	4406,163	4492,813
rca4	4024,413	4221,438	4237,625	4024,425	4856,800	5167,45

CU is 103%) making the method of [9] inefficient in terms of accuracy for correlated input streams.

6. CONCLUSIONS

Assuming a real gate delay model, we have proposed a novel method for the estimation of the power dissipation of a logic circuit. The method constitutes an extension of the zero delay probabilistic method [5] and takes into account the first-order temporal and the spatial correlations. A modified Boolean function, which describes the logic behavior of a signal in time domain, and extension of the basic concepts of the zero delay power estimation models have been introduced. The accuracy of the method has been proved, while the importance of the input pattern dependencies in terms of accuracy has been shown in the analysis of the experimental results.

Since the proposed method is a global approach, our future work is to implement a method that propagates the primary input statistics and correlation coefficients through the logic network. Moreover, the proposed method could be extended to capture the pulse filtering and elimination capacitance in a chain of gates by considering a range of inertial gate delays $[d_{\min}, d_{\max}]$ and taking into account the load capacitance. In addition, the basic concepts and the proposed method could be modified to take place in the power estimation of the sequential circuits.

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APPENDIX I

Proof of Lemma 1 The stochastic process of an input signal at time point t has as one-step probability matrix the matrix $Q(t)$ where:

$$Q(t) = \begin{bmatrix} \pi_{00}^x(t) & \pi_{01}^x(t) \\ \pi_{10}^x(t) & \pi_{11}^x(t) \end{bmatrix} \quad (\text{I.1})$$

with $0 \leq \pi_{kl}^x(t) \leq 1$, $\sum_l \pi_{kl}^x(t) = 1$ and $k, l \in S$, where each entry, $\pi_{kl}^x(t)$, is the one-step conditional probability, which can be defined by:

$$\pi_{kl}^x(t) = \frac{p_{kl}^x(t)}{p_k^x(t)} \quad \forall k, l \in S \quad (\text{I.2})$$

It is assumed that the stochastic process is time homogeneous and therefore, Chapman-Kolmogorov equations are taken place [12]. Thus, we obtain that:

$$P(t) = P(t)Q(t) \quad (\text{I.3})$$

where, $P(t) = [p_0^x(t), p_1^x(t)]$ are the steady state probability vector at time t . The stochastic processes at $t=0$ and $t=0^-$ is shown in the following

Markov Chains of input signal x : (a) $t=0$, (b) $t=0^-$.

The corresponding one-step probability matrices $Q(0)$ and the $Q(0^-)$ are:

$$Q(0) = \begin{bmatrix} \pi_{00}^x(0) & \pi_{01}^x(0) \\ \pi_{10}^x(0) & \pi_{11}^x(0) \end{bmatrix} \quad (\text{I.4})$$

$$Q(0^-) = \begin{bmatrix} \pi_{00}^x(0^-) & 0 \\ 0 & \pi_{11}^x(0^-) \end{bmatrix} \quad (\text{I.5})$$

Using Eqs. (I.4) and (I.5) and solving Eq. (I.3), it is obtained that:

$$P(0) = P(0)Q(0) \quad (\text{I.6})$$

$$p_0^x(0) = p_1^x(0)\pi_{10}^x(0) + p_0^x(0)\pi_{00}^x(0) \quad (\text{I.7})$$

$$p_1^x(0) = p_1^x(0)\pi_{11}^x(0) + p_0^x(0)\pi_{01}^x(0) \quad (\text{I.8})$$

$$P(0^-) = P(0^-)Q(0^-) \quad (\text{I.9})$$

$$p_1^x(0^-) = p_1^x(0^-)\pi_{11}^x(0^-) \quad (\text{I.10})$$

$$p_0^x(0^-) = p_0^x(0^-)\pi_{00}^x(0^-) \quad (\text{I.11})$$

Additionally, the stochastic process is SSS and thus,

$$p_1^x(0^-) = p_1^x(0) = p_1^x(0^+) = p_1^x \quad (\text{I.12})$$

$$p_0^x(0^-) = p_0^x(0) = p_0^x(0^+) = p_0^x \quad (\text{I.13})$$

$$p_0^x + p_1^x = 1 \quad (\text{I.14})$$

Then, from Eqs. (I.7), (I.8) (I.10) (I.11), (I.12), (I.13) and (I.14), it is concluded that:

$$\pi_{11}^x(0^-) = \pi_{11}^x(0) + \pi_{10}^x(0) \quad (\text{I.15})$$

$$\pi_{00}^x(0^-) = \pi_{00}^x(0) + \pi_{01}^x(0) \quad (\text{I.16})$$

Eventually, multiplying the associated left-hand and right-hand side terms of Eqs. (I.15) and (I.16) with $p_k^x(0)$, it is obtained:

$$p_{kk}^x(0^-) = p_{kk}^x(0) + p_{k(1-k)}^x(0) \quad \forall k \in S \quad (\text{I.17})$$

$$p_{kl}^x(0^-) = 0 \quad \forall k, l \in S \wedge k \neq l \quad (\text{I.18})$$

Working in similar way, we can prove for $t=0^+$.

Proof of Lemma 2 We prove the formula of Eq. (11), $TC_{ll,mm}^{x_1,x_2}(0^-,0)$. The remaining formulas, *i.e.*, Eqs. (11.1), (11.2), (11.3), (11.4) and (11.5) can be proved similarly. By definition [5], the TC for the zero delay model is:

$$TC_{kl,mm}^{x_1,x_2}(0,0) = \frac{p(x_1^{kl}(0) \wedge x_2^{mn}(0))}{p(x_1^{kl}(0))p(x_2^{mn}(0))} \quad (\text{I.19})$$

where k and l are the logic values before a transition and m and n the values after a transition of

the signals x_1 and x_2 , respectively and $k, l, m, n \in S$. From Definition 2, $TC_{kk, mn}^{x_1, x_2}(0^-, 0)$ can be expressed as:

$$TC_{kk, mn}^{x_1, x_2}(0^-, 0) = \frac{p(x_1^{kk}(0^-) \wedge x_2^{mn}(0))}{p(x_1^{kk}(0^-))p(x_2^{mn}(0))} \quad (I.20)$$

Applying Lemma 1 (i.e., Eq. (4)) and substituting the event $x_1^{kk}(0^-)$ in terms of $t=0$ into (I.20), we obtain:

$$\begin{aligned} TC_{kk, mn}^{x_1, x_2}(0^-, 0) &= \frac{p((x_1^{kk}(0) \vee x_1^{k(1-k)}(0)) \wedge x_2^{mn}(0))}{(p(x_1^{k(1-k)}(0)) + p(x_1^{kk}(0)))p(x_2^{mn}(0))} \\ &\quad (I.21) \end{aligned}$$

Since the events $x_1^{kk}(0)$ and $x_1^{k(1-k)}(0)$ are mutually disjoint, it is obtained that:

$$\begin{aligned} TC_{kk, mn}^{x_1, x_2}(0^-, 0) &= \frac{p(x_1^{kk}(0) \wedge x_2^{mn}(0)) + p(x_1^{k(1-k)}(0) \wedge x_2^{mn}(0))}{(p(x_1^{k(1-k)}(0)) + p(x_1^{kk}(0)))p(x_2^{mn}(0))} \\ &\quad (I.22) \end{aligned}$$

By definition of TC [5] at $t=0$, and using Eq. (I.19) it holds:

$$\begin{aligned} p(x_1^{kl}(0) \wedge x_2^{mn}(0)) &= p(x_1^{kl}(0))p(x_2^{mn}(0))TC_{kl, mn}^{x_1, x_2}(0, 0) \quad (I.23) \end{aligned}$$

where $k, l, m, n \in S$.

Eventually, from Eqs. (I.22) and (I.23) we infer that:

$$\begin{aligned} TC_{kk, mn}^{x_1, x_2}(0^-, 0) &= \frac{TC_{kk, mn}^{x_1, x_2}(0, 0)p_{kk}^{x_1}(0) + TC_{k(1-k), mn}^{x_1, x_2}(0, 0)p_{k(1-k)}^{x_1}(0)}{p_{kk}^{x_1}(0)p_{mn}^{x_2}(0) + p_{k(1-k)}^{x_1}(0)p_{mn}^{x_2}(0)} \quad (I.24) \end{aligned}$$

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