VLSI DESIGN
2001, Vol. 13, Nos. 1–4, pp. 163–167
Reprints available directly from the publisher
Photocopying permitted by license only

Strain-Dependence of Electron Transport in Bulk Si and Deep-Submicron MOSFETs

F. M. BUFLER[a,*], P. D. YODER[b] and W. FICHTNER[a]

[a]*Institut für Integrierte Systeme, ETH Zürich, CH-8092 Zürich, Switzerland;*
[b]*Bell Laboratories, 600 Mountain Avenue, Murray Hill, NJ 07974, USA*

The strain-dependence of electron transport in bulk Si and deep-submicron MOSFETs is investigated by full-band Monte Carlo simulation. On the bulk level, the drift velocity at medium field strengths is still enhanced above Ge-contents of 20% in the substrate, where the low-field mobility is already saturated, while the saturation velocity remains unchanged under strain. In an n-MOSFET with a metallurgical channel length of 50 nm, the saturation drain current is enhanced by up to 11%, but this maximum improvement is essentially already achieved at a Ge-content of 20% emphasizing the role of the low-field mobility as a key indicator of device performance in the deep-submicron regime.

Keywords: Strained Si; Full band structure; Monte Carlo simulation; *n*-MOSFET

I. INTRODUCTION

Growing a thin Si layer on a Si_yGe_{1-y} substrate results in biaxial tensile strain in the layer due to the mismatch in lattice constants between Si and the substrate. This strain lifts four of the six conduction-band valleys upwards in energy, thereby reducing the in-plane conductivity mass as well as intervalley scattering. These properties lead to improved field-effect transistor (FET) performance, and various device structures exploiting these benefits are currently being investigated both experimentally [1] and theoretically [2]. At the same time devices are scaled into the deep submicron regime where the influence of the full-band structure is enhanced. In this regime, the question arises as to how nonlinear bulk transport properties affect the device behavior and, in the present case of strained Si, how transport characteristics on the bulk and the device level vary as a function of the applied strain. So far, Monte Carlo device simulations of strained-Si FETs mostly relied on analytical band structure descriptions [2–4] or referred only to a fixed strain level neglecting in addition impurity scattering [5]. It is therefore the aim of this paper

*Corresponding author. Tel.: +41 1 632 5401, Fax: +41 1 632 1194, e-mail: bufler@iis.ee.ethz.ch

to address the strain-dependence of the FET performance in the nonlinear operation regime by full-band Monte Carlo (FBMC) simulation and to investigate how this behavior is related to the corresponding transport properties in strained bulk Si.

II. MONTE CARLO SIMULATION

The full band structure of (001)-strained Si is obtained by nonlocal empirical pseudopotential calculations [6] including in addition the spin-orbit interaction. The phonon scattering model comprises f-type and g-type intervalley processes and intravalley acoustic phonons in the elastic equipartition approximation [7]. The results of this model are consistent with the main experimental findings for strained Si, *i.e.*, the saturation velocity being reached at very low electric fields [8] and an electron Hall mobility of $2830\,cm^2/(Vs)$ for a Ge-content of $y = 0.3$ [9] (our drift mobility is $2230\,cm^2/(Vs)$ and the Hall factor 1.30 [10]). The other scattering mechanisms are impurity scattering and surface roughness scattering. More details of the device simulation algorithm, which is based on the frozen field obtained from the drift-diffusion (DD) simulation, are published elsewhere [11]. The ratio of diffusive to specular scattering was adjusted to reproduce at a drain voltage of 0.1 V in the unstrained-Si MOSFET the DD drain current, which relies on the surface mobility model of Ref. [12]. This resulted in a value of 50% as was also used in Ref. [13].

When comparing device simulations of FETs consisting of different materials, one has to take into account that the different band edges, band gaps and effective densities of states lead to different electron affinities, work function differences to the gate material and especially to different threshold voltages. We have calculated the changes of the valence band edge in strained Si with respect to unstrained Si by invoking the model solid theory of Van de Walle [14]. Note that these changes are not the valence-band offsets with respect to the relaxed SiGe buffer. Here, we are only interested in comparing the device performance of Si-MOSFETs under different strain. The SiGe buffer is not explicitly considered in the simulation, but the corresponding Ge-content only serves to define the strain present in the Si material. Taking the experimental gap in unstrained Si of 1.12 eV, the changes in the band gaps under strain were extracted from Ref. [6] which subsequently lead to the changes in the conduction band edges, all of which are displayed in Figure 1. As a result, the threshold voltage in the strained material is lowered, in particular due to the smaller band gap. In the strained case, the threshold voltage was determined so that the electron density profile along the channel (integrated over the direction perpendicular to the Si/SiO_2 interface) was the same as in the unstrained case for a drain voltage of 0.05 V. This definition yields somewhat larger threshold voltages than when extracted from the slope of the transfer characteristics.

In addition, the strain-induced changes in the conductivity mass, in the maximum and minimum low-field mobility and in the velocity-field characteristics shown in Figure 2 were incorporated in

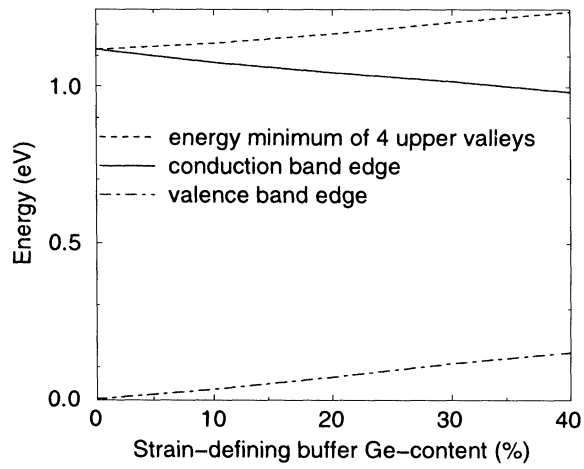

FIGURE 1 Valley splitting as well as conduction- and valence-band edges in strained Si. The strain is defined via a relaxed $Si_{1-y}Ge_y$ buffer layer.

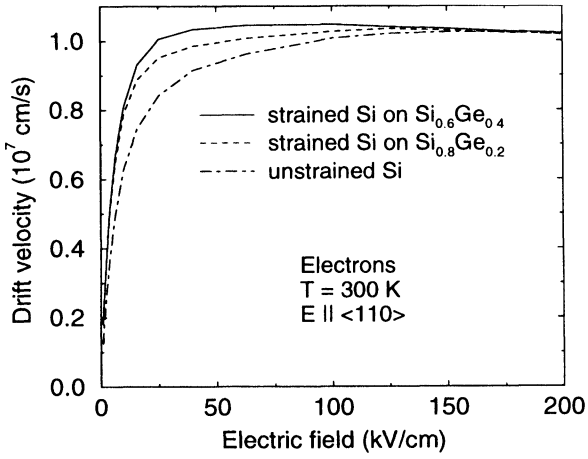

FIGURE 2 In-plane velocity-field characteristics with the field parallel to the ⟨110⟩ direction of electrons at 300 K in unstrained Si and in strained Si grown on a $Si_{0.8}Ge_{0.2}$ and a $Si_{0.6}Ge_{0.4}$ substrate, respectively.

the mobility parameterization of the DD model. (The different conductivity mass changes the surface acoustic phonon scattering [15].) Under strain, the diffusive scattering had to be enhanced by 10% so that the Monte Carlo results still agree in the linear regime with the DD drain current (in the nonlinear regime DD underestimates the saturation current).

On the other hand, it must be emphasized that the value of the surface mobility reduction in strained Si still involves large uncertainties. Due to quantization in the inversion layer, the population of the two valleys with a small in-plane mass is already enhanced in unstrained Si and the question arises to what extent the mobility enhancement can be further improved under strain. Theoretical [16] and experimental [17, 18] investigations of this problem are affected by uncertainties regarding the strength of intervalley phonon scattering and technological dependencies, respectively. However, the enhancement of the drain current in the linear regime by 44% at a gate voltage of 1 V above the threshold voltage in the present DD model seems reasonable in view of measured strain-induced improvements of the effective mobility between 17.5% [17] and 60% [18].

III. RESULTS

The velocity-field characteristics in Figure 2 exhibit the same saturation velocity in all three materials, while the strain-enhanced low-field mobility is also the same for the two different strain levels which differ only at medium field strengths. Another important strain-induced feature is that the saturation velocity is attained at much smaller field strengths than in unstrained Si in agreement with the measurement results of Sadek and Ismail [8].

The corresponding FBMC simulations of the MOSFET in Figure 3 yield the DC output characteristics of Figure 4. At the highest Ge-content of 40% in the substrate, the drain current is improved by 44% in the linear and by 11% in the saturation regime. A certain improvement of the drain current is also present for Ge-contents above 20%, where the low-field mobility is saturated, but this enhancement is rather small. Note also that the saturation of the drain current

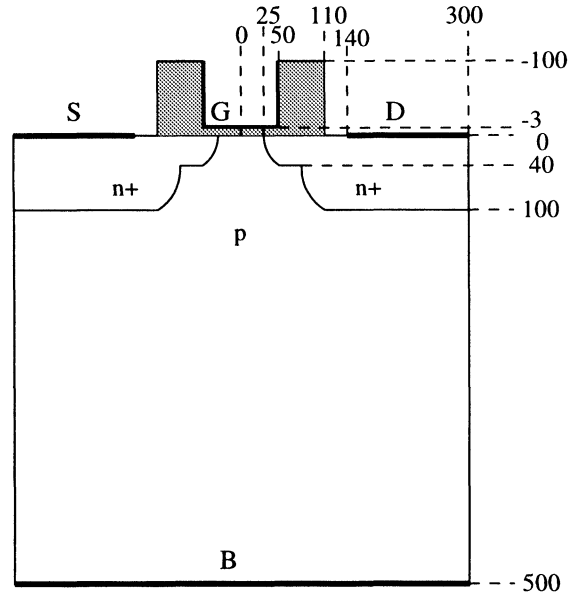

FIGURE 3 Structure of the simulated *n*-MOSFET. The maximum *n*-type dopings are $N_D = 1.5 \times 10^{20}\,cm^{-3}$ and $N_D = 5 \times 10^{19}\,cm^{-3}$, respectively, and the constant *p*-type doping is $N_A = 1 \times 10^{18}\,cm^{-3}$. The measure in the figure is *nm*.

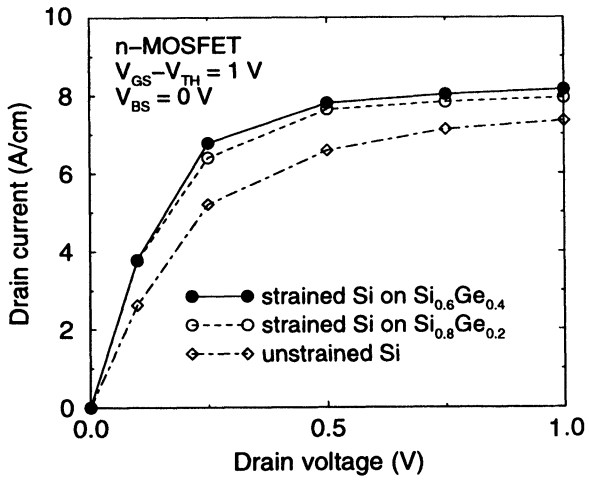

FIGURE 4 DC output characteristics of an *n*-MOSFET with a metallurgical channel length of 50 nm in unstrained Si and in strained Si grown on a $Si_{0.8}Ge_{0.2}$ and a $Si_{0.6}Ge_{0.4}$ substrate, respectively.

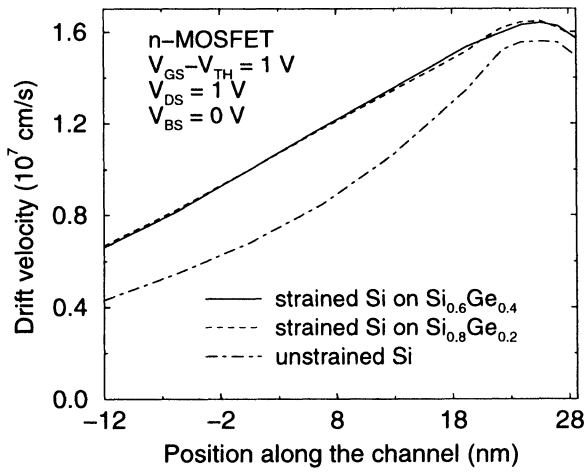

FIGURE 6 Average drift velocity along the channel of an *n*-MOSFET in unstrained Si and in strained Si grown on a $Si_{0.8}Ge_{0.2}$ and a $Si_{0.6}Ge_{0.4}$ substrate, respectively.

starts in the case of strained silicon at lower drain voltages than in the unstrained case.

In spite of appreciably different drain currents in the unstrained and strained case (also present in the DD model), the profile of the longitudinal field (averaged perpendicular to the gate-oxide interface by the relative electron density) in Figure 5 remains almost unchanged. In conjunction with the velocity profile in Figure 6, this demonstrates that the different performance originates mainly from different transport properties. In this respect, the output characteristics in figure together with the velocity-field characteristics in Figure 2 confirm that the bulk low-field mobility remains also in the submicron regime a key indicator for the performance of *n*-MOSFETS based on strained Si, irrespective of the velocity overshoot phenomena present at the drain side of the channel. In fact, despite identical saturation velocities, the drain current is appreciably enhanced while moderate changes of the bulk velocities at medium field strengths have only a minor influence. This is agreement with Ref. [19] where the decisive influence on the saturation drain current was also traced back to the low-field mobility.

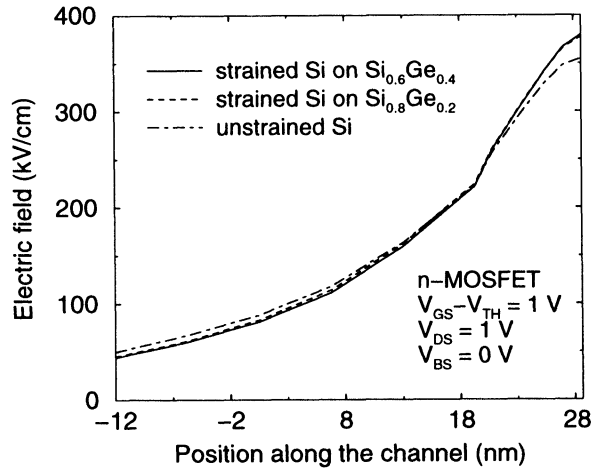

FIGURE 5 Average longitudinal electric field along the channel of an *n*-MOSFET in unstrained Si and in strained Si grown on a $Si_{0.8}Ge_{0.2}$ and a $Si_{0.6}Ge_{0.4}$ substrate, respectively.

IV. CONCLUSIONS

The strain-dependence of electron-transport in bulk Si and deep-submicron MOSFETs has been investigated by full-band Monte Carlo simulation, which enables an accurate description of transport properties and avoids for example the artificial negative slope of the velocity-field characteristics

present in analytical band models (see, *e.g.*, the comparison in Ref. [10]). On the bulk level, there is still an appreciable increase of the drift velocity at medium field strengths above a substrate germanium-content of 20%, where the low-field mobility saturates, whereas the saturation velocity does not change at all under strain. In contrast, on the device level, the saturation drain current is significantly increased under strain, but only up to a Ge-content of 20% demonstrating that the low-field mobility is a key indicator of device performance in the submicron regime.

Acknowledgment

We would like to thank M. Lundstrom and A. Wettstein for useful discussions as well as M. M. Rieger for calculating the band structures.

References

[1] König, U., Zeuner, M., Höck, G., Hackbarth, T., Glück, M., Ostermann, T. and Saxarra, M. (1999). "*n*- and *p*-type SiGe HFETs and circuits", *Solid-State Electron.*, **43**, 1383–1388.

[2] Roy, S., Kaya, S., Asenov, A. and Barker, J. R., "RF analysis methodology for Si and SiGe FETs based on transient Monte Carlo simulation", In: *Proc. SISPAD*, Kyoto (Japan), Sept. 1999, pp. 147–150.

[3] Dollfus, P. (1997). "$Si/Si_{1-x}Ge_x$ heterostructures: Electron transport and field-effect transistor operation using Monte Carlo simulation", *J. Appl. Phys.*, **82**, 3911–3916.

[4] Formicone, G. F., Vasileska, D. and Ferry, D. K. (1997). "Modeling of submicron $Si_{1-x}Ge_x$-based MOSFETs by self-consistent Monte Carlo simulation", *Phys. Status Solidi B*, **204**, 531–533.

[5] Keith, S., Bufler, F. M. and Meinerzhangen, B. (1997). "Full band Monte-Carlo device simulation of an 0.1 μm *n*-channel MOSFET in strained silicon material", In: *Proc. ESSDERC*, Grünbacher, H. Ed., Stuttgart, **27**, 200–203, Editions Frontières.

[6] Rieger, M. M. and Vogl, P. (1993). "Electronic-band parameters in strained $Si_{1-x}Ge_x$ alloys on $Si_{1-y}Ge_y$ substrates", *Phys. Rev. B*, **48**, 14276–14287.

[7] Jacoboni, C. and Reggiani, L. (1983). "The Monte Carlo method for the solution of charge transport in semiconductors with application to covalent materials", *Rev. Mod. Phys.*, **55**, 645–705.

[8] Sadek, A. and Ismail, K. (1995). "Si/SiGe CMOS possibilities", *Solid-State Electron.*, **38**, 1731–1734.

[9] Ismail, K., Nelson, S. F., Chu, J. O. and Meyerson, B. S. (1993). "Electron transport properties of Si/SiGe heterostructures: Measurements and device implications", *Appl. Phys. Lett.*, **63**, 660–662.

[10] Bufler, F. M., Graf, P., Keith, S. and Meinerzhagen, B. (1997). "Full band Monte Carlo investigation of electron transport in strained Si grown on $Si_{1-x}Ge_x$ substrates", *Appl. Phys. Lett.*, **70**, 2144–2146.

[11] Bufler, F. M., Yoder, P. D. and Fichtner, W. "Simple phase-space trajectory calculation for Monte Carlo device simulation including screened impurity scattering", In: *Proc. SISPAD*, Kyoto (Japan), Sept. 1999, pp. 31–34.

[12] Darwish, M. A., Lentz, J. L., Pinto, M. R., Zeitzoff, P. M., Krutsick, T. J. and Vuong, H. H. (1997). "An improved electron and hole mobility model for general purpose device simulation", *IEEE Trans. Electron Devices*, **44**, 1529–1538.

[13] Fischetti, M. V. and Laux, S. E. (1988). "Monte Carlo analysis of electron transport in small semiconductor devices including band-structure and space-charge effects", *Phys. Rev. B*, **38**, 9721–9745.

[14] Van de Walle, C. G. (2000). "Strain effects on the valence-band structure of SiGe", In: *Properties of Silicon Germanium and SiGe:Carbon*, Kasper, E. and Lyutovich, K. Eds. No. 24 in EMIS Datareviews Series, pp. 135–139, London: INSPEC, IEE, 2000.

[15] Sah, C. T., Ning, T. H., and Tschopp, L. L. (1972). "The scattering of electrons by surface oxide charges and by lattice vibrations at the silicon-silicon dioxide interface", *Surf. Sci.*, **32**, 561–575.

[16] Roldán, J. B., Gámiz, F., López-Villanueva, J. A. and Carceller, J. E. (1996). "A Monte Carlo study on the electron-transport properties of high-performance strained-Si on relaxed $Si_{1-x}Ge_x$ channel MOSFETs", *J. Appl. Phys.*, **80**, 5121–5128.

[17] John, S., Ray, S. K., Quinones, E. and Banerjee, S. K. (1999). "Strained Si n-channel metal-oxide-semiconductor transistor on relaxed $Si_{1-x}Ge_x$ formed by ion implantation of Ge", *Appl. Phys. Lett.*, **74**, 2076–2078.

[18] Sugii, N., Nakagawa, K., Yamaguchi, S. and Miyao, M. (1999). "Role of $Si_{1-x}Ge_x$ buffer layer on mobility enhancement in a strained-Si *n*-channel metal-oxide-semiconductor field-effect transistor", *Appl. Phys. Lett.*, **75**, 2948–2950.

[19] Houlet, P., Awano, Y. and Yokoyama, N. (1999). "Influence of non-linear effects on very short *p*MOSFET device performances", *Physica B*, **272**, 572–574.