Simulation of 0.35 μm /0.25 μm CMOS Technology Doping Profiles

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A careful calibration of a continuum process simulator is normally required to achieve a good agreement between simulated results and experimental dopant profiles. However, the validity of such a calibration procedure is often limited to a particular technology. By taking into account a number of physics-based models and experimental results available in literature, the predicting capability of the process simulation has been conveniently improved. In particular, this paper shows how concentration-depth profiles from two different CMOS technologies have been successfully reproduced with a unique set of fitting parameters.

Keywords: Process simulation; Ion implantation; Dopant diffusion; Secondary Ion Mass Spectroscopy; Damage distribution; Point defects

INTRODUCTION

Predictive device simulation requires, as a prerequisite, an accurate description of the impurity concentrations in silicon; this, in turn, asks for a reliable modelling of the primary fabrication processes, such as ion implantation and dopant diffusion, which determine the concentration-depth profiles. Due to the still partial understanding of the solid-state physics and chemistry which underlies process models, a careful calibration of a process-modelling tool is needed in order to achieve a reasonably good agreement between simulated results and experimental data. The validity of such a calibration procedure is frequently limited to a particular technology.

In this work, by taking into account a number of physics-based models and experimental results available in literature, concentration-depth profiles from two different actual technologies have been accurately reproduced by using the TSUPREM-4 [1] process simulator with a unique set of fitting parameters. At first, boron and phosphorous channel profiles, as well as source/drain n^+ profiles, have been simulated for a 0.35 μm CMOS technology. Simulation results have been compared against experimental dopant profiles to calibrate the simulator. Next, this calibrated version of TSUPREM-4 has been successfully checked by simulating profiles of the same dopant species for a 0.25 μm CMOS technology. Finally, a number of transfer characteristics of n-channel

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transistors with different channel lengths have been reproduced, indicating the Technology Computer Aided Design (TCAD) accuracy. In this way a large confidence in the applied methodology has been established, which can be applied for further downscaling of the technologies.

SIMULATION RESULTS AND COMPARISON WITH EXPERIMENTS

Concentration profiles have been obtained by Secondary Ion Mass Spectroscopy (SIMS) on test wafers from actual CMOS technologies, after front-end processing, *i.e.*, just before silicidation. They have been compared to the results of process simulations with the fully coupled dopant-defect diffusion model available in TSUPREM-4. These simulations took into account all relevant process steps and assumed default point-defect diffusivity and equilibrium concentration.

The n-channel profiles (Figs. 1 and 2) show a good overall agreement between SIMS data and simulation results (with the as-implanted profiles modelled with the Monte Carlo approach),

FIGURE 1 SIMS and simulated boron profile for a 0.35 μm CMOS technology. The channel profile resulted from $1 \times 10^{13} \text{ cm}^{-2}$ dose, 180 keV, $5 \times 10^{12} \text{ cm}^{-2}$ dose, 90 keV and $4 \times 10^{12} \text{ cm}^{-2}$ dose, 25 keV boron implants.

FIGURE 2 SIMS and simulated boron profile for a 0.25 μm CMOS technology. The channel profile resulted from $1.8 \times 10^{13} \text{ cm}^{-2}$ dose, 180 keV and $6.5 \times 10^{12} \text{ cm}^{-2}$ dose, 25 keV boron implants.

although with some minor deviations near the surface. However, because conventional SIMS is generally less accurate near the surface, we simulated boron annealing after implant by assuming default diffusivities and by modelling the trapping of implanted ions at the Si-SiO₂ interface as proposed by Oh and Ward [2], without any attempt to fit the data in the near-surface region.

Source/drain n⁺ profiles have been simulated as follows. To reduce the computational workload, arsenic and phosphorous as-implanted profiles have been modelled by a Pearson IV distribution. Furthermore, the channelling contribution has been neglected since these impurities are implanted through a screening oxide. As for the ion-generated damage distribution, the net excess of interstitials has been described by adopting an effective “+n” factor, which depends on energy and ion mass as recently proposed in [3]. Such an amount of interstitials induces Transient Enhanced Diffusion (TED) during annealing just after ion implantation, and causes a large spreading of the dopant beyond the implanted region.

The simulation accurately predicts the junction depth (Figs. 3 and 4). The calculated boron

FIGURE 3 Source/drain n^+ profiles for a $0.35\mu\text{m}$ CMOS technology. A $5 \times 10^{13}\text{cm}^{-2}$ dose, 20 keV phosphorous implant is annealed at 850°C for 30 min. Then, a $4 \times 10^{15}\text{cm}^{-2}$ dose, 75 keV arsenic implant is annealed at 850°C for 30 min and at 1100°C for 10 s.

FIGURE 4 Source/drain n^+ profiles for a $0.25\mu\text{m}$ CMOS technology. A $1.2 \times 10^{14}\text{cm}^{-2}$ dose, 40 keV arsenic implant is annealed at 970°C for 10 s and at 850°C for 30 min. Then, a $4 \times 10^{15}\text{cm}^{-2}$ dose, 70 keV arsenic implant is annealed at 900°C for 10 min and at 1070°C for 10 s.

distribution in the n^+ region shows some deviations with respect to the experimental profile; such deviations, however, clearly do not affect the net

doping concentration. As for the phosphorous profile, one cannot fit the entire curve by accounting for interstitials only, as in the intrinsic region; to match the SIMS profile, an additional vacancy mechanism has been introduced, as recently suggested [4, 5]. Such a modification still allows one to match the experimental data available for the intrinsic case, as shown in Figure 5. The diffusivities of arsenic and phosphorous used throughout the process simulations are shown in Table I.

The accuracy of the process simulator has been subsequently evaluated by reproducing a number of electrical transistor characteristics, taken from devices having different channel lengths. In particular, we considered transfer characteristics at different substrate voltages, aiming at reproducing the subthreshold slope and the threshold voltages. In long-channel devices, these quantities are mainly determined by the channel profile, while the influence of the lateral diffusion of the source/drain profiles is negligible. In short-channel devices, a wrong estimate of the effective channel length may lead to a large deviation in the simulated threshold voltage when compared to the measured one. Typically, the magnitude of the

FIGURE 5 SIMS and simulated phosphorous profile for a $0.35\mu\text{m}$ CMOS technology. The channel profile resulted from $8 \times 10^{12}\text{cm}^{-2}$ dose, 450 keV, $2.5 \times 10^{12}\text{cm}^{-2}$ dose, 220 keV and $5.5 \times 10^{12}\text{cm}^{-2}$ dose, 70 keV phosphorous implants.

TABLE I Parameter set used in the TSUPREM-4 simulations. Activation energies for arsenic have been taken from [6], whereas those for phosphorous have been taken from [7, 8]. Pre-exponential coefficients have been adjusted to fit the experimental profiles. The fractional interstitialcy component of diffusion for arsenic has been taken from [9], whereas that for phosphorous in the intrinsic region is taken from [10]

Species	Pre-exponential [cm ² /s]	Activation energy [eV]
AsI ⁰	0.07	3.44
AsV ⁰	0.13	3.44
AsI ⁻	7	4.05
AsV ⁻	13	4.05
PI ⁰	5.76	3.66
PV ⁰	0.24	3.66
PI ⁻	5.77	4.0
PV ⁻	5.77	4.0
PI ⁼	5×10^{-5}	2.9
PV ⁼	5×10^{-5}	2.9

FIGURE 6 Transfer characteristics of a 0.35 μm n-channel MOS transistors at $V_{ds} = 0.1$ V.

deviation increases when a back-bias is applied to the transistor, indicating inaccuracies in the lateral junction profile. The simulated oxide thickness compares very well to the measured one, and a good agreement between experimental data and simulation results for all channel lengths has been obtained after calibrating only the work function difference between the gate and the

silicon. A single value for it has been used throughout all device simulations. As an example, Figure 6 shows a comparison between the measured and simulated transfer characteristics for a 0.35 μm n-channel MOS transistor. The good agreement indicates the overall accuracy of the process simulation.

CONCLUSION

A number of concentration-depth profiles from actual CMOS technologies have been reasonably reproduced using TSUPREM-4 with a single parameter set. To improve the predicting capability of the process simulation, we determined such a set by taking into account the data available in literature and by considering physics-based models for ion implantation and dopant diffusion. In general, default parameters for boron have been successfully used, whereas diffusivities of arsenic and phosphorous have been adjusted to match the SIMS profiles. The accuracy of the calibrated version of TSUPREM-4 has been finally evaluated by reproducing a number of electrical transistor characteristics, measured on devices having different channel lengths. As the predictability of the simulations appeared rather good, the calibrated process simulator can be conveniently used for an exploratory investigation of further scaled-down technologies.

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