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Defect Level Estimation for Pseudorandom Testing Using Stochastic Analysis*

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Pseudorandom testing has been widely used in built-in self-testing of VLSI circuits. Although the defect level estimation for pseudorandom testing has been performed using sequential statical analysis, no closed form can be accomplished as complex combinatorial enumerations are involved. In this work, a Markov model is employed to describe the pseudorandom test behaviors. For the first time, a closed form of the defect level equation is derived by solving the differential equation extracted from the Markov model. The defect level equation clearly describes the relationships among defect level, fabrication yield, the number of all input combinations, circuit detectability (in terms of the worst single stuck-at fault), and pseudorandom test length. The Markov model is then extended to consider all single stuck-at faults, instead of only the worst single stuck-at fault. Results demonstrate that the defect level analysis for pseudorandom testing by only dealing with the worst single stuck-at fault is not adequate (In fact, the worst single stuck-at fault analysis is just a special case). A closed form of the defect level equation is successfully derived to incorporate all single stuck-at faults into consideration. Although our discussions are primarily based on the single struck-at fault model, it is not difficult to extend the results to other fault types.

Keywords: Defect level analysis; Random testing; Pseudorandom testing; Markov model; Differential equations

1. INTRODUCTION

Defect level (DL) is an important indicator of test quality, and is defined as the percentage of a product, such as a chip, that is defective and is shipped for use after test. Thus, high DL in a product is not acceptable, especially, for the design of highly reliable systems. Low DL can be achieved by either increasing the fabrication yield or enhancing the defect coverage of circuit testing. However,

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VLSI manufacturing is subject to process contaminations which makes perfect yield impossible. Ideally, testing should be performed to detect all chips that contain defects. But, there are too many different defect types as the fabrication density of VLSI circuits keeps increasing. Instead of trying to detect all defects, testing process is designed to achieve a tolerable DL under constraints such as test application time, test generation time, and test storage. Built-In Self-Testing (BIST) has been one of the most promising alternatives to achieve high test quality using limited test resources [1, 2]. The main idea of BIST is to have the chip test itself. Pseudorandom self-testing is a very popular BIST technique [3, 4], which has been successfully applied to many commercial products [5, 6].

Pseudorandom testing deals with testing a circuit with test patterns that have many characteristics of random patterns, but the entire test sequence is generated deterministically using built-in digital devices such as linear feedback shift registers (LFSRs) [2, 4, 7]. Thus, the entire test sequence can be regenerated by giving the same state or seed value. Pseudorandom patterns can be generated with or without test vector repetitions depending on the test length and the circuit structure of test pattern generators. If the circuit under test (CUT) is a combinational circuit and the faults do not induce any sequential behavior, then pseudorandom patterns without test pattern repetition are preferred to increase the fault detection probabilities. In this work, we assume that the CUT is a combinational circuit or a sequential circuit with full scan design, and faults occurring will not induce any sequential behavior. Thus, the DL analysis using pseudorandom test patterns without test vector repetition will be investigated.

The DL estimation for pseudorandom testing has been thoroughly studied in [8] using the technique of sequential statistical analysis [9]. Many important DL properties under pseudorandom testing have been identified; unfortunately, no closed form can be derived to well describe the relationships among DL, pseudorandom test length, fabrication yield, the number of all possible test patterns, and the CUT testability. The difficulty of deriving a closed form for the DL equation lies in the involvement of very complex combinatorial enumerations. Thus, deriving the DL of pseudorandom testing relies on computer enumeration which is not only time-consuming but also inaccurate (because of intolerable numerical errors accumulated during the enumeration process). Additionally, the previous analysis in [8] is mainly based on the worst fault analysis which is not adequate as far as high test quality is concerned.

In this paper, the DL analysis for pseudorandom testing is considered from a different viewpoint which successfully avoids the tedious computer enumeration process. First, a Markov model [9] is proposed to describe the pseudorandom test behavior and a simple differential equation is extracted from this model. A closed form for the DL equation can then be derived by solving the differential equation. Of course, the differential equation extracted does not faithfully reflect the real situation since pseudorandom test patterns are discrete. However, the test patterns are virtually continuous as more and more test vectors are applied (generally, on the order of several millions). Our results demonstrate that the approximation is very accurate and computationally cost-effective. The deviation induced by the differential approximation is almost negligible, when the number of pseudorandom test patterns is large.

Most investigations to the DL analysis of pseudorandom testing are mainly using the worst or average single stuck-at fault detectability, and this is inadequate as far as high test quality is concerned [10]. To solve this problem, the proposed Markov model is extended to incorporate all single stuck-at faults into consideration. A closed form is also obtained to illustrate the relationships among DL, pseudorandom test length, fabrication yield, the number of all possible test patterns, the CUT testability, and the number of single stuck-at faults significantly contributing to DL. Results show that the worst single stuck-at fault analysis is just a special case of the all single stuck-at fault analysis. The deviation can be very

significant when the number of low-detectability faults is large. In fact, analysing the DL of pseudorandom testing by considering all low-detectability faults which are weighted by the probabilities of their occurrence can dramatically enhance the test quality. Although the discussions mainly focus on single stuck-at faults, the results can be easily extended to other fault types as long as their corresponding detectabilities can be derived.

This paper is organized as follows. Section 2 gives the required background on DL analysis, and Section 3 presents the Markov model and the DL analysis for pseudorandom testing based on the worst single stuck-at fault assumption. Results are then extended to consider all single stuck-at faults in Section 4. Section 5 discusses the impacts of fault model, fault occurrence, fault distribution, and fault coverage distribution to the DL analysis. Concluding remarks are given in Section 6.

2. BACKGROUND

The DL of circuit testing is the probability of shipping defective products, and its value should be controlled to be as small as possible. If the number of defective products shipped for use among the total number of products shipped is known, then the DL can be estimated using the following equation

$$DL = \frac{\textit{Number of defective products shipped}}{\textit{Total number of products shipped}} \quad (1)$$

In [11], the DL of circuit testing is determined as a function of fault coverage (the fraction of faults detected) and yield based on the following assumptions:

(1) The chip has exactly n faults and m of them are tested;
(2) The probability of a fault occurring is independent of whether any other fault has occurred or not; and
(3) Each fault has an equal probability of occurring.

The assumptions ensure the uniform distribution of faults. Equation (2) shown below is derived using probability theory

$$DL = 1 - Y^{1-T} \quad (2)$$

where Y is the fabrication yield and T is the single stuck-at fault coverage. Equation (2) can be employed to find the DL of a testing method, if the yield and fault coverage are both known. Fault coverage is available for deterministic test generation methods or random testing supported by fault simulation [2, 7]. Equation (2) also shows that DL is exponentially related to fault coverage.

The deterministic DL analysis of [11] was extended to random testing in [12], which provides an equation relating DL, yield, random test length, and susceptibility. Based on the observations from results of many different examples, it is concluded that random pattern testability is a function of the number of random patterns, and that all examples have the same basic shape. The function describing the basic shape – an exponential response as in a RC circuit – is then employed to approximate the relationship between fault coverage and random test length by the equation

$$\begin{aligned} T &= 1 - e^{-\ln(N)/\log_{10}\alpha \ln 10} \\ &= 1 - N^{-1/\log_{10}\alpha \ln 10} \end{aligned} \quad (3)$$

where N is the number of random patterns applied and α is the fault susceptibility constant. Finally, by combining Eqs. (2) and (3), the DL for random testing is derived as

$$DL = 1 - Y^{N^{-1/\log_{10}\alpha \ln 10}} \quad (4)$$

The *curve fitting* of random testing using a statistical sampling plan has also been described, and it allows one to deduce the number of random patterns required to give a specified DL with a known yield. Experimental data suggest the validity of the DL model for random testing. Note that α is estimated using fitting methods [12].

In [8], the technique of *sequential statistical analysis* was employed as a vehicle to derive the relationship among DL, yield, random test length and detection probability. Instead of using the deterministic DL analysis as a bridge as in [12], sequential statistical analysis directly examines the random test behavior and results in a simple derivation for the DL estimation. The susceptibility constant (α) used in [12] is replaced by the worst detection probability, σ, using the single stuck-at fault model. The DL of random testing obtained is given by equation

$$DL = \frac{(1-\sigma)^x(1-Y)/Y}{1+(1-\sigma)^x(1-Y)/Y} \tag{5}$$

where x is the random test length. The technique of sequential statistical analysis was then extended to pseudorandom testing in which no test patterns can be repeated. It has been established that the DL of pseudorandom testing is no larger than that of random testing, if the CUT is a combinational circuit and faults do not result in any sequential behavior. The DL of pseudorandom testing can be represented by the following equation

$$DL = \frac{[\prod_{i=1}^{i=x}(1-\beta/(M-x+i))](1-Y)}{(1-(\beta/M)(1-Y)) - \sum_{i=1}^{i=x-1}\beta/(M-x+i)[(1-\beta/(M-x+i+1))\cdots(1-\beta/M)(1-Y)]} \tag{6}$$

where M is the total number of input combinations, and β is the number of test patterns detecting the worst single stuck-at fault. Due to the complex combinatorial enumeration, the above equation cannot be further manipulated to a closed form [8]. Thus, computer enumeration, which is not only time-consuming but also inaccurate, is resorted to derive the DL of pseudorandom testing. The purpose of this work is to alleviate this difficulty by obtaining a closed form for the DL analysis of pseudorandom testing using stochastic analysis.

All previously mentioned methods estimate the DL of circuit testing in terms of fault coverage or detection probability to reflect the testability of the CUT. It is also possible to analyze the DL of circuit testing based on wafer test data [13]. In this approach, the data on the measured fraction of failing chips *versus* the number of test vectors is used to empirically determine a failure probability density function. True yield and DL (or reject ratio) can then be estimated without fault coverage or detection probability analysis. Since the tested product quality is directly evaluated from test data, the need for complex fault models and fault analysis has been eliminated. Other important DL analysis methods or practices can be found in [14–20].

3. WORST FAULT ANALYSIS OF PSEUDORANDOM TESTING

Stochastic analysis has been widely used in sequential circuit testing [21] and built-in self-testing [22]. Theoretically, pseudorandom testing also has stochastic behavior since the detection probability of each pseudorandom test pattern depends on whether its predecessor detects the fault or not. If test pattern t_i does not detect fault f, then test pattern t_{i+1} has higher probability of detecting f. Pseudorandom testing can be well described using a discrete stochastic model, since the test patterns are applied one by one. Unfortunately, discrete models generally lead to the difficulty of solving difference equations as in [8]. In this work, we use a continuous stochastic model which results in easily solvable differential equations. This solution is appropriate since the deviation between discrete modeling and continuous modeling can be ignored, if the number of pseudorandom test patterns applied is large. In the BIST design of VLSI circuits, the number of pseudorandom test patterns applied is generally on the order of at least several millions. Thus, the

continuous stochastic analysis is very accurate as results demonstrate later.

To simplify the analysis, we introduce some notation and terminology that will be utilized.

Fault Spaces ω: $\omega = w_0, w_1$. The set ω denotes whether the CUT is defective or defect-free. Let w_0 denote the defect-free circuit condition, and w_1 the condition of the circuit being defective. For ease of discussion, a single stuck-at fault model is assumed. However, the general case can be implied.

Test Set τ: $\tau = t_1, t_2, \ldots, t_m$. τ is a set of pseudorandom test patterns. Thus, $t_i = 0$ or 1 for $1 \le i \le m$.

Detection Set γ: $\gamma = T_1, T_2, \ldots, T_m$. If test patterns $t_1, \ldots, t_j$ are applied to the CUT and the circuit fails, that is, the observed outputs are different from those of the fault-free circuit, the value of T_j is defined to be 1. On the other hand, if test patterns $t_1, \ldots, t_j$ do not cause the CUT to fail, that is, the CUT produces an output sequence identical to that of the fault-free circuit, then the value of T_j is defined to be 0.

A Priori Probabilities $P(w_i)$, $0 \le i \le 1$: Here $P_i = P(w_i)$, $0 \le i \le 1$, denotes the a priori probability that the circuit is in state w_i. In particular, $P_0 = P(w_0)$ is the a priori probability that the circuit is fault-free, while $P_1 = P(w_1)$ is the a priori probability that the circuit is faulty. The values of the P_i's are assumed to be known, since they can be obtained empirically from the information supplied by the manufacturer, or from experimental data. Note $P_0 + P_1 = 1$ and P_0 is the fabrication yield Y of a manufacturing process.

Using the above definitions and notations, the defect level of circuit testing can be formulated as

$$DL = \frac{P(T_x = 0|w_1)P(w_1)}{[P(T_x = 0|w_0)P(w_0) + P(T_x = 0|w_1)P(w_1)]} \tag{7}$$

Obviously, we have $P(T_x = 0|w_0) = 1$. From the above equation, it can be observed that the major difficulty on DL analysis lies in the derivation of $P(T_x = 0|w_1)$, the escape probability. Instead of using sequential statistical analysis and solving a set of recurrence relations as in [8], we concentrate on dealing with the escape probability analysis, $P(T_x = 0|w_1)$, for x pseudorandom test patterns. The result is then employed to solve Eq. (7).

In order to investigate the fault detection behavior under pseudorandom testing, a stochastic model with two states S_0 and S_1 is established. As shown in Figure 1, S_0 represents the state in which the (worst) fault has not been detected and S_1 corresponds to the detection of the fault. We also assume that the total number of pseudorandom test patterns is M, the number of pseudorandom test patterns that have been applied is x, and the worst fault can be detected by β pseudorandom test patterns as in [8]. When pseudorandom testing proceeds, state transition probabilities keep changing because no test pattern can be repeated. For example, the state transition probability from S_0 to S_1 is $(\beta/(M - x + 1))$ and the probability is increased as more and more patterns are applied (*i.e.*, x is larger and larger). Other state transitions can be discussed similarly.

The following differential equation can be extracted from the Markov model, to describe the relationship of the state probabilities.

$$\frac{dS_0(x)}{dx} = -\frac{\beta}{M - x + 1} S_0(x) \tag{8}$$

The initial condition (*i.e.*, the initial state probabilities) is $S_0(0) = 1$ and $S_1(0) = 0$. It should be noted that S_i denotes either state i or the probability of state i without causing confusion. The analytical solution of Eq. (8), subject to the

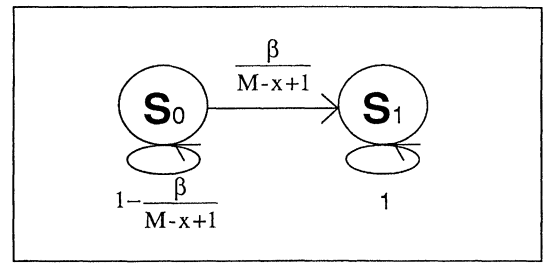

FIGURE 1 The Markov model for pseudorandom testing.

initial condition, is finally given as

$$S_0(x) = \left(\frac{M - x + 1}{M + 1}\right)^{\beta} \tag{9}$$

The detection probability is $S_1(x)$ and the escape probability is $S_0(x)$, and $S_1(x) = 1$ corresponds to the detection of the worst fault. Thus, we have

$$P(T_x = 0|w_1) = \left(\frac{M - x + 1}{M + 1}\right)^{\beta} \tag{10}$$

Substituting the above equation into Eq. (7), we have

$$DL_s = \frac{((M - x + 1)/(M + 1))^{\beta}(1 - Y)}{Y + ((M - x + 1)/(M + 1))^{\beta}(1 - Y)} \tag{11}$$

where DL_s denotes the DL value derived using the proposed differential analysis based on the stochastic model. The above representation for the DL analysis of pseudorandom testing is much simpler than its discrete counterpart given by Eq. (6).

Deriving the DL for pseudorandom testing using Eq. (6) is not economical at all, even worse, the numerical error accumulated is not tolerable in large test cases (*e.g.*, M is on the order of millions and a long pseudorandom test sequence has been applied). Figures 2a, 2b, and 2c show a sample of results which provides the relationship among DL, detectability, yield, the pseudorandom test length applied, and the total number of pseudorandom test patterns, under different circumstances. Equation (11) also reveals that the DL of circuit testing can be reduced by: (1) increasing the fabrication yield, (2) increasing the detectability, or (3) increasing the pseudorandom test length. The fabrication yield can be increased by improving the manufacturing deficiencies, while the detectability can be enhanced using design-for-testability techniques [2]. It appears that enhancing the circuit detectability or applying longer test sequence is more beneficial than increasing the fabrication yield, since the relationship between DL and β, x is an exponential function (however, the relationship between DL and Y is linear). Of course, design-for-testability techniques need expensive hardware

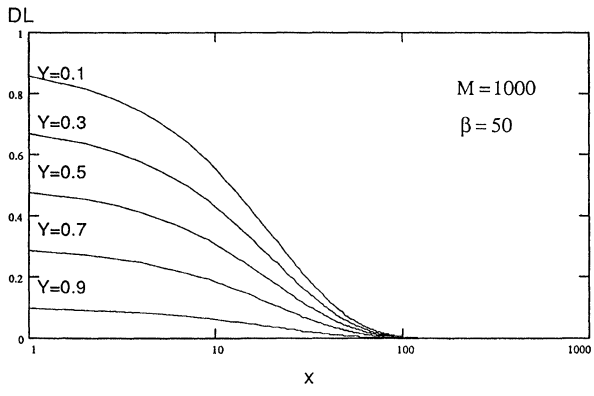

FIGURE 2a DL of pseudorandom testing: $\beta = 50$.

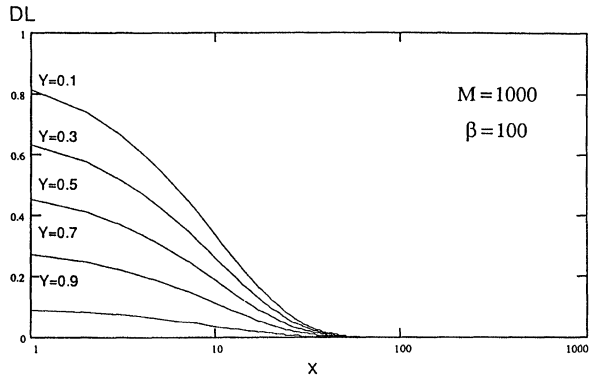

FIGURE 2b DL of pseudorandom testing: $\beta = 100$.

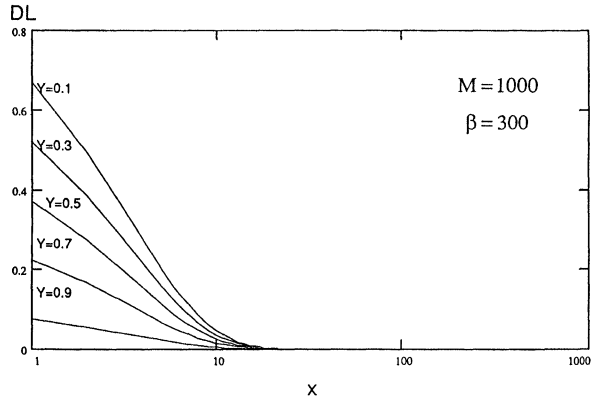

FIGURE 2c DL of pseudorandom testing: $\beta = 300$.

overhead and applying longer test sequence increases test costs.

The major difference between the proposed differential solution and [8] lies in using different strategies to derive $P(T_x=0|w_1)$. If Eq. (8) is solved as a difference equation, then the probability of state S_0 can be determined as

$$S_0(x)=\prod_{t=1}^{t=x}\left(1-\frac{\beta}{M-t+1}\right) \tag{12}$$

The above discrete solution involves very tedious computational enumerations, which can be very time-consuming and inaccurate. Especially, numerical errors accumulated after million times (or more) of divisions and multiplications will be intolerable. The DL thus derived using the discrete solution can be represented by

$$DL_d=\frac{\left[\prod_{t=1}^{t=x}(1-\beta/(M-t+1))\right](1-Y)}{Y+\left[\prod_{t=1}^{t=x}(1-\beta/(M-t+1))\right](1-Y)} \tag{13}$$

where DL_d denotes the DL derived using discrete analysis. It can be found that the above equation is a simpler form of Eq. (6). To investigate the deviation between the difference and differential solutions, we must concentrate on Eqs. (9) and (12). By the difference solution, the escape probability, $S_0(x)$, equals 0 if $x=M-\beta+1$; and this is the real case for pseudorandom testing. Substituting $x=M-\beta+1$ into Eq. (9), the escape probability using the differential solution can be represented as

$$\left(\frac{\beta}{M+1}\right)^{\beta} \tag{14}$$

It is interesting to find that the above equation approaches 0 regardless of the value of β, when M is large. This demonstrates that the proposed differential solution is rather accurate around the zero-escape point. Table I also lists a sample of values for Eq. (14) under $M=1{,}000{,}000$ and 2,000,000, for several different β values.

TABLE I Deviations of the difference and differential solutions around the zero-escape point

M	β	Zero-escape value
1000000	1	9.999990e−07
1000000	2	3.999992e−12
1000000	3	2.699992e−17
1000000	4	2.559990e−22
1000000	5	3.124984e−27
1000000	6	4.665572e−32
2000000	1	4.999998e−07
2000000	2	9.999990e−13
2000000	3	3.374995e−18
2000000	4	1.599997e−23
2000000	5	9.765601e−29
2000000	6	7.289978e−34

We have also found that the differential solution provides an upper bound for the escape probability of pseudorandom testing. This can be verified by the following lemmas and theorem.

LEMMA 1 $(M-\beta)(M+1)^{\beta}<M^{\beta+1}$ *for* $M>0$ *and* $\beta>0$.

Proof The lemma can be proved by induction on β. Since $(M-1)(M+1)<M^2$, the lemma holds for $\beta=1$. Assume the lemma is true for $\beta=k$, we have $(M-k)(M+1)^k<M^{k+1}$. For $\beta=k+1$, we must prove $(M-k-1)(M+1)^{k+1}<M^{k+2}$. By rearranging the left-hand side of the equation and using the induction hypothesis, we have $(M-k)(M+1)^{k+1}-(M+1)^{k+1}<M^{k+1}-(M+1)^{k+1}<0<M^{k+2}$.

LEMMA 2 $(M-f+1)^{\beta}(M-f-\beta)<(M-f)^{\beta+1}$ *for* $M\geq f>0$, *and* $\beta>0$.

Proof Again, the lemma can be proved by induction on β. In fact, this lemma degenerates to Lemma 1 if $M-f$ is replaced by M.

THEOREM 1 $\prod_{t=1}^{t=x}(1-\beta/(M-t+1))<((M-x+1)/(M+1))^{\beta}$ *for* $M\geq x>0$, *and* $\beta>0$.

Proof The theorem can be proved by induction on x. If there is only one test pattern applied (*i.e.*, $x=1$), we have $(1-\beta/M)<(M/(M+1))^{\beta}=M^{\beta}/(M+1)^{\beta}$. This is to verify $(M-\beta)(M+1)^{\beta}<M^{\beta+1}$ which has been proved in Lemma 1. Now, suppose

the theorem holds for $x=f$, we have $(1-\beta/M)(1-\beta/(M-1))\cdots(1-\beta/(M-f+1)) < ((M-f+1)/(M+1))^{\beta}$. Suppose $f+1$ pseudorandom test patterns have been applied, we must verify $(1-\beta/M)(1-\beta/(M-1))\cdots(1-\beta/(M-f+1))(1-(\beta/(M-f)) < ((M-f)/(M+1))^{\beta}$. This can be done by manipulating the equation as follows.

$$\begin{aligned}
&\left(1-\frac{\beta}{M}\right)\left(1-\frac{\beta}{M-1}\right)\\
&\quad\cdots\left(1-\frac{\beta}{M-f+1}\right)\left(1-\frac{\beta}{M-f}\right)\\
&\qquad<\left(\frac{M-f+1}{M+1}\right)^{\beta}\left(1-\frac{\beta}{M-f}\right)\\
&\qquad=\left(\frac{M-f+1}{M+1}\right)^{\beta}\left(\frac{M-f-\beta}{M-f}\right)\\
&\qquad<\frac{(M-f)^{\beta+1}}{(M+1)^{\beta}(M-f)}\quad\text{(By Lemma 2)}\\
&\qquad=\left(\frac{M-f}{M+1}\right)^{\beta}.
\end{aligned}$$

Note that the equality condition of the above theorem holds when $\beta=0$, since both sides of the equation give value 1. The reason can be easily explained and is omitted. We can also prove that DL_s gives an upper bound for the real case (*i.e.*, the difference solution). This can be easily achieved by applying Theorem 1 to compare Eqs. (11) and (13).

THEOREM 2 *$DL_d < DL_s$ for $M \geq x > 0$, and $\beta > 0$.*

Proof Representing the escape probabilities of both differential analysis and discrete analysis by $b=\prod_{t=1}^{t=x}(1-\beta/(M-t+1))$ and $a=((M-x+1)/(M+1))^{\beta}$, we have $DL_s=a(1-Y)/(Y+a(1-Y))$ and $DL_d=b(1-Y)/(Y+b(1-Y))$. It can be easily verified that $a(1-Y)/(Y+a(1-Y)) > b(1-Y)/(Y+b(1-Y))$ by manipulating the equation based on the fact of $a>b$ (Theorem 1).

The determination of DL depends on two factors: yield and testability. We have found that the deviation between DL_s and DL_d is dramatically shrunk, if the yield is very high. This can be easily verified by comparing the factors of DL_d and DL_s. Our previous work shows that the DL derived using the random pattern assumption (*i.e.*, test patterns can be repeated) also provides an upper bound for the DL of pseudorandom testing [8]. Using sequential statistical analysis, the DL of random testing has been determined as

$$DL_r=\frac{(1-\beta/M)^x(1-Y)/Y}{1+(1-\beta/M)^x(1-Y)/Y} \tag{15}$$

where DL_r denotes the DL of random testing [8]. Computer simulation reveals that the value of DL_r is a good approximation to that of DL_d, only if either the yield or circuit detectability is high. Theoretically, the value of DL_s should be very close to that of DL_d as long as the number of pseudorandom test patterns applied is large (and this is the usual case in BIST applications). When compared with DL_r, DL_s tends to be a better approximation to DL_d which is the actual DL value of pseudorandom testing. It is interesting to compare the values of DL_d, DL_s and DL_r using different parameters. In order to control the numerical errors induced by DL_d as small as possible, the values of M and x should not be too large; however, M and x cannot be too small either. The reason is to guarantee the "continuity" property which has been utilized to analyze DL_s. A reasonable compromise is to have $M=1000$. The yield value, Y, is set to 0.5 to prevent the effects of Y from being amplified or shrunk.

Tables IIa–IIe give the values of DL_d, DL_s, and DL_r under different β and x values. It is worth noting that the deviations among DL_d, DL_s, and DL_r should be much smaller than those shown in Tables IIa–IIe, as the number of pseudorandom test patterns applied is on the order of millions. We have observed the superiority of using DL_s as an approximation to DL_d, when β is relatively much smaller than M (the real case). Deflections of DL_r from DL_d for small β can be very significant, sometimes several order-of-magnitudes larger than that of DL_s from DL_d, as the value of x increases

TABLE IIa Values of DL_d, DL_s, and DL_r for different β and x values

β	x	DL_d	DL_s	DL_r
10	50	3.739479e−01	3.746294e−01	3.769494e−01
10	100	2.575697e−01	2.587462e−01	2.679529e−01
10	150	1.633944e−01	1.647329e−01	1.813021e−01
10	200	9.597526e−02	9.718175e−02	1.181500e−01
10	250	5.255381e−02	5.347965e−02	7.498069e−02
10	300	2.695701e−02	2.758612e−02	4.674831e−02
10	350	1.296750e−02	1.335458e−02	2.881509e−02
10	400	5.832198e−03	6.050182e−03	1.763401e−02
10	450	2.434636e−03	2.547226e−03	1.074352e−02
10	500	9.323178e−04	9.853904e−04	6.527594e−03
10	550	3.219974e−04	3.445680e−04	3.959442e−03
10	600	9.792943e−05	1.064282e−04	2.399239e−03
10	650	2.534690e−05	2.810077e−05	1.452931e−03
10	700	5.308512e−06	6.043960e−06	8.795369e−04
10	750	8.314244e−07	9.826435e−07	5.323101e−04

TABLE IIb

β	x	DL_d	DL_s	DL_r
50	50	6.714416e−02	7.162206e−02	7.144745e−02
50	100	4.455848e−03	5.155737e−03	5.885683e−03
50	150	2.362899e−04	2.982940e−04	4.553475e−04
50	200	1.038335e−05	1.445159e−05	3.505144e−05
50	250	3.703278e−07	5.758279e−07	2.697119e−06
50	300	1.040695e−08	1.837372e−08	2.075303e−07
50	350	2.221246e−10	4.543030e−10	1.596842e−08
50	400	3.439130e−12	8.356409e−12	1.228689e−09
50	450	3.642969e−14	1.086116e−13	9.454148e−11
50	500	2.446416e−16	9.336464e−16	7.274492e−12
50	550	9.407833e−19	4.865452e−18	5.597356e−13
50	600	1.800747e−21	1.366202e−20	4.306884e−14
50	650	1.403408e−24	1.752475e−23	3.313931e−15
50	700	3.290254e−28	8.065307e−27	2.549903e−16
50	750	1.424658e−32	9.161829e−31	1.962022e−17

TABLE IIc

β	x	DL_d	DL_s	DL_r
100	50	4.455848e−03	5.916526e−03	5.127350e−03
100	100	1.469662e−05	2.685713e−05	2.656069e−05
100	150	3.409544e−08	8.903243e−08	1.368915e−07
100	200	5.342381e−11	2.088545e−10	7.055079e−10
100	250	5.354464e−14	3.315782e−13	3.636029e−12
100	300	3.211636e−17	3.375935e−16	1.873928e−14
100	350	1.061333e−20	2.063912e−19	9.657802e−17
100	400	1.740646e−24	6.982958e−23	4.977414e−19
100	450	1.238204e−28	1.179647e−26	2.565247e−21
100	500	3.197616e−33	8.716955e−31	1.322071e−23
100	550	2.353687e−38	2.367263e−35	6.813656e−26
100	600	3.503246e−44	1.866502e−40	3.511605e−28
100	650	0.000000e+00	0.000000e+00	1.809802e−30
100	700	0.000000e+00	0.000000e+00	9.327314e−33
100	750	0.000000e+00	0.000000e+00	4.807088e−35

TABLE IId

β	x	DL_d	DL_s	DL_r
200	50	1.038335e−05	3.542195e−05	1.427227e−05
200	100	5.342381e−11	7.213445e−10	2.037036e−10
200	150	1.242191e−16	7.926775e−15	2.907355e−15
200	200	1.167447e−22	4.362021e−20	4.149516e−20
200	250	3.866729e−29	1.099441e−25	5.922387e−25
200	300	3.803757e−36	1.139694e−31	8.452712e−30
200	350	8.968310e−44	4.259732e−38	1.206411e−34
200	400	0.000000e+00	4.203895e−45	1.721848e−39
200	450	0.000000e+00	0.000000e+00	2.522337e−44
200	500	0.000000e+00	0.000000e+00	0.000000e+00

TABLE IIe

β	x	DL_d	DL_s	DL_r
400	50	3.439130e−12	1.254804e−09	8.082813e−12
400	100	1.740646e−24	5.203378e−19	6.533186e−23
400	150	9.514172e−38	6.283376e−29	5.280652e−34
400	200	0.000000e+00	1.902722e−39	4.203895e−45
400	250	0.000000e+00	0.000000e+00	0.000000e+00

(Tabs. IIa, IIb). We have also found that DL_s loses its superiority when β is relatively large, say about 20% of M in the above example as shown in Tables IId, IIe; though this situation will not occur in real circuits. The reason can be easily explained by investigating into Eq. (15) where each pseudorandom test application dramatically reduces the escape probability for large β. Thus, each of DL_s and DL_r has its own limitation and a natural consequence is to provide a good approximation for DL_d by taking advantages of both DL_s and DL_r. Finally, the DL of pseudorandom testing can be determined as

$$DL_{pr}=\frac{\text{Min}\{((M-x+1)/(M+1))^{\beta},((M-\beta)/M)^{x}\}(1-Y)}{Y+\text{Min}\{((M-x+1)/(M+1))^{\beta},((M-\beta)/M)^{x}\}(1-Y)} \tag{16}$$

where $\text{Min}(a, b)$ denotes the minimal value of a and b, and DL_{pr} gives the DL value of pseudorandom

testing by incorporating both DL_s and DL_r into consideration. In summary, Eq. (16) provides a very good upper bound regardless of the β values. In most cases, the value of β is very small when compared with M (generally, β/M is smaller than 10^{-5}). Thus, DL_s gives very accurate analysis as shown in Table III where M is assigned 1,000,000. We emphasize again that it is more appropriate to use DL_s rather than DL_d for very long pseudorandom test sequence as given in Table III, since DL_d is not accurate enough due to the large amount of numerical errors accumulated.

The other advantage of using DL_s over DL_d is the easiness of deriving the required pseudorandom test length for a specified DL value. Rearranging Eq. (11), the relationships between the required pseudorandom test length (x_s) and other parameters such as DL, the fabrication yield, the worst fault detectability, and M can be given as

$$x_s = \{(M+1)\left\{1 - \left[\frac{(1-DL)(1-Y)}{DL \cdot Y}\right]^{\beta}\right\} \quad (17)$$

The same derivation is not possible for DL_d which does not have a closed-form representation.

TABLE III Values of DL_d, DL_s, and DL_r for large pseudorandom test length

β	x	DL_d	DL_s	DL_r
10	50000	3.745057e−01	3.745064e−01	3.775401e−01
10	100000	2.585325e−01	2.585336e−01	2.689404e−01
10	150000	1.644894e−01	1.644907e−01	1.824244e−01
10	200000	9.696189e−02	9.696309e−02	1.192019e−01
10	250000	5.331061e−02	5.331153e−02	7.585730e−02
10	300000	2.747101e−02	2.747164e−02	4.742520e−02
10	350000	1.328359e−02	1.328398e−02	2.931173e−02
10	400000	6.010097e−03	6.010315e−03	1.798586e−02
10	450000	2.526459e−03	2.526573e−03	1.098670e−02
10	500000	9.755659e−04	9.756195e−04	6.692685e−03
10	550000	3.403717e−04	3.403945e−04	4.070026e−03
10	600000	1.048395e−04	1.048482e−04	2.472549e−03
10	650000	2.758241e−05	2.758523e−05	1.501134e−03
10	700000	5.904245e−06	5.905003e−06	9.110193e−04
10	750000	9.535447e−07	9.537021e−07	5.527579e−04
10	800000	1.023816e−07	1.024041e−07	3.353367e−04
10	850000	5.765034e−09	5.766831e−09	2.034183e−04
10	900000	9.995951e−11	1.000090e−10	1.233890e−04
10	950000	9.757278e−14	9.767480e−14	7.484268e−05

Similarly, the required random test length, x_r, for a given DL can be presented as shown below by manipulating Eq. (15).

$$x_r = \frac{\ln(\theta/(1-\theta) \cdot Y/(1-Y))}{\ln(1-\beta/M)} \quad (18)$$

Finally, the minimal pseudorandom test length required to satisfy the specified DL can be determined by equation

$$x_{pr} = \text{Min}\{x_s, x_r\} \quad (19)$$

The above equation is especially useful in pseudorandom test length estimation.

An important factor of maintaining a good DL analysis is to accurately determine the fault detection probability or detectability. Exact value of the detection probability for each fault can be derived using signal probability computation [23], if the CUT size is small. For large circuits, detection probability can be approximated using testability analysis [24–26]. By computer simulation or circuit structure analysis, controllability (the degree to which the test vectors exercise circuit nodes) and the observability (the likehood of faults propagating to the output) of each line in the CUT can be estimated. Detection probability of a stuck-at-v fault occurring at line l can then be determined by multiplying the $\bar{v}$ controllability to the observability of l. Recently, a BDD-based algorithm for computation of *exact* fault detection probabilities has been proposed [27] and the algorithm is able to deal with most ISCAS85 benchmark combinational circuits [28], as the simulation results demonstrate. The worst fault detection probability, σ, is the minimum value of all detection probabilities. The worst detectability, β, can be approximated using the product of σ and the total number of input pattern combinations (2^n, for an n-input circuit) of the CUT. Yield estimation also plays an important role in the DL analysis. Mostly, a rather accurate yield value can be determined by analyzing the defect statistics and test data [29].

4. K-FAULT ANALYSIS OF PSEUDORANDOM TESTING

Generally, the quality of random testing is considered based on the concept of *test confidence* [2], and a random test length is determined to achieve the test confidence measured by the probability that the applied random patterns detect *every* single stuck-at fault [10] or the worst stuck-at fault [30]. The confidences thus determined are called *testing quality* and *detection quality*, respectively [2]. Mostly, the random test sequence provided by the embedded BIST device is pseudorandom, and the *same* set of test patterns is generated and expected to detect all possible single stuck-at faults occurring on each CUT. Thus, the test confidence measured by testing quality is more convincing than that given using detection quality.

Random or pseudorandom DL analysis has been considered by combining both the fabrication quality (in terms of yield) and test confidence (in terms of detection quality), and gives a more complete estimation on the shipping quality of chips than test confidence can provide. Most pseudorandom DL discussions are based on single stuck-at fault model in terms of the worst detection probability to estimate the test confidence. Unfortunately, this is inadequate when very high test quality is demanded. In this section, the test confidence of pseudorandom DL analysis is extended to consider the testing quality, instead of the detection quality only. That is, the value of $P(T_x=0|w_1)$ will be estimated by considering all single stuck-at faults, instead of the worst single stuck-at fault only.

By definition, the *test set* of a fault is the set of all input vectors which detect the fault. Two faults f_1 and f_2 are *disjoint* if their corresponding test sets have no test vectors in common. The detectability of single stuck-at fault f is the number of test patterns detecting f. Similarly, two faults are *conjoint* if their corresponding test sets share at least one test vector. Our previous work indicates that:

(1) The pseudorandom test length required for a fault set with a disjoint test set is no less than that for a fault set with a conjoint test set, to achieve the same test confidence [31].
(2) Each fault whose detectability is not smaller than twice that of the worst detectability can be ignored from the test confidence consideration [31].

The above observations are consistent with the results of random test consideration [10]. Based on these two observations, the analysis of DL – in terms of testing quality – for pseudorandom testing can be greatly simplified.

Consider a disjoint fault set whose members are faults $f_1, \ldots, f_m$; and $k(k \leq m)$ faults have the worst detectability (or less than twice the worst detectability). To further simplify the analysis, each fault in the fault set is assumed to have detectability equal to the worst detectability, β. Figure 3 shows the $(k+1)$ states of the Markov chain which describes the detection process for the k worst faults. In state S_0 none of the faults have been detected, and S_i relates to the detection of i faults. Thus, state S_k is an absorbing state in which all faults have been detected. Transition probabilities among the states are labeled along the corresponding edges of the graph shown in Figure 3. It can be observed that transition probabilities keep changing when test patterns are applied. The following set of differential equations describes the relationship among state transitions in the Markov

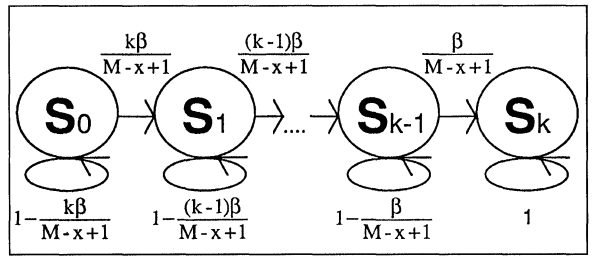

FIGURE 3 The Markov model for pseudorandom testing by considering all single stuck-at faults.

chain:

$$\begin{aligned}
\frac{dS_0(t)}{dt} &= -\frac{k\beta}{M-t+1}S_0(t) \\
&\vdots \\
\frac{dS_i(t)}{dt} &= \frac{(k-i+1)\beta}{M-t+1}S_{i-1}(t) - \frac{(k-i)\beta}{M-t+1}S_i(t); \qquad (20) \\
&\vdots \\
\frac{dS_k(t)}{dt} &= \frac{\beta}{M-t+1}S_{k-1}(t)
\end{aligned}$$

with the initial condition: $S_0(0)=1$, and $S_1(0)=\cdots=S_i(0)\cdots=S_k(0)=0$.

By solving the above differential equations, the state probability of S_k after x pseudorandom test patterns have been applied can be determined as $S_k(x)=[1-(1-x/(M+1))^{\beta}]^k$. Details of the derivation process for the above differential equations can be found in [31]. The value of $S_k(x)$ gives a lower bound for the detection probability by considering all single stuck-at faults. We emphasize that β is the number of different test patterns which detect the worst single stuck-at fault. The escape probability, $P(T_x=0|w_1)$, can easily be given as $P(T_x=0|w_1)=1-S_k(x)$. Finally, the DL of pseudorandom testing, in terms of testing quality, can be represented by the following equation

$$DL_k = \frac{\{1-[1-(1-x/(M+1))^{\beta}]^k\}(1-Y)}{Y+\{1-[1-(1-x/(M+1))^{\beta}]^k\}(1-Y)} \qquad (21)$$

where DL_k denotes the DL value determined by considering all single stuck-at faults (in fact, k faults after a series of simplifications). It is interesting to find that the above equation degenerates to the DL_s equation of the worst fault case Eq. (11), if k is set to 1. Figure 4 ($M=1{,}000$) and Table IV ($M=1{,}000{,}000$) also show the relationships between DL_k and x for several different k values, with the unbiased yield value. The deviation between the DL_k values derived by considering the worst single stuck-at fault ($k=1$) and all single stuck-at faults ($k>1$) is very significant. However, using the above Equation to estimate the DL of pseudorandom testing is very dangerous, since the measurement is too pessimistic. In fact, Eq. (21) is derived by assuming that only the k worst faults may occur. In real circuits, the number of faults whose detectabilities are equal the worst detectability or smaller than twice of the worst detectability is very limited. As matter of fact, most typical circuits have only a few of hard-to-detect faults. Thus, the escape probability of the k worst faults must be weighted by their occurring probability, P_k; and the above equation

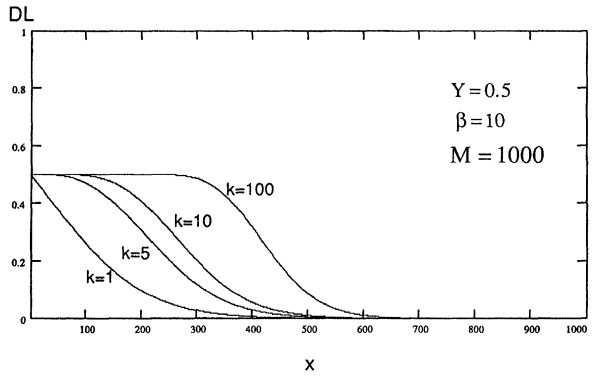

FIGURE 4 DL of pseudorandom testing for different k values.

TABLE IV DL of pseudorandom testing under different k values

β	x	$k=1$	$k=5$	$k=10$
10	50000	3.745064e−01	4.973857e−01	4.999729e−01
10	100000	2.585336e−01	4.688725e−01	4.965415e−01
10	150000	1.644907e−01	3.997128e−01	4.704390e−01
10	200000	9.696309e−02	3.023136e−01	4.043581e−01
10	250000	5.331153e−02	2.010178e−01	3.055005e−01
10	300000	2.747164e−02	1.177621e−01	1.994525e−01
10	350000	1.328398e−02	6.149625e−02	1.124980e−01
10	400000	6.010315e−03	2.900354e−02	5.557697e−02
10	450000	2.526573e−03	1.244406e−02	2.443112e−02
10	500000	9.756195e−04	4.849699e−03	9.629293e−03
10	550000	3.403945e−04	1.698503e−03	3.388372e−03
10	600000	1.048482e−04	5.239113e−04	1.047000e−03
10	650000	2.758523e−05	1.379033e−04	2.757496e−04
10	700000	5.905003e−06	2.952397e−05	5.904532e−05
10	750000	9.537021e−07	4.768483e−06	9.536898e−06
10	800000	1.024041e−07	5.120201e−07	1.024039e−06
10	850000	5.766831e−09	2.883415e−08	5.766830e−08
10	900000	1.000090e−10	5.000450e−10	1.000090e−09
10	950000	9.769963e−14	4.884981e−13	9.769963e−13

can be refined to

$$DL_k = \frac{\{1 - [1 - (1 - x/(M+1))^{\beta}]^k\}(1 - Y)P_k}{Y + \{1 - [1 - (1 - x/(M+1))^{\beta}]^k\}(1 - Y)P_k} \tag{22}$$

Faults whose detectabilities are not smaller than twice of the worst detectability are not involved in the above DL analysis, since their detection can be ignored from the test confidence consideration as discussed before [10, 31]. Rearranging the above equation, the relationships between the required pseudorandom test length and other parameters such as DL, fabrication yield, k, β, and M can be represented as

$$x = (M+1)\left[1 - \left\{1 - \left[1 - \frac{DL \cdot Y}{(1 - DL)(1 - Y)P_k}\right]^{-k}\right\}^{-\beta}\right] \tag{23}$$

This equation clearly gives the required pseudorandom test length for a specified DL value. The β and k values used in the above equations can be obtained from the detectability profile generated using the exact detectability analysis [27] or testability approximation [24–26] as discussed in the previous section. Equations (22) and (23) can be further refined by taking random testing into consideration as Eqs. (16) and (19). For example, replacing the term $(1-x/(M+1))^{\beta}$ of Eq. (22) by $\text{Min}\{((M-x+1)/(M+1))^{\beta}, ((M-\beta)/M)^{x}\}$, Eq. (22) can provide a more accurate DL estimation for the k-fault considerations. When the values of k, and P_k are inevitably large, they can be reduced using many design-for-testability techniques [2] if the hardware overhead can be justified by the test cost reduction.

5. DISCUSSION

DL analysis is a very important problem of digital circuit testing; unfortunately, the analysis is extremely difficult since DL is related to testing and manufacturing variations. The factors affecting DL analysis at least include fault occurrence, fault distribution, fault modeling, and fault coverage distribution. To simplify the analysis, most researches are performed based on the assumptions of: (1) single stuck-at fault model, (2) equally likely fault occurrence, (3) uniform fault distribution, and (4) uniform fault coverage distribution. Based on these assumptions, numerous models have been proposed to estimate the DL of circuit fabrication and testing. Recently, there have been more and more criticisms concerning these assumptions.

It has been an agreement that the single stuck-at fault model is not adequate in representing VLSI defects. In fact, the majority of VLSI defects can not be modeled by single stuck-at faults. The effectiveness of using the stuck-at fault coverage as a predictor of the defect level has been studied by simulating bridging faults on benchmark circuits [32]. Results demonstrate that the predicted DL may differ from the real defect level by as much as an order of magnitude, as the desired DL decreases. Another analysis also concludes that unmodeled faults have significant impacts on defect coverage, and more than 100% single stuck-at fault coverage is required if the DL is intended to be controlled very small [33]. Experimental data announced from HP indicates that using single stuck-at fault coverage as an estimator predicts a much lower (than the actual) DL, when fault coverage exceeds 90% [34]. Although most reports draw unfavorable conclusions to the single stuck-at model, there might be good agreement between the model and actual fabrication data under the right set of conditions [35]. For example, it is possible to achieve a good agreement between the actual and predicted DL, if the stuck-at fault coverage is obtained using functional test patterns [34]. Our DL analysis method has been established based on the single stuck-at fault model, as far as the detectability is concerned. It is interesting to verify the availability of the work, since pseudorandom test patterns have closer relationships to

functional test patterns (than to deterministic test patterns). The long test sequence, which achieves high single stuck-at fault coverage, generally has a very high possibility of detecting other unmodeled faults.

Most DL analysis methods use the assumption of uniform defect distribution, *i.e.*, the presence of any particular defect is independent of the presence of other faults. However, defects on a wafer are not uniformly distributed, and tend to exhibit clustering. The spatial defect clustering information can be employed to optimize wafer-level test costs [36]. It also has been found that a faulty chip generally has more than one defects [33]. Multiple faults, which might contain different fault types, occurring on the same chip sometimes result in fault masking behavior [2]. Multiple fault detection has been identified as a very difficult problem in the VLSI testing area, and its influence on DL deserves more attention. The probability of multiple stuck-at fault detection using single stuck-at test set depends on the circuit structure, instead of the circuit size. For example, there exists a complete test set for single stuck-at faults that detects all multiple stuck-at faults, if the CUT is fanout-free [37, 38]. Though all single stuck-at faults have been considered in this work, the detection of multiple faults and non-uniformly distributed faults on a single chip needs to be further researched. The effect of multiple stuck-at faults under random testing environment has been analyzed in [39].

It is natural that defects generally occur with different probabilities, since critical areas on a chip is more apt to cause defects. To simplify the discussion, a Poisson's model has been assumed for the defect distribution over the chip [40]. The well-known William and Brown defect model [11] has been extended to a more general case by removing the hypothesis of equally likely fault and exploiting the concept of critical area to evaluate the fault occurrence probabilities over the chip [40]. In this work, the worst detectability has been used to estimate the DL for pseudorandom testing. DL estimation using the worst case hypothesis might be pessimistic, since the hypothesis implicitly assumes that all fault occurrences are the worst faults. The results have been extended to consider all single stuck-at faults, and the DL analysis of non-equally likely faults has been considered by weighting different fault occurrence probabilities to the corresponding fault detectabilities. Recent work has indicated that equiprobability hypothesis and other non-equiprobability distributions result in very low difference in random test length estimation, when the fault coverage is high [41]. This might alleviate the difficulty of finding a fault occurrence distribution by assuming that all faults may occur equally likely.

Recent work has reported that non-uniform distribution of detected faults has strong impacts on test quality [42]. It has been concluded that fault coverage requirements are significantly higher, if the undetected faults are clustered rather than being uniformly distributed. Thus, the conventional fault coverage – which is based on the randomly distributed coverage assumption – gives a lower bound on acceptable fault coverage to achieve the expected DL. Since our DL analysis is based on the weighted worst faults, the impact of non-uniform detected fault distribution is less serious. In summary, there are too many factors affecting the accuracies of the DL analysis regardless of the testing techniques employed. Most proposed DL analysis methods have inherent deficiencies, and more researches are required.

6. CONCLUSIONS

In this paper, the DL analysis of pseudorandom testing has been achieved using a stochastic model. This is the first time to derive a closed form which clearly gives the relationships among DL, detectability, yield, the number of all input combinations, and the applied test length, under pseudorandom testing environments. Results obtained based on the single stuck-at fault model and worst case analysis demonstrate that the DL estimated using continuous stochastic analysis

gives a very good approximation to the actual DL value, provided the number of pseudorandom test patterns applied is large. Generally, the pseudorandom test set is very long (at least on the order of several millions), and this makes the proposed solution well fit to many practical applications. The analysis is then extended to consider all single stuck-at faults. A closed form has also been derived to take the number (k) of hard-to-detect faults into account. However, we must emphasize that the k-fault analysis results in a too pessimistic solution and has been relaxed by weighting fault occurring probabilities into the k-fault escape probability. The results obtained are mainly based on the single stuck-at fault model. However, they can be extended to other fault types such as bridging faults, as long as the corresponding detectabilities can be derived [43].

Recently, there have been many reports questioning the assumptions employed in the process of DL analysis. However, the analysis is almost impossible if these assumptions are removed. It appears to us that solutions proposed based on the stringent assumptions still can be used, however, the results must be interpreted with care. Especially, the DL values under very high fault coverage are critical. Fortunately, pseudorandom testing might be immune to this critical region since the long test sequence generally detects many unmodeled, or non-uniformly distributed faults.

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