Optimization of FIBMOS Through 2D Silvaco ATLAS and 2D Monte Carlo Particle-based Device Simulations

J. KANG, X. HE, D. VASILESKA* and D. K. SCHRODER

*Department of Electrical Engineering and Center for Solid State Electronics Research,
Arizona State University, Tempe, AZ 85287-5706, USA*

Focused Ion Beam MOSFETs (FIBMOS) demonstrate large enhancements in core device performance areas such as output resistance, hot electron reliability and voltage stability upon channel length or drain voltage variation. In this work, we describe an optimization technique for FIBMOS threshold voltage characterization using the 2D Silvaco ATLAS simulator. Both ATLAS and 2D Monte Carlo particle-based simulations were used to show that FIBMOS devices exhibit enhanced current drive capabilities when compared to normal MOSFETs. It was also found that the device performance is very much dependent upon the FIB implant profile. High and narrow doping of the FIB implant leads to high drain current and low hot carrier reliability, whereas low and wide doping gives rise to lower drain current and higher hot carrier reliability.

Keywords: Device scaling; FIBMOS devices; Threshold voltage characterization; Channel engineering; Hot carrier reliability

INTRODUCTION

Focused Ion Beam (FIB) implantation has recently been proposed for channel engineering in high-performance MOSFET fabrication. Shen and his co-workers [1] fabricated FIBMOS devices with a special narrow doping region implanted with FIB on the source side of the channel. They showed that this novel device structure, schematically shown in Figure 1, exhibits higher output resistance, reduced hot electron degradation, more stable threshold voltage (V_T) upon device scaling,

and higher operation frequency. However, the rather asymmetric doping profile in this device prevents one from using the classical expressions for the threshold voltage since it is a rather complex function of the step doping width and density. In this work, we first describe the optimization technique that Kang *et al.* [2] developed for FIBMOS threshold voltage characterization, based on 2D device simulations and 3D V_T contour mapping. It enables one to design FIBMOS devices with a certain V_T and best performance in consideration of the drain current,

*Corresponding author. Tel.: +1 480 965-6651, Fax: +1 480 965 8058, e-mail: vasilesk@imap2.asu.edu

FIGURE 1 Schematic description of the structure and doping profile of a one-step FIBMOS device with gate length $0.25\ \mu\text{m}$ and oxide thickness of $5\ \text{nm}$.

hot-electron degradation, V_T stability and maximum operation frequency.

Using both 2D Silvaco ATLAS energy balance model and 2D Monte Carlo particle-based simulations, we also examine hot-electron reliability of FIBMOS devices. This is a severe problem in normal deep-submicrometer MOSFETs in which the high substrate doping, used to prevent the punch-through effect, leads to large electric fields and enhanced impact ionization. For n -channel MOSFETs, the electrons generated *via* the impact ionization process tend to be injected into the gate oxide (leading to a threshold voltage shift and degradation of the channel mobility) or are injected into the drain. The generated holes are swept into the substrate, thus giving rise to substrate leakage current and enhanced impact ionization due to the forward biasing of the source/substrate junction. Both the 2D Silvaco ATLAS and the 2D Monte Carlo particle-based simulator show that the built-in electric fields at the source side of the channel, due to the presence of the FIB implant, lead to enhanced current-drive capabilities of the FIBMOS device when compared to normal

MOSFETs. Our 2D Monte Carlo particle-based simulations also show that (due to the relatively low electric field at the drain end of the channel) the average electron energy in FIBMOS devices is low which, in turn, significantly reduces the probability for impact ionization to occur.

THRESHOLD VOLTAGE CHARACTERIZATION

As already discussed in the introduction, FIBMOS devices have an asymmetric channel doping profile which influences the device performance. For example, the threshold voltage is not only a function of the step doping density, but it is also a function of the step doping width. To understand the relationship between the doping profile of the FIBMOS device and the threshold voltage, we simulated a large number of FIBMOS devices with various implant step widths and doping densities. The Silvaco device simulator ATLAS was used for this purpose [2]. The extracted threshold voltages were then mapped on a plane of step width and step doping density. In other words, three-dimensional contour plots for the threshold voltage were generated with the step width and the step doping density on the horizontal and vertical axis, respectively. The extracted threshold voltages were then rearranged for contour plots. A sample contour plot for $0.25\ \mu\text{m}$ gate-length FIBMOS devices is shown in Figure 2. From these contour plots, it is possible to find the combinations of step doping width and doping density that give the desired threshold voltage. In Table I, we list four different combinations of parameters that lead to the best device performance. One should note that the four combinations of doping parameters do not result in identical device performance, even though the threshold voltage is the same. The drain current is reduced as one goes from high and narrow to low and wide doping profile. These are important features of FIBMOS. Therefore, if one needs high output current and device reliability is less important, high and narrow doping is best.

FIGURE 2 Contour plots for one-step FIBMOS with channel length of $0.25\ \mu\text{m}$. The numbers on the contour lines represent threshold voltages.

TABLE I Parameters for step doping giving a threshold voltage of $0.69\ \text{V}$. The channel length of the FIBMOS device equals $0.25\ \mu\text{m}$.

Step doping width (nm)	60	80	100	120
Step doping density ($\times 10^{18}\ \text{cm}^{-3}$)	1.95	1.61	1.43	1.32
$I_D(\text{A}/\mu\text{m})$ at $V_G = 1.8\ \text{V}$	94.81	93.18	90.76	88.15

For high reliability, low and wide doping has to be used.

DEVICE TRANSFER AND OUTPUT CHARACTERISTICS

To examine the enhancement in the current drive capabilities of FIBMOS devices with respect to normal MOSFETs, we developed a 2D Monte Carlo particle-based simulator. The Monte Carlo model, used in the transport portion of the simulator, is based on the usual Si band-structure for three-dimensional electrons in a set of non-parabolic Δ -valleys with energy-dependent effective masses. The six conduction band valleys are included through three pairs: valley pair 1 pointing in the (100) direction, valley pair 2 in the (010) direction, and valley pair 3 in the (001) direction. The explicit inclusion of the longitudinal and

transverse masses is important and this is done in the program using the Herring-Vogt transformation [3]. Intravalley scattering is limited to acoustic phonons. For the intervalley scattering, we include both g - and f -phonon processes. It is important to note that, by group symmetry considerations, the zeroth-order low-energy f - and g -phonon processes are forbidden. Nevertheless, three zeroth-order f -phonons and three zeroth-order g -phonons with various energies are usually assumed [4]. We have taken into account this selection rule and have considered two high-energy f - and g -phonons and two low-energy f - and g -phonons. The high-energy phonon scattering processes are included *via* the usual zeroth-order interaction term, and the two low-energy phonons are treated *via* a first-order process [5]. The first-order process is not really important for low-energy electrons but gives a significant contribution for high-energy electrons. The low-energy phonons are important in achieving a smooth velocity saturation curve, especially at low temperatures. The phonon energies and coupling constants in our model are determined so that the experimental temperature-dependent mobility and velocity-field characteristics are consistently recovered [6]. At present, impact ionization, surface-roughness and Coulomb scattering are not included in the model. However, these simplifications do not prevent us from examining the overall performance enhancement of FIBMOS devices with respect to normal MOSFETs.

The gate length of both the regular MOSFET and the FIBMOS device being investigated equals $0.25\ \mu\text{m}$. The source and drain extension is $50\ \text{nm}$, and the junction depth is $36\ \text{nm}$. The standard device has a substrate doping density of $10^{18}\ \text{cm}^{-3}$. The doping density of the source and drain regions of this device is $10^{19}\ \text{cm}^{-3}$. The substrate doping of the FIBMOS device equals $10^{16}\ \text{cm}^{-3}$, the length of the one-step FIB region is $70\ \text{nm}$, the depth of the FIB region is $36\ \text{nm}$, and the doping of this region is $1.4 \times 10^{18}\ \text{cm}^{-3}$. The source and drain doping of the FIBMOS device is identical to the one used for the standard device.

The conduction band edge, for applied bias $V_G = 1$ V and $V_D = 0.8$ V, is shown in the top panel of Figure 3. One can clearly see the presence of a potential barrier near the source end of the channel, as a result of the high doping of the FIB region. Also note that the width of the barrier region is less than 40 nm, which suggests that source to drain tunneling might take place in this device structure, thus leading to enhanced off-state leakage currents. The x -component of the electric field (electric field component along the channel) is shown on the bottom panel of Figure 3. The presence of a built-in electric field near the source

FIGURE 3 Top panel: Conduction band edge variation for the FIBMOS device, for $V_G = 1$ V and $V_D = 0.8$ V. Bottom panel: The x -component of the electric field for the same bias conditions.

end of the channel can significantly accelerate those electrons that make it over the potential barrier. Similar electric field conditions exist in bipolar junction transistors with graded base regions.

The average electron drift velocity and the average electron kinetic energy along the channel of the FIBMOS device, for the bias conditions from Figure 3, are shown in Figure 4(a) and 4(b), respectively. Note that both the average drift velocity and the average electron energies are low in the front end of the FIB region. Because of the built-in field in the FIBMOS device, once electrons surmount the potential barrier at the source end of the channel, their energy and velocity increase rapidly. Phonon scattering and the presence of relatively low electric fields at the middle

FIGURE 4 (a) Average drift velocity and (b) average energy of the carriers along the channel of the FIBMOS device. In both cases, the applied bias equals $V_G = 1$ V and $V_D = 0.8$ V.

and drain end of the channel lead to a reduction in both the average drift velocity and the average electron energy, thus eliminating the problem of substrate leakage currents due to impact ionization. The characteristics of the regular device are quite different. The drift velocity is relatively low near the source end of the channel which, as shown later, leads to a factor of four smaller drain current when compared to the drain current of the FIBMOS device. On the other hand, the average electron energy peaks at the drain end of the channel and is about a factor of four higher than the average electron energy in the FIBMOS device. This gives rise to hot-carrier degradation in regular MOSFETs, and can be reduced by the introduction of the lightly doped drain (LDD) regions.

The transfer and the output characteristics of the FIBMOS device and the regular MOSFET, obtained with the 2D particle-based simulator, are shown in Figures 5(a) and 5(b), respectively. Also shown in Figure 5(b) are the output characteristics of both the regular and the FIBMOS device obtained with the Silvaco ATLAS simulator [2]. Assuming that the threshold voltage equals the gate voltage for which the drain current is $1\mu\text{A}/\mu\text{m}$, we find that threshold voltage of the regular MOSFET is $V_T = 0.68\text{ V}$, in close agreement to the Silvaco ATLAS predictions. For the FIBMOS device, the threshold voltage equals $V_T = 0.61\text{ V}$. This slightly lower value of V_T is due to the fact that we use $1.4 \times 10^{18}\text{ cm}^{-3}$ instead of $1.8 \times 10^{18}\text{ cm}^{-3}$ doping of the FIB region, and leads to slight overestimation of the performance of the FIBMOS device. Both the Silvaco ATLAS and the 2D Monte Carlo particle-based simulations suggest that the FIBMOS device being investigated exhibits significantly higher drain current when compared with the normal MOSFET performance. For example, for a gate voltage $V_G = 1.0\text{ V}$, the current of the FIBMOS device is more than a factor of four larger than the drain current of the normal MOSFET. Note also that in the Monte Carlo particle-based simulations we use 10^{19} cm^{-3} doping for the source and drain regions, which leads to about 30% current degradation due

FIGURE 5 (a) Transfer characteristics for $V_D = 0.2\text{ V}$. (b) Output characteristics for gate bias $V_G = 1\text{ V}$.

to series resistance effect [7]. This, in a way compensates for the fact that Coulomb and surface-roughness scattering are not being considered in the present model. The source and drain doping used in the Silvaco ATLAS simulations equals 10^{20} cm^{-3} , thus leading to significantly smaller source and drain series resistance.

CONCLUSIONS

We have proposed and used an optimization technique for threshold voltage extraction of a one-step FIBMOS device. Using 3D contour plots for a range of step doping width and doping density, we have determined the doping profiles that set the threshold voltage at the targeted value

for best device performance. We find that if the system requirements are high current drive or low-power operation, one needs to use narrow FIB implants with high doping. On the other hand, if the system requires long device lifetime, then wide and low-doping profiles for the FIB implant need to be used. Both the 2D Monte Carlo particle-based simulations and the Silvaco ATLAS simulations suggest performance enhancement of FIBMOS devices with respect to normal MOSFETs. An increase in the drain current of about a factor of four at the highest drain voltage was found for the FIBMOS device when compared to the regular MOSFET device. Similar trends have been observed in Ref. [8].

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