Non-Equilibrium Hole Transport in Deep Sub-Micron Well-Tempered Si p -MOSFETs

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As MOSFETs are scaled to deep submicron dimensions non-equilibrium, near ballistic, transport in p -MOSFETs becomes important. Recent experimental data indicates that as MOSFETs are scaled the performance gap between n and p -channel shrinks. Non-equilibrium transport effects and performance potentials of 'Well Tempered' Si p -MOSFETs with gate lengths of 50 and 25 nm are studied. Monte Carlo and calibrated Drift Diffusion simulations of these devices provide a quantitative estimate of the importance and the influence of non-equilibrium transport on submicron device performance. A possible explanation for the closing performance gap between n - and p -channel MOSFETs is offered.

Keywords: Silicon p -MOSFETs; Monte carlo; Non equilibrium transport; Hole transport; Deep sub-micron; Drift diffusion

1. INTRODUCTION

Si MOSFET technology represents by far the largest market share of the electronics industry (>95%). The current generation of MOSFETs have feature sizes of around 0.1 μm . The next generation of MOSFETs will have decanano dimensions, for example gate lengths of 90 nm by 2002 and 25 nm are predicted for 2014 [1]. To date, most simulation studies have concentrated on n -MOSFETs because of their intrinsically better performance as compared to p -channel devices and the simpler bandstructure for electrons. However, there is a growing interest in studying

p -MOSFETs due to the closing performance gap between n and p -channel devices, as defined in terms of transconductance, and the possibility of including a strained SiGe channel.

As the gate lengths of Si MOSFETs are shrunk to deep submicron dimensions, there is a significant difference in the behaviour of the intrinsic transconductance, g_m , between n and p -type MOSFETs: a steady increase in g_m is observed for p -MOSFETs whereas n -MOSFETs exhibit a saturation with corresponding gate length reduction [2]. It is speculated that the continuous improvement in p -MOSFET performance below 0.1 μm is related to the onset of velocity overshoot

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effects which are present at longer channel lengths in the n -channel devices.

The expected prevalence of non-equilibrium transport effects in sub $0.1\mu\text{m}$ device structures means that simulation techniques based on Drift Diffusion and Hydrodynamic models, are unlikely to be suitable for a detailed modelling of transport. Hence only an ‘exact’ solution to the Boltzmann Transport equation will supply reliable results and Monte Carlo (MC) is ideally suited for this purpose. By comparing MC simulations with a carefully calibrated Drift Diffusion model (DD) we are able to make a quantitative estimate of the importance of non-equilibrium transport on the device performance. Although previous Monte Carlo simulations of p -channel MOSFETs have been performed [3], (most notably the full-band simulations of the Breman group [4, 5]), they have concentrated on the effects of introducing either strained Si or SiGe into the standard p -MOSFET design. To date no MC studies have been carried out on deep sub-micron bulk Si *well-tempered* p -MOSFETs. The *well-tempered* p -channel MOSFETs studied here are mirror images, in terms of doping and the polysilicon gate, of the n -channel devices advanced in [6]. These devices, more fully discussed in Section 2, provide an excellent basis with which to compare future designs for SiGe and other advanced p -MOSFET architectures.

The rest of the paper is laid out as follows: Section 2 provides an outline of the *well-tempered* devices. Section 3 provides an outline of the Monte Carlo and Drift Diffusion models employed. Section 4 presents and discusses our simulation results. We finish with concluding remarks in Section 5.

2. DEVICE STRUCTURES

The *well-tempered* device structures considered here are similar to the Si n -MOSFETs presented by the Microsystems Technology Laboratory at the Massachusetts Institute of Technology [6]. Our devices are their p -type analogue mirror images in

FIGURE 1 Two-dimensional schematic cross section of the 50 nm ‘Well Tempered’ p -MOSFET being simulated.

terms of doping, *i.e.*, n -doping is replaced with p -doping and a p -polysilicon gate is used instead of an n -polysilicon gate in order to achieve the appropriate threshold voltage. The 25 and 50 nm MOSFETs described here make use of the proposed super-halo doping described by Taur *et al* [7]. A two-dimensional schematic cross section of a *well-tempered* p -MOSFET is shown in Figure 1.

3. MODELLING METHODS

3.1. Monte Carlo Method

The MC method is used to simulate the motion of charge carriers through a semiconductor device self-consistently with the electric field by following the progress of a representative number of ‘super-particles’, typically tens of thousands of which are considered, in order to solve the Boltzmann Transport Equation. These superparticles are propagated between scattering events by integrating the semi-classical equations of motion. The advantage of the MC method is that it allows for the inclusion of the full bandstructure (particularly important for holes) and associated scattering rates to be implemented in a natural and self-consistent framework.

The bandstructure model used in the simulations presented here is based on a six band $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian (3-valence bands+spin), after Kane [8, 9], with inclusion of spin-orbit coupling. The valence band parameters (L, M, N) used in the $\mathbf{k}\cdot\mathbf{p}$ model are chosen to give the best agreement with

non-local pseudopotential theory [10]. An example is shown in Figure 2, where a constant energy surface is presented for the heavy hole band. All the scattering mechanisms considered here; optical phonons, inelastic acoustic phonons and ionized impurity scattering (which implements statistical screening [11]), are calculated within the Born-Oppenheimer approximation [12]. Note that a continuous doping profile is assumed. Interface roughness scattering, using the semi-empirical model described by Sangiorgi *et al.* [13], is implemented. The scattering rates take into account the complicated valence bandstructure and Bloch overlap integrals using Wiley's approximation [14]. We note that some previous Monte Carlo simulations of devices have neglected the contribution of the overlap integrals [4, 5]. This is surprising since their importance for describing carrier transport in anisotropic bands has been understood for some time [15]. The acoustic and optical coupling constants are calibrated by comparing Monte Carlo results with the bulk steady-state experimental velocity-field measurements for *p-type* Si [16], as shown in Figure 3. The agreement with published experimental data is

FIGURE 2 The equi-energetic heavy $|3/2, 3/2\rangle$ hole surface in Si at 40 meV, (corresponding to a temperature of approximately 300 K), as calculated from $\mathbf{k} \cdot \mathbf{p}$. The anisotropy and warping can clearly be seen.

FIGURE 3 Steady state velocity-field characteristics obtained from our Monte Carlo simulations.

good, within the limited range they cover, although our velocities at high electric fields are slightly higher than those obtained from previous full band simulations [17].

3.2. Drift Diffusion Method

The Drift Diffusion model represents a first-order approximation to the Boltzmann Transport equation. Here, Poisson's equation is solved self consistently with the carrier continuity equations. A Maxwell-Boltzmann distribution is assumed which is in thermal equilibrium with the lattice temperature. The resulting equations are solved using the commercial device simulator MEDICITM [18]. The Drift Diffusion model therefore provides solutions in the absence of non-equilibrium transport effects. By comparing the results obtained from a calibrated DD model with those obtained from MC, we are able to clearly identify the effect of non-equilibrium transport on device performance.

4. DEVICE RESULTS

The interface scattering model in the Monte Carlo simulations is calibrated by reproducing the universal mobility for Si *p*-MOSFETs [19], as shown in Figure 4. The DD model is calibrated by

FIGURE 4 Effective mobility as a function of the perpendicular electric field.

comparing it with the bulk-steady state velocity-field and I_D - V_G characteristics of a relatively long channel p -MOSFET at a low drain bias of 0.1 V obtained from MC simulations, shown in Figures 5 and 3 respectively. The low drain bias ensures the absence of non-equilibrium transport effects. The I_D - V_G characteristics are used to calibrate the electrostatics and the low-field mobility. We find that a low-mobility of $200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ achieves the best agreement with Monte Carlo data. The saturation velocity, V_{sat} and other appropriate parameters are calibrated so as to obtain the closest agreement with the bulk-steady state velocity-field characteristics (Fig. 3). The results

FIGURE 5 I_D - V_G data for a long channel Si p -MOSFET, $V_{DS} = -0.1 \text{ V}$. Data shown from both MC (solid symbols and line) and DD (open symbols and dashed line) models.

(DD and MC) for the 25 and 50 p -MOSFETs, are shown in Figures 6 and 7 respectively.

We can see that the results from DD are consistently slightly lower than the results obtained from MC. This may be attributed to the presence of non-equilibrium transport effects and velocity overshoot in the Monte Carlo simulations and is consistent with the increasing difference between MC and DD, as channel lengths are shrunk. Although non-equilibrium effects are clearly present in the p -MOSFETs with decanano dimensions, their influences on drive current is not significant; they have also been observed in

FIGURE 6 I_D - V_D simulation results for Si p -MOSFETs, for 25 nm 'Well Tempered' p -MOSFET, obtained from both MC (solid symbols with lines) and DD (open symbols).

FIGURE 7 I_D - V_D simulation results for Si p -MOSFETs, for 50 nm 'Well Tempered' p -MOSFET, obtained from both MC (solid symbols with lines) and DD (open symbols).

n-MOSFETs. Non-equilibrium transport effects become important when the electric fields are such that the carriers are able to move a significant portion of the channel length without reaching equilibrium. The velocities (or energies) in such circumstances are often higher than the equilibrium velocity field characteristics (shown in Fig. 3), which is one of the assumptions at the heart of the DD model. The resulting higher velocities within the MC simulations lead to higher drain current characteristics than those predicted by the DD model.

5. CONCLUSIONS

Two-dimensional Monte Carlo simulations of 'Well Tempered' Si *p*-MOSFETs with gate lengths of 25 and 50 nm have been performed. However, it should be noted that the 25 and 50 nm device designs are hypothetical and based on process technology that is still very much in the development stage. By comparing Monte Carlo simulations with carefully calibrated Drift Diffusion results, we have shown that non-equilibrium transport is important for understanding the high current device characteristics in sub 0.1 μm *p*-MOSFETs.

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