Analytic I–V Model for Single-Electron Transistors

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We present an analytical model for the I–V characteristics of a single-electron transistor, which may be incorporated in a conventional circuit simulator, such as SPICE. Our model takes as its input the physical SET characteristics (capacitances and tunnel resistances, which may be determined experimentally), and it yields I–V curves which are in excellent agreement with the ones obtained from full-scale Monte Carlo simulations.

Keywords: Nanoelectronics; Single-electron transistor; Coulomb blockade; Device simulation; Circuit simulation

INTRODUCTION

Single-electron transistors (SET) offer the promise of ultra-high integration densities and ultra-low power consumption [1]. Considerable effort has been expended over the past decade, or so, in the understanding of the physical principles of SET operation, and this topic has reached a quite mature stage [2]. The fabrication technology of SET's has also come a long way, from its beginnings with individual metallic islands operating at cryogenic temperatures, to device structures approaching room-temperature operation.

The development of large-scale SET circuits will require the development of simulation tools, and some work has been done in this area in recognition of this need [3–5]. Most simulation approaches are based on the Monte Carlo technique, and the main challenges is to reconcile

the numerical expense of this method with the requirement of an economical device model which may be used for the simulation of large circuits.

In this paper, we present an analytical model for the I–V characteristics of a single-electron transistor, which may be incorporated in a conventional circuit simulator, such as SPICE. Our model takes as its input the physical SET characteristics (capacitances and tunnel resistances, which may be determined experimentally), and it yields I–V curves which are in excellent agreement with the ones obtained from full-scale Monte Carlo simulators, such as SIMON [6].

THE MODEL

Our model is based on the schematic SET structure shown in Figure 1. Electrons may tunnel across the

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FIGURE 1 SET schematic with source (s), drain (d), and gate (g) contacts. The source (drain) tunnel junctions are characterized by junction capacitances C_s (C_d) and tunnel resistances R_s (R_d). The gate contact is capacitively coupled (C_g) to the central island.

source and drain junctions, and these tunneling rates Γ are given by the “orthodox theory” of single-electron tunneling.

$$\Gamma = \frac{1}{e^2 \cdot R_T} \frac{-\Delta E}{1 - \exp(\Delta E/k_B T)}, \quad (1)$$

where $\Delta E = E_{\text{after}} - E_{\text{before}}$ is the change in the free energy during a tunneling event.

The main insight of our work is that out of all many possible tunnel events which contribute to the current (and which are included in the full Monte Carlo models), only a few are truly significant and need to be considered. Specifically, current across the SET may be viewed as the combined process of an electron tunneling first across the source- and then the drain junction (with rates Γ_s and Γ_d respectively). The current then can be written as:

$$I_{ds} = e \cdot \frac{\Gamma_s \cdot \Gamma_d}{\Gamma_s + \Gamma_d}, \quad (2)$$

where the rates (within the “orthodox theory”) are analytic functions of the SET parameters and the applied biases, V_{ds} and V_{gs} . Specifically, the rates given by the changes in energy which can be expressed as junction charges in the

following way:

$$\begin{aligned} \Delta E_s &= \frac{e}{C_\Sigma} \cdot Q_s \quad \text{with} \\ Q_s &= (C_d + C_g/2) \cdot V_{ds} + C_g \cdot V_{gs} - e/2 + Q_0 \end{aligned} \quad (3)$$

$$\begin{aligned} \Delta E_d &= \frac{e}{C_\Sigma} \cdot Q_d \quad \text{with} \\ Q_d &= (C_s + C_g/2) \cdot V_{ds} + C_g \cdot V_{gs} - e/2 + Q_0 \end{aligned} \quad (4)$$

In the above expressions, C_Σ is the sum of all capacitances and Q_0 represents some background charge.

This model is valid as long as the central island has one extra electron, *i.e.*, the one that carries the current. The range of validity of the model can be expressed as:

$$0 < Q_s < e \quad \text{and} \quad 0 < Q_d < e \quad (5)$$

For bias conditions outside this range of validity, a straightforward extrapolation procedure may be applied for the rates, and thus the current. More details can be found in a forthcoming publication [7].

RESULTS

Figure 2 shows the result of this model for symmetric SET structure (*i.e.*, source and drain junctions with identical parameters; for this example, we chose values of $C_g = 5$ aF, $C_s = C_d = 1$ aF, $R_s = R_d = 100$ M Ω , and the temperature was assumed to be $T = 3$ K). The lower panels show the tunneling rates and the upper panels the respective resulting drain currents, according to Eq. (2), as a function of the gate bias with the drain bias held constant ($V_{ds} = 30$ mV). The solid line in the upper panels, which is the same in (a) and (c), shows the current obtained from the full Monte Carlo simulation using SIMON [6]. The range of validity of the above model (*i.e.*, only one electron hops across the island) is indicated by the full circles, and the open circles indicate the presence of more

FIGURE 2 The dots in the upper panels, (a) and (c), show the SET current according to Eq. (2) for the rates in the respective lower panels, (b) and (d); the solid line, which is the same in (a) and (b), shows the current obtained from the full Monte Carlo simulations using SIMON [6]. The range of validity of the basic model (inequalities (5)) is indicated by the full circles, and the open circles indicate that the rates need to be modified. A simple extrapolation procedure (compare (b) and (d)) yields excellent agreement between our simple analytical model and the full Monte Carlo simulations, as can be seen in panel (d).

FIGURE 3 Comparison of our analytical model (symbols) and the full Monte Carlo simulations using SIMON [6] (solid lines) for both a symmetrical SET structure, shown in panel (a), and an asymmetrical SET structure, shown in panel (b).

than the one extra electron on the island. Panel (a) shows that simply using the rates of the “orthodox theory” gives excellent agreement with SIMON

when only one extra electron carries the current (full circles), but underestimates the current when there are extra electrons involved (open circles).

It is clear that the rates outside the range of validity of our model (open circles) have to be modified, and we chose the simplest modification of simply leaving them constant. Panel (d) shows the modified rates according to this simple extrapolation, which takes the flow of extra electrons into account. The resulting current is in excellent agreement with the full Monte Carlo simulator, as can be seen in panel (c).

Figure 3 shows the results of our model for several drain biases and for symmetrical and asymmetrical junctions. Figure 3(a) shows the results for a symmetrical SET with the following parameters: $C_g = 3.2$ aF, $C_s = C_d = 1.6$ aF, $R_s = R_d = 100$ M Ω ; and Figure 3(b) is for an asymmetrical SET with parameter values of: $C_g = 3.2$ aF, $C_s = 2.4$ aF, $C_d = 1.6$ aF, $R_s = 80$ M Ω , $R_d = 100$ M Ω . The predictions of our unmodified model are indicated by the full dots (relations (5) are satisfied) and the open circles indicate the modification due to the extrapolation of the rates when inequalities (5) are not valid. The solid lines are the results for SIMON. We find excellent agreement between our simple analytical model and full-scale Monte Carlo simulations.

SUMMARY

We have found that a simple analytical model for the I–V characteristics of a single-electron transistor yields excellent agreement with full-scale Monte Carlo simulations. Our model is based on the physical picture that the SET current is primarily carried by one extra electron on the

central island and with tunneling rates which are given by the “orthodox” theory of single-electron phenomena. When more events need to be considered, *i.e.*, inequalities (5) are no longer satisfied, straightforward extrapolation procedures may be applied, which yield excellent agreement with Monte Carlo simulators, such as SIMON.

Our I–V model is sufficiently simple to make it useful for circuit simulations. We have already incorporated it in standard SPICE simulators, and these results will be presented elsewhere [7].

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