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Random Pattern Testability Enhancement by Circuit Rewiring*

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Generally, there exist random-pattern resistant faults that result in the poor fault coverage in Build-In Self-Testing (BIST) scheme. In this paper, we propose a method to enhance the random pattern testability by a circuit restructuring technique, called *circuit rewiring*. The basic idea of rewiring is to replace a wire by another wire with the circuit functionality remaining unchanged. For two types of rewiring, fanin rewiring and fanout rewiring, we first analyze the testability change for each type of wire replacement. Based on the analysis, an efficient algorithm is given to enhance circuit testability. For a poor observability node, we try to increase its observability by adding an additional fanout to the node and removing an alternative wire whose source node has relatively good observability. The technique does not introduce any hardware overhead and performance degradation since a wire addition is followed immediately by another wire removal. Thus, it is basically cost-free when compared to other testability enhancement techniques.

Keywords: Circuit rewiring; Alternative wire; Dominator; Testability; Observability; Random pattern

1. INTRODUCTION

Testing a digital circuit is an experiment in which the circuit under test (CUT) is exercised by applying a sequence of input test patterns and then its output responses are analyzed to ascertain whether there exist faults in the circuit. *Built-In Self-Testing* (BIST) has been widely used in testing modern circuits or chips, and the basic idea is to have the circuit test itself [1, 2]. Basically, BIST of logic circuits can be divided into two major categories: *random* testing and *exhaustive* testing. By embedding a built-in device such as *linear feedback shift register* (LFSR) inside the chip, we

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can have a sequence of random test patterns generated if the LFSR is initiated with a proper seed value. The defects that occur can be sensitized and detected if the number of random test patterns is large. Of course, there is no real random pattern generator as long as the machine is built by human, since bit dependency occurs. However, the test vectors generated still have many properties of random patterns and are called *pseudo-random* test patterns [3]. The problem with pseudo-random testing lies in the difficulty of enhancing the random pattern testability for circuits containing many random-pattern resistant faults.

Basically, the random-pattern resistance problem is solved by applying *weighted* random patterns [4, 14, 19] or by inserting *test points* [13, 15–18]. The basic idea of weighted random pattern testing is to test the logic with biased random patterns, *i.e.*, the numbers of logic 1 and logic 0 applied to each input are not equal. This can be achieved by building a weighted random pattern generator from an LFSR with AND/OR gates. Substantial improvement can be obtained if the test patterns are properly weighted. Instead of changing the distribution of random patterns, the other major approach is to modify the logic by inserting test points such that the detection probabilities of all random-pattern resistant faults can be increased [15]. Both approaches incur hardware overhead and performance degradation.

In this work, we propose a method that is able to enhance the random pattern testability of the CUT by a circuit restructuring technique called circuit rewiring. The rewiring technique for testability enhancement has the potential of no hardware overhead and performance degradation. The basic idea of circuit rewiring is to find a wire to replace another one without changing the circuit function. Thus, it is beneficial to supersede a hard-to-test line using another easy-to-test line. Given a set of random test patterns, all undetected faults can be identified by fault simulation. The fault coverage accomplished by the set of random patterns can be further increased by circuit rewiring. In this experiment, we try to rewire the circuit such that the observabilities of undetected lines can be enhanced. Simulation results demonstrate that the circuit rewiring technique can successfully break the random pattern barrier for many benchmark circuits. Without rewiring, the fault coverage of a CUT might saturate and remain a constant regardless of more test patterns being applied. However, the fault coverage can be made higher if circuit lines are properly rewired. We have observed that circuit rewiring increases random pattern fault coverage in most cases.

The background of circuit rewiring is described in Section 2, while Section 3 investigates the relationship between circuit rewiring and random pattern testability, and a heuristic rewiring method is proposed. Simulation results are provided in Section 4, and Section 5 concludes the work.

2. BACKGROUND

This paper applies the idea of rewiring to improve the testability of a circuit. There have been several studies [5–7, 10, 12] on how to logically exchange wire connections under the constraint that the circuit function remains unchanged. In this section, we will review the basic concept of rewiring which has the ability of modifying a circuit. In the next section, an algorithm using circuit rewiring for testability enhancement will be presented.

By definition, wire A is an *alternative* wire of wire B, if we can replace wire B by wire A. Consider the circuit shown in Figure 1, wire $g_1 \rightarrow g_4$ can be replaced by wire $g_5 \rightarrow g_9$ with the circuit function remaining unchanged, *i.e.*, both circuits

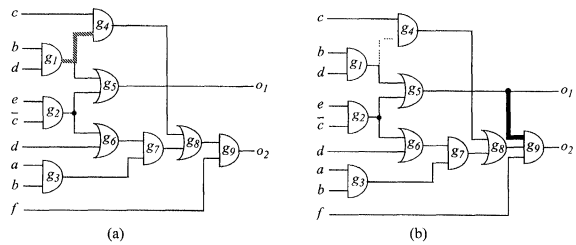

FIGURE 1 An example for single alternative wire replacement.

in Figure 1 are functionally equivalent. In this case, we say that wire $g_5 \rightarrow g_9$ is an alternative wire of wire $g_1 \rightarrow g_4$. Additionally, the alternative wires are mutually alternative, *i.e.*, if wire A is an alternative wire of wire B then wire B is also an alternative wire of wire A. Thus, we can also replace $g_5 \rightarrow g_9$ by $g_1 \rightarrow g_4$ in Figure 1.

Let us further examine the same example. First, a *redundant* wire is a wire that can be added (removed) to (from) a circuit without changing the circuit function. It can be found that the non-existing wire $g_5 \rightarrow g_9$ is redundant in Figure 1(a) and can be added to the circuit. On the other hand, $g_1 \rightarrow g_4$ is ir-redundant in Figure 1(a). However, when wire $g_5 \rightarrow g_9$ is added to the circuit, wire $g_1 \rightarrow g_4$ becomes redundant and can thus be removed from the circuit (Fig. 1(b)). From this example, we can observe that an originally irredundant wire may become redundant after adding some redundant wire to a circuit. The way of redundancy addition and removal forms the basic idea for the circuit rewiring technique.

The procedure of finding an alternative wire for the target wire first searches a non-existing wire, called *candidate* connection, that once added makes the target wire redundant. Then, the rewiring technique checks whether the candidate connection is redundant, *i.e.*, whether adding the non-existing wire preserves the circuit functionality. It is only when the candidate connection is verified as redundant, we can then add the candidate connection and further remove the target wire. All redundancy checks can be done through reasoning of automatic test pattern generation (ATPG). More details of finding alternative wires can be found in [7].

3. REWIRING FOR TESTABILITY

In the section, the effect of rewiring to circuit testability is first analyzed, and then a heuristic method for testability enhancement will be presented. In order to test a stuck-at fault, it is required to activate the fault and then propagate the fault effect to at least one primary output. By definition, the probability of a primary input vector to activate a fault f is called the *controllability* of f, while that to propagate the fault effect of f to a primary output is called the *observability* of f. Both controllability and observability of a fault adequately indicate the degree of difficulty to activate the fault and to observe the fault effect. Thus, the testability of a fault can be measured by these two values.

For observability, in general, if a node is close to a primary output, then the observability of the node is high. A primary output node is considered to be fully observable. Further, if a node has many fanouts, the node has good opportunity to be highly observable because the fault effect can propagate to primary outputs from one of its fanouts. (We neglect the fault-masking problem.) In a circuit, some nodes may have very good observability such as a primary output node or a node with many fanouts while some nodes may have very poor observability. Since each iteration of the rewiring process allows to add/remove a wire at the fanout of a certain node, the basic idea of our approach is to improve the low observability of a node by adding new fanouts to this node. Thus, special types of rewiring extended from [6] are analyzed, and the effects to circuit testability caused by such rewirings are then investigated. Before further discussion, several definitions are provided. Node B is a transitive fanout of node A, if there exists a path from node A to node B. Node A is a *dominator* of node B (wire C), if every path from node B (wire C) to any primary output must pass through node A. For example, in Figure 1(a), nodes g_8 and g_9 are dominators of both node g_4 and wire $g_1 \rightarrow g_4$.

3.1. Two Special Types of Rewiring

Here, we will describe two special types of rewiring and the first one is named the *fanout rewiring*. In this case, a fanout wire $g_a \rightarrow g_b$ of gate g_a dotted in Figure 2(a) is replaced by another fanout wire

$g_a \rightarrow g_d$ bold in Figure 2(b); additionally, node g_d is restricted to be a dominator of g_b and both gates g_d and g_b must have the *same* type of function, *i.e.*, they are both OR gates as in the figure or AND gates. In Figure 2, let Cone II contain all the wires and gates that are the transitive fanouts of g_a and are dominated by g_d, while let Cone I contain all the wires dominated by g_a. We have the following theorem.

THEOREM 1 *Suppose wire $g_a \rightarrow g_b$ can be replaced by $g_a \rightarrow g_d$ where g_d is a dominator of g_b. A test pattern which an detect a stuck-at fault in Cone* II *after rewiring (Fig. 2(b)), can also detect the same fault before rewiring (Fig. 2(a)). Further, if a test vector can detect a fault in Cone* I *before rewiring (Fig. 2(a)), the same vector can also detect the fault after rewiring (Fig. 2(b)).*

Proof Consider testing line w stuck-at fault in the rewired circuit shown in Figure 2(b). Because g_d is a dominator of w, the side-input g_a must be assigned the noncontrolling value 0. Assigning 0 to g_a will cause both wires $g_a \rightarrow g_d$ in Figure 2(b) and $g_a \rightarrow g_b$ in Figure 2(a) to be "transparent", *i.e.*, their presence will not affect the result. Therefore, any test pattern which can detect w stuck-at fault for the circuit after line substitution is also a test pattern for the same fault in the circuit before line substitution. The case for Cone I and other gate types can be proved similarly. Q.E.D.

LEMMA 1 *If wire $g_a \rightarrow g_b$ is replaced by $g_a \rightarrow g_d$, the testability of a fault in Cone* II *decreases while that in Cone* I *increases.*

Proof This can be directly proved from Theorem 1.

The intuition behind the above theorem and lemma is that after replacing $g_a \rightarrow g_b$ by $g_a \rightarrow g_d$, node g_a has a fanout wire which is closer to the primary outputs, as a result, the observability of g_a increases and so do the wires dominated by g_a. On the other hand, the wires in Cone II has the additional constraint, g_a must be 0 during testing; therefore, the testability for wires in Cone II will decrease after wire replacement.

Another type of rewiring is referred as the *fanin rewiring*. Let the fanin wire $g_a \rightarrow g_d$ of gate g_d dotted in Figure 3(a) be replaced by another fanin wire $g_b \rightarrow g_d$ bold in Figure 3(b). Further, wires dominated by g_a are referred as Cone III and wires dominated by g_b are referred as Cone IV. Suppose there is no multiple fault cancellation problem, the observability of the wires in Cone III will decrease after rewiring because one fanout wire of the gate g_a has been deleted. Since an additional fanout wire is added to gate g_b, the observability of wires in Cone IV will potentially increase.

The change of testability after rewiring can be used to guide wire replacement to improve the circuit testability. For example, since the primary outputs are fully observable, there is no loss of

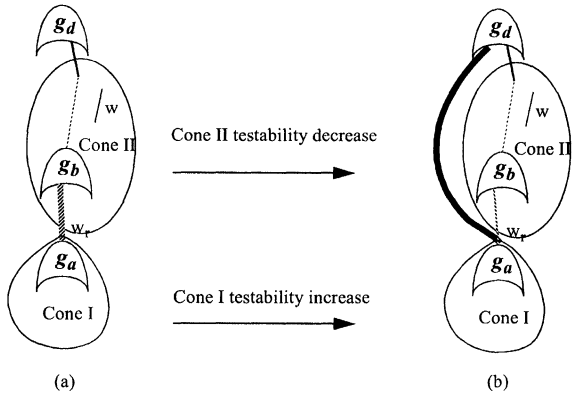

FIGURE 2 Fanout rewiring.

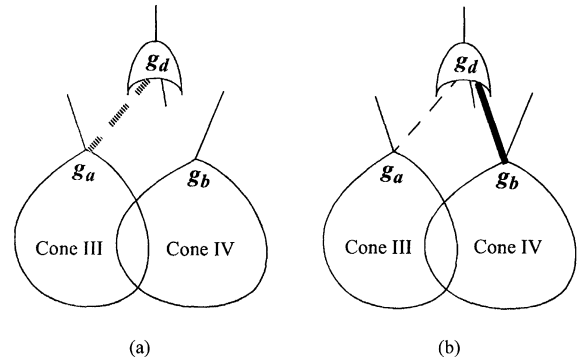

FIGURE 3 Fanin rewiring.

observability by removing any of its fanouts. Consider wire $g_5 \rightarrow g_9$ in Figure 1(b), since g_5 is directly connected to primary output O_1, node g_5 is fully observable. Removing another fanout from g_5 will not decrease the observability of g_5 at all. Therefore, replacing $g_5 \rightarrow g_9$ by $g_1 \rightarrow g_4$ will not decease the observability of g_5 but may increase the observability of g_1 because the number of g_1's fanouts is increased by one.

3.2. A Heuristic for Improving Testability

There are two possibilities in using the circuit rewiring technique for testability enhancement. The first one tries to improve the testability of a CUT without considering what kind of patterns are applied, while the second approach tries to improve the fault coverage for a given set of patterns.

In the first approach, we estimate the fault coverage of the CUT. The estimation can be done by applying testability analysis methods [2, 8, 9, 11]. For each rewiring, the fault coverage of the CUT can be estimated again. In the rewiring technique, when a wire is added to improve the observability of node a, the fanout wire of another node b must be removed and the observability of node b will be reduced. In order to improve the observability of a node, we apply the first approach that removes a wire whose source node has more fanouts to one whose source node has less fanouts. In this way, we are able to "shift" some testability from high testability nodes to low testability nodes.

In the second approach, we assume that a set of random or deterministic test patterns has been given and try to improve the fault coverage for these patterns. First, the patterns are simulated and faults that are not covered by these patterns are identified. Then, we index nodes in such a way that a node that is the transitive fanouts of many undetected faults is given a large number. The objective in this approach is to improve the observabilities for nodes with large indices because increasing the observabilities for these nodes can greatly improve the observabilities of many undetected faults. We will use the same technique as the one used in the first approach to add new fanouts for nodes with large indices. After each rewiring, the circuit must be re-simulated because the fault detection behavior might be changed after each iteration of rewiring step has been taken. That is, the rewiring process can not guarantee the detection of undetected faults; even worse, some detected faults might turn to be undetected. Thus, fault simulation must be performed for each iteration to guarantee that the rewiring process is beneficial.

In the third approach, we estimate the observability of each node in the CUT. Similar to the second approch, the objective of this approach is to improve the observabilities of the nodes with lower observabilities, and also uses the same technique as the one used in the first approach to add new fanouts for nodes with lower observabilities. After each rewiring, we also re-simulate the circuit to estimate the observability of each node in the CUT again.

Consider the example shown in Figure 4(a) with test vector $(a, b, c, d, e) = (0, 1, 0, 1, 0)$. After fault simulation using the test vector, it can be found that stem line g_1 *stuck-at* 1 cannot be detected, and

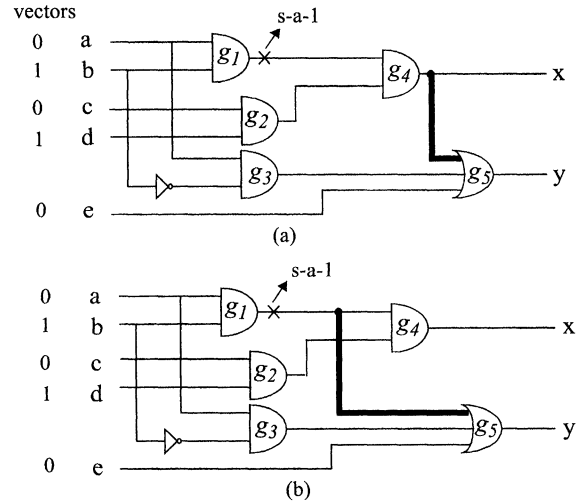

FIGURE 4 An example for testability enhancement.

TABLE I Simulation results (approach 1)

Circuit	# of faults	# of random patterns	# of DF of ckt.org	FC of ckt.org	# of DF of ckt.rm	FC of ckt.rm	Time (sec)
9symml	774	500	709	91.60%	740	95.61	393.25
		1000	760	98.19%	768	99.22	488.11
C1355	1984	500	1876	94.56%	1876	94.56	
C1908	2116	500	1804	85.26%	1804	85.26	7418.50
C2670	3090	1000	2498	81.68%	2561	82.88	26660.14
		5000	2537	82.10%	2572	83.24	48510.96
C3540	4440	2000	4222	95.09%	4222	95.09	81503.50
C432	736	500	690	93.75%	692	94.02	189.08
		1000	690	93.75%	692	94.02	234.10
		*50000	690	93.75%	692	94.02	2495.35
C499	1568	500	1494	95.28%	1502	95.79	657.18
		1000	1535	97.90%	1543	98.41	721.06
		2000	1558	99.36%	1566	99.87	894.10
		5000	1560	99.49%	1568	100.00	1366.11
		*100000	1560	99.49%	1568	100.00	19641.02
C6288	9408	500	9404	99.96%	9404	99.96	20599.70
C880	1280	1000	1221	95.39%	1225	95.70	1011.71
		5000	1259	98.36%	1260	98.44	1980.14
		10000	1268	99.06%	1268	99.06	3040.29
alu2	1762	1000	1464	83.09%	1532	86.95	8561.32
		3000	1481	84.05%	1547	87.80	12216.92
		*50000	1481	84.05%	1547	87.80	108144.58
alu4	3164	5000	2775	87.71%	2830	89.44	44578.30
apex6	2432	5000	2356	96.88%	2374	97.62	14933.60
		10000	2383	97.99%	2394	98.44	23964.05
apex7	922	500	831	90.13%	842	91.32	1152.18
		1000	837	90.78%	848	91.97	685.06
		5000	849	92.08%	860	93.28	1314.10
		10000	859	93.17%	869	94.25	2180.25
		20000	863	93.60%	872	94.58	3886.33
		*100000	863	93.60%	872	94.58	19149.90
b1	48	500	30	62.50%	34	70.83	0.01
		*100000	30	62.50%	34	70.83	4.01
b9	480	500	465	96.88%	472	98.33	120.06
		1000	471	98.12%	476	99.17	140.06
		*50000	471	98.12%	476	99.17	1790.56
c8	930	1000	758	81.51%	762	81.94	439.07
		5000	787	84.62%	787	84.62	907.10
cc	262	100	228	87.02%	236	90.08	11.02
		200	258	98.47%	259	98.85	14.02
cm85a	176	100	156	88.64%	163	92.61	4.02
		200	174	98.86%	175	99.43	4.02
cmb	164	1000	103	62.80%	106	64.63	3.02
		5000	138	84.15%	141	85.98	7.01
		10000	150	91.46%	150	91.46	12.02
comp	510	5000	304	59.61%	325	63.73	169.12
		10000	326	63.92%	343	67.25	248.15
		50000	422	82.75%	437	85.69	978.67
cordic	328	500	256	78.05%	256	78.05	43.03
count	476	500	387	81.30%	397	83.40	43.02
cu	230	500	204	88.70%	214	93.04	17.02
		1000	205	89.13%	215	93.48	19.02
		5000	211	91.74%	221	96.09	39.03
		*50000	212	92.17%	221	96.09	64.03

TABLE II Simulation results (approach 2)

Circuit	# of faults	# of random patterns	# of DF of ckt.org	FC of ckt.org	# of DF of ckt.rm	FC of ckt.rm	Time (sec)
9symml	774	500	709	91.60	755	97.55%	556.68
		1000	760	98.19	773	99.87%	435.56
		2000	771	99.61	774	100.00%	233.07
C1355	1984	500	1876	94.56	1876	94.56%	54.07
C1908	2116	500	1804	85.26	1804	85.26%	6487.14
C2670	3090	1000	2498	81.68	2550	82.52%	11826.18
		5000	2537	82.10	2555	82.69%	21795.32
C3540	4440	2000	4222	95.09	4222	95.09%	18271.36
C432	736	500	690	93.75	692	94.02%	245.41
		1000	690	93.75	692	94.02%	266.08
		*50000	690	93.75	692	94.02%	1852.26
C499	1568	500	1494	95.28	1502	95.79%	666.08
		1000	1535	97.90	1543	98.41%	735.17
		2000	1558	99.36	1566	99.87%	904.12
		5000	1560	99.49	1568	100.00%	1403.15
		*100000	1560	99.49	1568	100.00%	18953.08
C6288	9408	500	9404	99.96	9404	99.96%	1262.23
C880	1280	1000	1221	95.39	1225	95.70%	723.66
		5000	1259	98.36	1260	98.44%	451.40
		10000	1268	99.06	1268	99.06%	71.10
alu2	1762	1000	1464	83.09	1519	86.21%	3766.57
		3000	1481	84.05	1534	87.06%	5351.31
		*50000	1481	84.05	1534	87.06%	83394.63
alu4	3164	5000	2775	87.71	2843	89.85%	53492.16
apex6	2432	5000	2356	96.88	2372	97.53%	3156.88
		10000	2383	97.99	2398	98.60%	3239.53
		50000	2418	99.42	2422	99.59%	9261.08
		100000	2424	99.67	2424	99.67%	7873.49
apex7	922	500	831	90.13	840	91.11%	314.05
		1000	837	90.78	845	91.65%	363.05
		5000	849	92.08	857	92.95%	706.08
		10000	859	93.17	866	93.93%	933.03
		20000	863	93.60	870	94.36%	1692.35
		*100000	863	93.60	870	94.36%	8300.22
b1	48	500	30	62.50	34	70.83%	0.01
		*100000	30	62.50	34	70.83%	3.02
b9	480	500	465	96.88	472	98.33%	56.10
		1000	471	98.12	474	98.75%	61.09
		*50000	471	98.12	474	98.75%	442.12
c8	930	1000	758	81.51	763	82.04%	634.91
		5000	787	84.62	787	84.62%	657.02
cc	262	100	228	87.02	233	88.93%	11.03
		200	258	98.47	259	98.85%	2.01
		300	262	100.00	262	100.00%	0.00
cm85a	176	100	156	88.64	163	92.61%	4.02
		200	174	98.86	175	99.43%	1.01
		300	176	100.00	176	100.00%	0.00
cmb	164	1000	103	62.80	105	64.02%	4.02
		5000	138	84.15	138	84.15%	9.02
		10000	150	91.46	150	91.46%	13.03
comp	510	5000	304	59.61	310	60.78%	38.06
		10000	326	63.92	332	65.10%	69.09
		50000	422	82.75	424	83.14%	289.52
		100000	435	85.29	437	85.69%	311.07
		200000	445	87.25	447	87.65%	637.15
cordic	328	500	256	78.05	257	78.35%	81.20
cu	230	500	204	88.70	209	90.87%	19.06
		1000	205	89.13	210	91.30%	21.05
		5000	211	91.74	216	93.91%	42.09
		10000	212	92.17	217	94.35%	37.02
		*50000	212	92.17	217	94.35%	162.08

TABLE III Simulation results (approach 3)

Circuit	# of faults	# of random patterns	# of DF of ckt.org	FC of ckt.org	# of DF of ckt.rm	FC of ckt.rm	Time (sec)
9symml	774	500	709	91.60%	739	95.48%	371.09
		1000	760	98.19%	771	99.61%	472.10
C1355	1984	500	1876	94.56%	1876	94.56%	127.07
C1908	2116	500	1804	85.26%	1804	85.26%	1970.48
C2670	3090	1000	2498	81.68%	2550	82.52%	36266.61
		5000	2537	82.10%	2563	82.94%	94808.92
C3540	4440	2000	4222	95.09%	4222	95.09%	49027.77
			4244	95.59%	4244	95.59%	72015.88
C432	736	500	690	93.75%	692	94.02%	149.05
		1000	690	93.75%	692	94.02%	169.04
		*50000	690	93.75%	692	94.02%	2024.41
C499	1568	500	1494	95.28%	1502	95.79%	632.08
		1000	1535	97.90%	1543	98.41%	744.08
		2000	1558	99.36%	1566	99.87%	881.11
		5000	1560	99.49%	1568	100.00%	1320.17
		*100000	1560	99.49%	1568	100.00%	35941.18
C6288	9408	500	9404	99.96%	9404	99.96%	32278.51
C880	1280	1000	1221	95.39%	1226	95.78%	1512.29
		5000	1259	98.36%	1260	98.44%	2911.74
		10000	1268	99.06%	1268	99.06%	4003.97
alu2	1762	1000	1464	83.09%	1518	86.15%	3901.32
		3000	1481	84.05%	1535	87.12%	5949.40
		*50000	1481	84.05%	1535	87.12%	52435.91
alu4	3164	5000	2775	87.71%	2842	89.82%	36426.47
apex6	2432	5000	2356	96.88%	2374	97.53%	12171.90
		10000	2383	97.99%	2398	98.60%	20083.04
		50000	2418	99.42%	2421	99.55%	91871.47
		100000	2424	99.67%			
apex7	922	500	831	90.13%	841	91.21%	1086.29
		1000	837	90.78%	848	91.97%	1221.27
		5000	849	92.08%	860	93.28%	2278.55
		10000	859	93.17%	869	94.25%	3691.02
		20000	863	93.60%	872	94.58%	6785.89
		*100000	863	93.60%	872	94.58%	29931.91
b1	48	500	30	62.50%	34	70.83%	0.00
		*100000	30	62.50%	34	70.83%	4.01
b9	480	500	465	96.88%	471	98.12%	99.03
		1000	471	98.12%	475	98.96%	117.04
		*50000	471	98.12%	475	98.96%	1510.20
c8	930	1000	758	81.51%	761	81.83%	449.07
		5000	787	84.62%	787	84.62%	909.14
cc	262	100	228	87.02%	234	88.93%	16.03
		200	258	98.47%	259	98.85%	21.02
		300	262	100.00%	262	100.00%	1.02
cm85a	176	100	156	88.64%	163	92.61%	7.02
		200	174	98.86%	175	99.43%	8.02
		300	176	100.00%	176	100.00%	0.00
cmb	164	1000	103	62.80%	106	64.63%	4.01
		5000	138	84.15%	140	85.37%	9.02
		10000	150	91.46%	150	91.46%	14.02
		20000	152	92.68%	152	92.68%	25.02
comp	510	5000	304	59.61%	325	63.73%	184.05
		10000	326	63.92%	343	67.25%	275.07
		50000	422	82.75%	437	85.69%	1055.25
		100000	435	85.29%	450	88.24%	2068.52
		200000	445	87.25%	461	90.39%	3986.19
cordic	328	500	256	78.05%	256	78.05%	71.05
cu	230	500	204	88.70%	213	92.61%	17.04

TABLE III (Continued)

Circuit	# of faults	# of random patterns	# of DF of ckt.org	FC of ckt.org	# of DF of ckt.rm	FC of ckt.rm	Time (sec)
		1000	205	89.13%	214	93.04%	19.02
		5000	211	91.74%	220	95.65%	37.03
		10000	212	92.17%	221	96.09%	62.03
		*50000	212	92.17%	221	96.09%	264.09

an index is assigned to it. By assumption, node g_1 has the largest index, so one more fanout is added to node g_1 for improving its observability. Since $g_1 \rightarrow g_5$ (bold in Fig. 4(b)) can replace $g_4 \rightarrow g_5$ (bold in Fig. 4(a)) whose source node g_4 has high observability, we perform this wire replacement in Figure 4(b). After rewiring, the fault simulation process is performed again, and stem line g_1 $s-a-1$ is successfully detected by test vector $(0,1,0,1,0)$. The process will be repeated until either there is no fault remaining undetected or no further rewiring is possible.

The problem with the second approach is that, for each rewiring, the fault simulation process must be executed to ensure that the fault coverage is not devastated. It will be more efficient if there are rules to guide the wire selection and the rewiring processes such that the fault simulation process can be avoided for each rewiring. However, this is very difficult (if not impossible) since the rewiring process results in global effects to the entire circuit and no simple rules can be derived. Thus, to ensure a better solution, fault simulation needs to be performed for each rewiring process. However, we feel that this is still tolerable because the process of rewiring for testability is a one-time process and is a worthwhile effort.

```
rewire_for_testability (network, n) {
  PN = generate_random_patterns (n);
  FC_o = fault_simulation (network, PN);
  index_all_node (network);                    (Reference Section 3.2)
  for each node i {
    for each fanin node k {
      if (there exists alternative wire) {
        find the node m with the maximum index;
        rewire wire k->i to wire m->i;
        FC_m = fault_simulation (network, PN);
        if (FC_m <= FC_o)
          undo rewiring;                       (rewire wire m->i to wire k->i)
        else
          FC_o = FC_m;
      }
    }
  }
  return FC_o;
}
```

FIGURE 5 Pseudo code of approach.

4. SIMULATION RESULTS

In order to evaluate the performance for the rewiring technique, the simulation software has been developed based on the SIS environment. We summarize the simulation results by Tables I, II and III. The simulation results of these three tables are generated by applying three different approaches to indexing nodes. Table I shows the simulation results by applying the first approach that assigns an index to the node of a circuit with the fanout number of each node. And Tables II and III show the simulation results by applying the second approach with the number of undetected faults on the input cone of each node indexed and the third approach with the observability of each node indexed, respectively. A pseudo-code example for approach 2 is shown in Figure 5.

Table II shows the results of computer simulation using the second approach, and it can be found that the rewiring process improves random pattern fault coverage in most cases. Note that different random test pattern lengths are used depending on the random pattern resistances of these circuits. It appears that the rewiring process is able to break the random test pattern barriers for many circuits. For example, the fault coverage of circuit ALU2 remains 84.05% after 3,000 random test patterns have been applied. In fact, we tried 50,000 random test patterns for ALU2 and failed to improve the fault coverage. However, after rewiring, the fault coverage can be easily improved to 86.21% by 1,000 random test patterns and to 87.06% by 3,000 random patterns. Each number n following the asterisk ($^*n$) in Table II indicates that the coverage can no longer be improved even by applying n random test patterns. Thus, it can be observed that circuit rewiring has successfully broken the random pattern barriers for many circuits. Of course, there are cases where rewiring fails to improve the fault coverage, and other design for testability methods that really add extra circuit must be used. All experiments are done on the platform of UltaSparc workstation.

5. CONCLUSIONS

In this paper, we have presented a method to enhance the random pattern testability by circuit rewiring. The basic idea is to remove fanouts for gates whose observabilities have been relatively high; meanwhile, alternative wires are added to increase the observabilities for gates whose observabilities are relatively low. The wire addition and removal process does not change the circuit function. Compared with other random testability enhancement approaches, the proposed circuit rewiring technique does not introduce any hardware overhead, thus it is basically a cost-free method. Simulation results demonstrate that the rewiring technique is able to successfully break the random pattern barrier of the CUT and to improve the random test fault coverage efficiently for most circuits. The approach can also be incorporated into other random testability enhancement methods (needs hardware overhead) as a preprocess, *i.e.*, the random testability can first be improved using the proposed method, then other methods are used to gain higher fault coverage with tolerable hardware overhead. So far, the majority of computing time is used in fault simulation for each rewiring process. The future research includes: (a) finding rules to guide circuit rewiring to avoid excessive fault simulation, or (b) using a smarter fault simulation method if the rules cannot be obtained.

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