VLSI Design, 2002 VOL. 15 (1), pp. 477–483

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Charge Pump Circuits for Low-voltage Applications*

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(Received 1 February 2001; Revised 26 March 2001)

In this paper, a low-voltage, high performance charge pump circuit, suitable for implementation in standard CMOS technologies is proposed. Its pumping operation is based on cascading several cross-connected NMOS voltage doubler stages. For very low-voltage applications (1.2 V, 0.9 V), where the performance of the NMOS transistors is limited due to body effect, two improved versions of the charge pump with cascaded voltage doublers (charge pump with CVD) are also proposed. The first utilises PMOS transistors (charge pump with CVD-PMOS) in parallel to the cross-connected NMOS transistors, while the second improves the pumping gain by boosting the clock amplitude (charge pump with CVD-BCLK). Simulations at 50 MHz have shown that a five-stages charge pump with CVD can achieve a 1.5–8.4 V voltage conversion. For the same stage number and frequency, an output voltage of 4 and 7.3 V can be generated from 0.9 V, by using the charge pump with CVD-PMOS and the charge pump with CVD-BCLK, respectively.

Keywords: Charge pump; Flash memory; Low voltage; Voltage doubler; Dickson; Boosted clock

INTRODUCTION

Charge pump circuits are mostly used in applications where voltages higher than the nominal power supply voltage are needed. High voltages are necessary for the programming of nonvolatile memories, for biasing the PMOS well in order to reduce the leakage currents and for driving electrostatic actuators and the analogue switches in switched-capacitor systems. The charge pump circuit reported by Dickson has been widely used, for generating high voltages [1,2]. The specific circuit makes use of capacitors interconnected with diodes and coupled in parallel by two non-overlapping clocks. The diodes of the Dickson circuit can be replaced by NMOS transistors as shown in Fig. 1, resulting in a more efficient implementation [1,3,4]. However, the resulting circuit performance is limited due to the threshold voltage drop of the NMOS devices and the reverse charge-sharing phenomenon. Moreover, for high output generated voltages, the increase in the threshold voltage due to the body effect, can significantly reduce the pumping gain.

In order to overcome the above-mentioned problems, the charge pump of Fig. 2(NCP-2), reported in Ref. [5], utilises the charge transfer switches (MSi transistors). Each of the MSi transistors is controlled by the pass transistors MNi and MPi as clearly depicted in Fig. 2. In that way the charge transfer switches can be turned off completely when required, preventing the reverse charge flow. Also, they can be turned on more effectively by the high voltage generated in the next stage.

More advanced schemes have been applied to increase the voltage gain, such as floating PMOS with bootstrapped gates [6], PMOS transistors with controllable substrate [7] and four phase clocking [8]. The proposed charge pump circuit with CVD can generate higher output voltage when compared with the Dickson charge pump using NMOS devices and the NCP-2, without employing any of the above mentioned complicated circuit techniques. Moreover, for very low-voltage operation, two improved versions of the charge pump circuit with CVD are also proposed, suitable for operation even under a power supply voltage of 0.9 V.

The rest of the paper is organised as follows: the second section describes the charge pump with cascaded voltage doublers. In the third section, the improved charge pumps for low voltage applications are proposed. Finally in

*Based on "A CMOS charge pump for low voltage operation" by Y. Moisiadis, I. Bouras and A. Arapoyanni which appeared in *IEEE International Symposium on Circuits and Systems* 2000, (ISCAS '00), Geneve, Switzerland, Vol. 5, pp. 577–580.

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ISSN 1065-514X print/ISSN 1563-5171 online
DOI: 10.1080/1065514021000012084

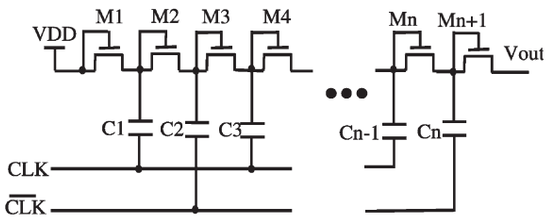

FIGURE 1 The Dickson charge pump circuit with NMOS.

the fourth section, the proposed charge pumps are compared with the Dickson and the NCP-2 charge pump.

CHARGE PUMP WITH CASCADED VOLTAGE DOUBLERS

The proposed charge pump with cascaded voltage doublers (charge pump with CVD) is presented in Fig. 3 [9]. It utilises the cross-connected NMOS voltage doubler [10], as a pumping stage. The cascade operation ensures that the high voltage generated by each stage is fed in the next stage. For a power supply voltage and clock amplitude equal to VDD, the output voltage from each stage is higher than the voltage generated from its previous stage, by the voltage value VDD. (This is the ideal voltage value if we ignore the influence of the body effect and the parasitic elements). As a result, for a n-stage charge pump with CVD, the generated high output voltage will be equal to:

$$V_{\text{out}} = V_{\text{DD}} + n\,V_{\text{DD}} = (n+1)V_{\text{DD}} \qquad (1)$$

The charge transfer from one stage to the next is accomplished by using a pair of PMOS transistors as serial switches (MPi transistors). To ensure that during the operation of the charge pump, the well of the PMOS switches is always in the higher voltage between source and drain, we adopt the principle of bulk switching, using the MSi PMOS transistors [11]. Each of the MSi transistors is dedicated to bias the well of one of the MPi transistor, in the highest voltage between source and drain. Two-phase overlapping clocking is used to drive the pumping capacitors of each pumping stage. Better results can be obtained with the use of a non-overlapping clocking scheme.

IMPROVED CHARGE PUMPS WITH CASCADED VOLTAGE DOUBLERS

For low-voltage operations and large number of pumping stages, the cross-connected NMOS transistors present limited driving capability due to body effect, resulting in reduced output voltage. To overcome this limitation, we propose a second version of the charge pump with CVD, using PMOS transistors in parallel with the cross-connected NMOS (charge pump CVD-PMOS) [9]. These PMOS transistors (MEi transistors) are inserted only in the stages, where the NMOS transistors exhibit limited performance due to body effect. Each of the PMOS transistors is controlled by a pair of NMOS and PMOS transistors (MCi transistors), according to the scheme shown in Fig. 4, using the Vn, $\overline{Vn}$ pulses of the current stage and the $Vn-1$, $\overline{Vn-1}$ pulses of the previous stage. In this way the PMOS are completely turned on and turned off, avoiding the charge-sharing phenomenon from one stage to its previous. The substrates of the PMOS are all connected to the common node Vsub, to ensure that they are always tied in the higher voltage between source and drain.

Figure 5 shows the Vn, $\overline{Vn}$, $Vn-1$ and $\overline{Vn-1}$ pulses, used for the control of the transistors MEi. In the case of stage $n-1$, both $Vn-1$ and $\overline{Vn-1}$ pulses vary between the voltage levels $(n-1)$VDD and nVDD, while in the next stage pulses Vn and $\overline{Vn}$ exhibit a voltage variation between the voltage levels nVDD and $(n+1)$VDD. Consequently, during period A transistor MC1 is on, driving the gate of transistor ME1 with a voltage $(n+1)$ VDD, while transistor MC2 is off. As a result, transistor

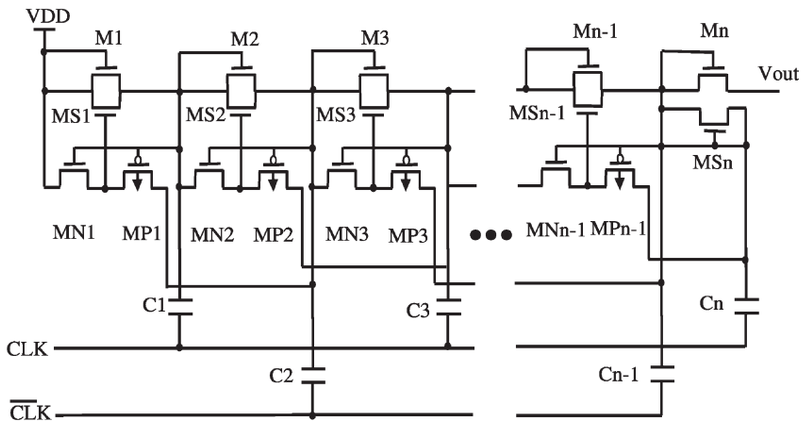

FIGURE 2 The NCP-2 charge pump circuit.

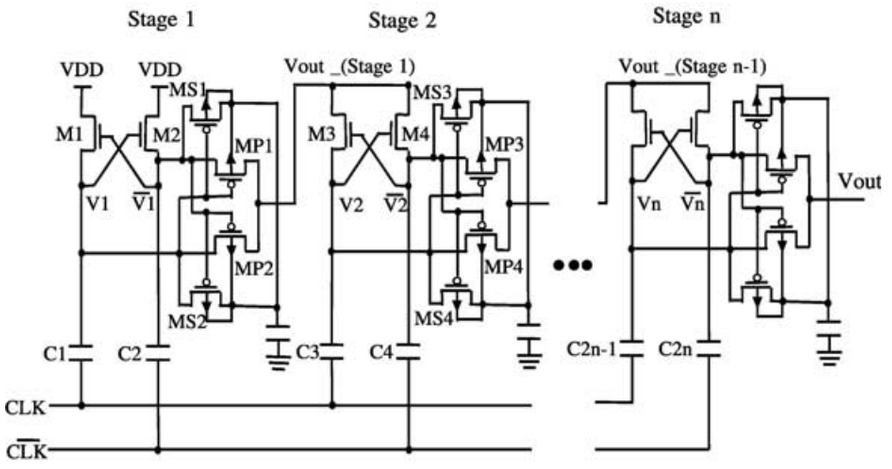

FIGURE 3 The proposed charge pump with the cascade voltage doublers (charge pump with CVD).

ME1 is completely off. In the next time period B, transistor MC1 is off while transistor MC2 is on. Transistor ME1 is also on, since its gate is charged to a voltage value $(n-1)$VDD. In this way transistor ME1 assists the NMOS transistor M1, whose conductivity is reduced due to the body effect. Unlike M1, transistor ME1 does not suffer from body effect since its substrate is always connected to $(n+1)$VDD. Similarly, transistor ME2 is on during period A, conducting in parallel with transistor M2, while during period B transistor ME2 is off.

For very low-voltage applications, the pumping gain of the charge pump with CVD can be further increased by boosting the clock amplitude. The proposed charge pump with CVD and boosted clock (charge pump with CVD-BCLK) is shown in Fig. 6, along with the circuitry used for the clock boosting. All the pumping capacitors C1–Cn are driven by the boosted clock pulses BCLK and $\overline{\text{BCLK}}$. A cross-connected NMOS pair is applied for boosting the clock pulses. The high voltage Vpp for biasing the substrate of the PMOS transistors MB3 and MB5 can be obtained from the first stage output of the charge pump circuit.

SIMULATION RESULTS

The simulations were performed with the HSPICE simulator, using a standard 0.35 um CMOS technology. The threshold voltages of the NMOS and PMOS devices are 0.52 and -0.65 V, respectively. All the simulations were carried out at 50 MHz.

In a double-well technology, the NMOS transistors are shared the same p-substrate, which is connected to GND. As a result, the highest value of the charge pump output voltage is limited by the gate oxide breakdown voltage (BV_{ox}) and the breakdown voltage between the n^+/p-substrate (BV_{n+-s}) (Fig. 7). For the specific technology typical values of the above voltages are

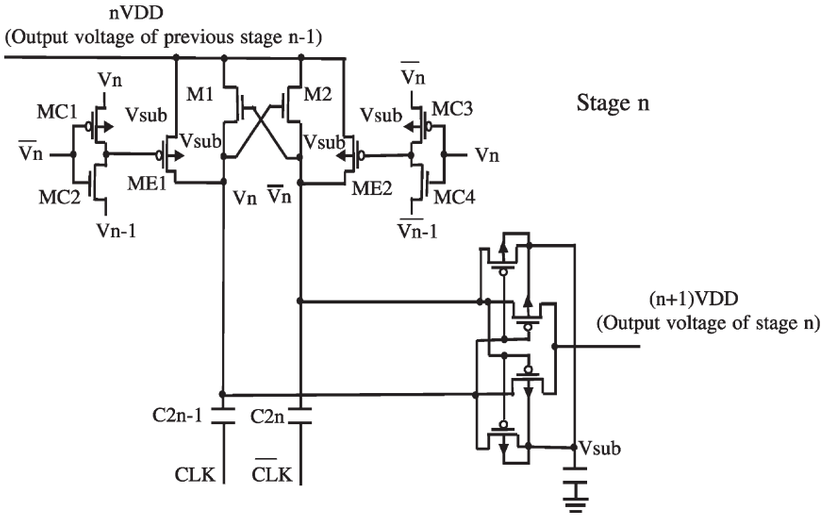

FIGURE 4 One stage of the proposed charge pump with the cascade voltage doublers and PMOS transistors (charge pump with CVD-PMOS).

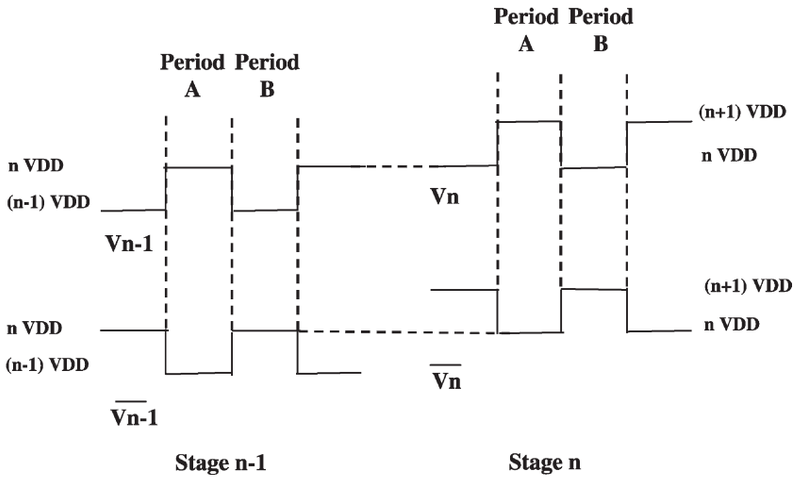

FIGURE 5 Pulses controlling transistors MCi in the charge pump with CVD-PMOS.

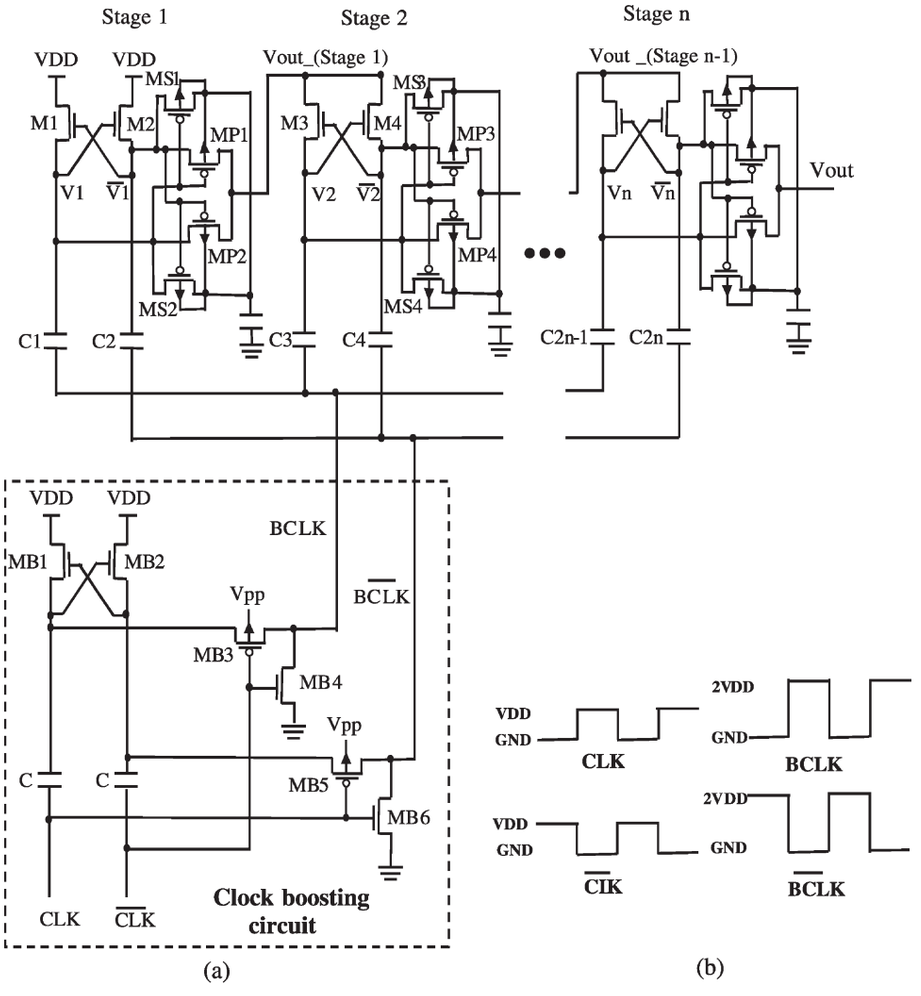

FIGURE 6 (a) The proposed charge pump with the cascade voltage doublers and the boosted clock circuitry (charge pump with CVD-BCLK). (b) Clock and boosted clock pulses.

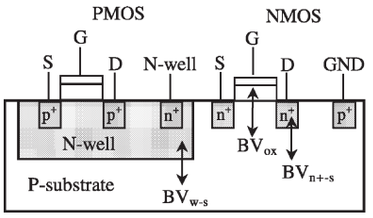

FIGURE 7 Cross section of the PMOS and NMOS transistor.

$BV_{ox} = BV_{n+-s} = 9.5\,V$. Also since the *n*-well of the PMOS transistors is tied in the highest voltage between source and drain, the pn junction formed by the *n*-well/*p*-substrate is inversely biased. However, the breakdown voltage between *N*-well/*p*-substrate is very high ($BV_{w-s} = 30\,V$) to cause any reliability problem.

The proposed charge pump with CVD along with the two improved versions, are compared with the MOS Dickson and the NCP-2 charge pump. For the charge pump with CVD-PMOS, the additional PMOS transistors are inserted only in the fourth and fifth stage, where the NMOS transistors present significantly reduced driving capability. The pumping capacitor values in all the charge pumps are 3pF. Figures 8–11 present the output voltage for different numbers of pumping capacitors and power supply voltages. The output current loading is 1.5 uA in all cases. From these figures it is obvious that the charge pump with CVD presents higher voltage gain when compared with the two other circuits, for all the power supply voltages and for any number of pumping capacitors.

Figures 10 and 11 indicate that for very low power supplies (1.2 and 0.9 V) the charge pump with CVD-PMOS and the charge pump with CVD-BCLK result in significant increase of the pumping gain, while the performance of the rest charge pump circuits is limited for large number of pumping stages. More specifically, the charge pump with CVD-PMOS can achieve a 0.9–4 V voltage generation, while for the same power supply the

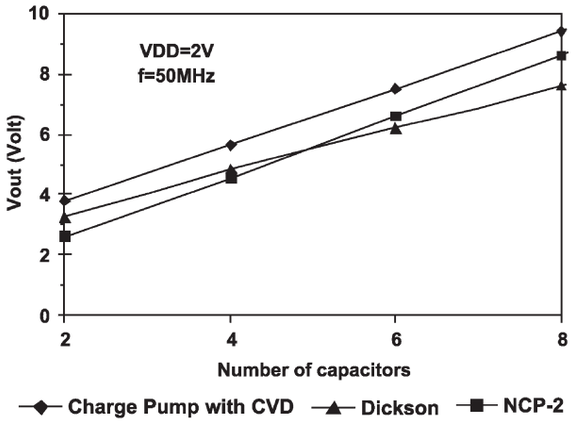

FIGURE 8 Simulated output voltages against the number of the pumping capacitors for VDD = 2 V.

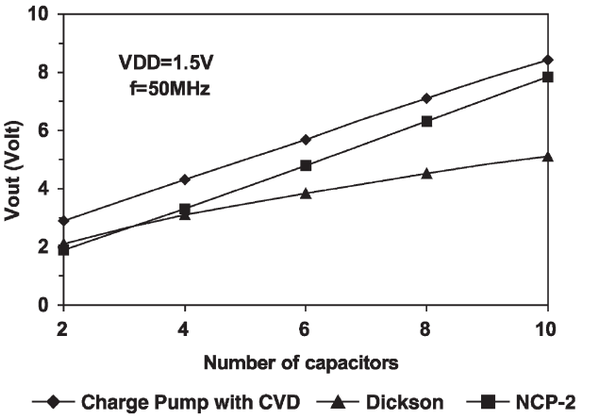

FIGURE 9 Simulated output voltages against the number of the pumping capacitors for VDD = 1.5 V.

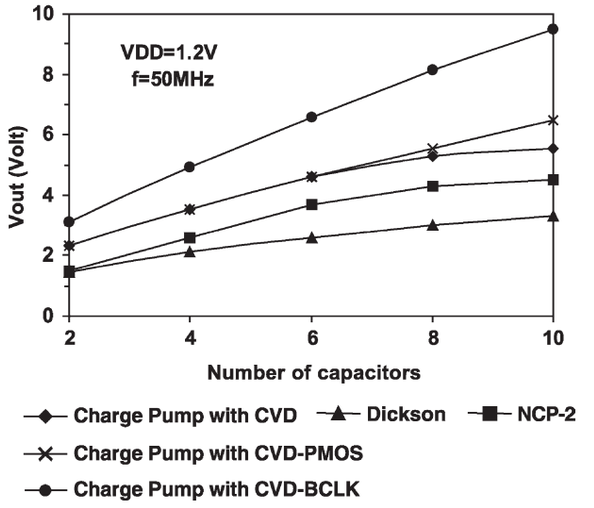

FIGURE 10 Simulated output voltages against the number of the pumping capacitors for VDD = 1.2 V.

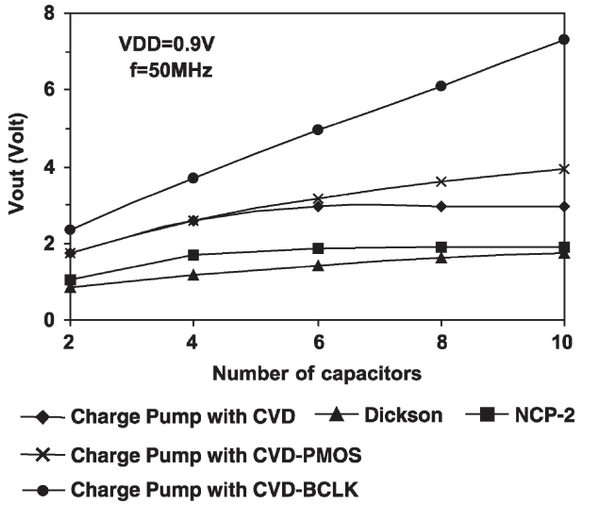

FIGURE 11 Simulated output voltages against the number of the pumping capacitors for VDD = 0.9 V.

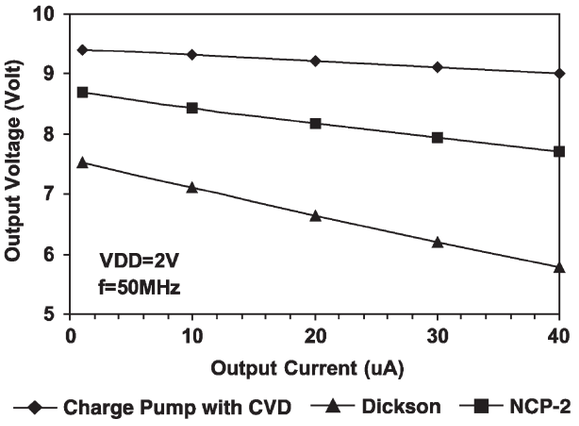

FIGURE 12 Simulated output voltages against the output current for VDD = 2 V.

output voltage of the charge pump with CVD-BCLK can reach 7.3 V.

Figures 12–15 show the output voltage for different values of output current. All the charge pumps are using eight pumping capacitors. For the same output current the proposed charge pump circuits can generate much higher output voltages compared with the Dickson and the NCP-2 charge pump. Also the superiority of the charge pump with CVD-PMOS and with CVD-BCLK is obvious even for large output currents.

CONCLUSION

A low-voltage, high performance charge pump circuit is presented. Each pumping stage consists of an improved version of the voltage doubler, with the cross-connected NMOS transistors. The resulting charge pump with cascaded voltage doublers (charge pump with CVD), outperforms the Dickson and the NCP-2 charge pump with the same number of pumping capacitors. For very low-voltage operation, two additional versions are proposed to overcome the limited, due to body effect, behaviour of the cross-connected NMOS transistors. In the first scheme PMOS transistors are inserted in parallel with the cross-connected NMOS transistors, to enhance their conductivity (charge pump with CVD-PMOS). The second version utilises a clock boosting circuit to increase the clock amplitude for driving the pumping capacitors. Simulations at 50 MHz have shown that the charge pump with CVD can achieve a 2–9.4 V and a 1.5–8.4 V voltage conversion. Also by using the charge pump with CVD-PMOS and the charge pump with CVD-BCLK an output voltage of 4 and 7.3 V can be generated from 0.9 V, respectively.

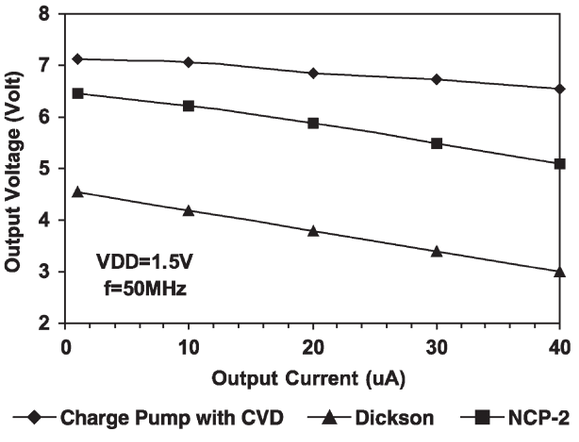

FIGURE 13 Simulated output voltages against the output current for VDD = 1.5 V.

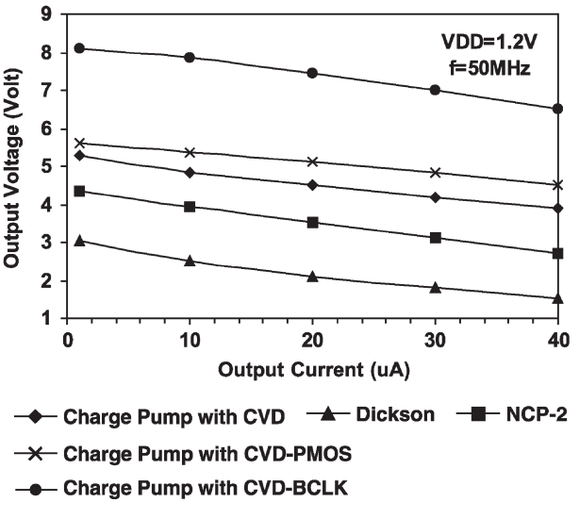

FIGURE 14 Simulated output voltages against the output current for VDD = 1.2 V.

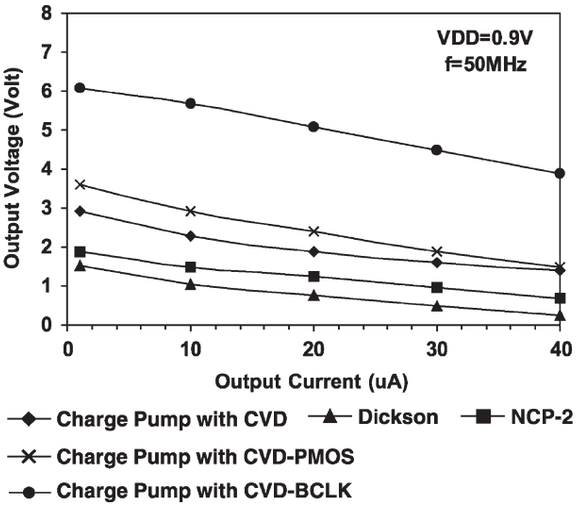

FIGURE 15 Simulated output voltages against the output current for VDD = 0.9 V.

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