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Efficient Implementation of a Demultiplexer Based on a Multirate Filter Bank for the Skyplex Satellites DVB System

MARCO RE*, ANDREA DEL RE† and GIAN CARLO CARDARILLI‡

Department of Electronic Engineering, University of Rome, Via del Politecnico 1, Rome, Italy

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In this paper, an extensive comparison among alternative algorithms for the implementation of a digital demultiplexer has been carried out. The computational complexity, the performances and the accuracy with respect to the quantization effects (quantization noise and coefficient quantization) have been evaluated for the different algorithms. The selected digital architecture has been designed to be compliant with the Eutelsat specifications for the Skyplex Digital Video Broadcast (DVB) television system (Re, M., Cardarilli, G.C., Del Re, A. and Lojacono R. (2000) "FPGA Implementation of a Demux based on a multirate filter bank". *International Symposium on Circuits and Systems 2000*, **5**(May), 353–356). At present, a more expensive and complex analog structure, based on six Surface Acoustic Wave (SAW) filters, is used. The new digital architecture has been mapped on six Altera Flex 10K-100 devices. The final test bed, that includes a complete interface to the demodulator, has been implemented on a four-layers PCB.

Keywords: Filter bank; Demultiplexing; Digital communication; Satellite; Filter; FPGA

INTRODUCTION

Improving performance of communication systems requires more sophisticated processing algorithms. This request is more evident in high challenging sectors as wireless communication and satellite applications. In these systems, new signal processing algorithms are used to obtain different advantages: device flexibility, better exploitation of the frequency spectrum, improving of service quality and reliability, are among the most important. Of course, the above objectives are achieved taking into account the application dependent system constrains, including device complexity and cost, power consumption, speed and design re-usability.

An interesting problem, in wireless and satellite applications, is the frequency demultiplexing. In fact, the massive exploitation of spectrum resources requires the reduction of bandwidth and of the transmission power for each channel, as well as the reduction of channel guard bands. Moreover, in different applications, dynamic frequency allocation is desired in order to cover different service types (requiring quite different data rates and bandwidth), as for example in software radio based systems [7].

The basic device in channel demultiplexing is the filter bank. Its task is the channels separation and its performance can be evaluated in terms of speed, selectivity, introduced distortions, complexity, weight and power consumption. In the past, filter banks have been implemented by using analog components, for example, a set of Surface Acoustic Wave (SAW) filters. This solution is effective in the case of analog post-processing of the signals at the demultiplexer output, because it does not require any analog to digital conversion. Nowadays, the high flexibility required for communication systems imposes the replacement of the analog processing with the digital one. Consequently, SAW based solution does not give the required integration and flexibility characteristics.

In this paper, a fully digital filter bank implementation is presented. It is based on the polyphase–multirate approach [1–6,9], that guarantees a good compromise among speed, complexity and filtering performance. The final architecture has been obtained evaluating different

*Corresponding authorE-mail: marco.re@ieee.org
†E-mail: delre@ing.uniroma2.it
‡E-mail: g.cardarilli@ieee.org

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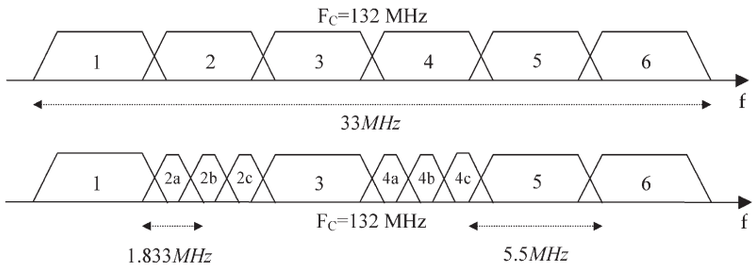

FIGURE 1 Example of signal bandwidth allocation.

solutions proposed in the literature. These architectures have been analyzed and compared, the results are then discussed in the paper.

SYSTEM SPECIFICATIONS

The system specifications of the implemented multirate filter bank, obtained from Refs. [11–13], are listed in the following:

- The input signal (transmitted in the *Ku* Band Fc = 12 GHz) is composed by 6 TV channels using the MPEG format.
- Each channel is Quadrature Phase Shift Keying (QPSK) modulated. Square Root Raised Cosine filters with roll-Off factor of 0.35 are used to limit the inter-symbol interference.
- The bandwidth of each main channel is 5.5 MHz.
- Two types of channels are supported:
  - low-Rate channel (bit-rate = 2.292 M bit/s)
  - high-Rate channel (bit-rate = 7.333, 6.875 or 6.111 M bit/s).

Any channel can be configured as single high-rate, or as up to 3 low-rate channels. In this case, the carriers are 1.833 MHz spaced each other. An example of band allocation is shown in Fig. 1.

In the first sketch, the input signal is composed by 6 high-rate channels; in the second, channel 2 and 4 are splitted in 3 low-rate channels.

- The prototype filter is characterized by 40 dB of attenuation and a maximum pass-band ripple of 0.7 dB. The −1 dB bandwidth must be larger than 4.8 MHz, the −3 dB bandwidth greater than 5.2 MHz and the −40 dB bandwidth must be less than 6 MHz. Moreover, its phase response is linear.
- The maximum imbalance among input channels is fixed at 12 dB.
- The output signal is real and allocated on a 3.667 MHz carrier.
- The SNR of the input signal is Eb/No = 10.6 dB.

The used demodulator unit [10] recognizes the kind of the input channel and is able to process the low-rate channel to obtain three single channels.

ANALOG FRONT END

The use of digital filter banks instead of the analog counterpart in FDM systems imposes the use of very high performance analog to digital converters. In fact, severe limitations for conversion speed and resolution are imposed by the large signal bandwidth and by the channel imbalance specification. In the application studied in this paper, the bandwidth of the signal to be converted is 33 MHz. Moreover, analysis and simulation results showed that 10 bits for the converter resolution are required for matching the system specification. Unfortunately, due to the current space technology limitations, we cannot convert the input signal directly at the Intermediate Frequency (IF) stage (at present, space qualified ADC with a sampling rate of, at least, 66 MHz and a precision of 10 bits are not available). Consequently, two different solutions have been studied to overcome this problem, either reducing the signal bandwidth. The corresponding architectures are illustrated in the following sections.

Complex Sampling Solution

The first solution is based on the complex sampling down-conversion scheme whose structure is shown in Fig. 2.

The I and Q components of the signal are extracted by using an analog pre-processing section based on a double down-conversion. In the first stage, the input signal is down-converted from RF = 12 GHz to IF = 600 MHz and then from IF to the Base-Band (*BB*) frequency. The I and Q components have half the bandwidth of the input signal. Consequently, the sampling frequency can be reduced to 33 MHz.

The complex sampling solution is critical for different reasons [8]. The first reason is related to the tolerance of the *π-hybrid* component of the analog section, that induces a phase drifting. This shifting introduces a phase error in the I and Q components. Moreover, the two channel output may not have the same amplitude gain, and

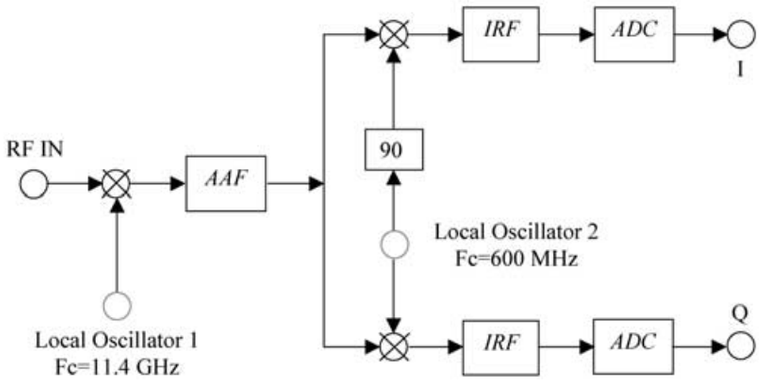

FIGURE 2 Complex sampling block diagram.

finally, timing errors in the I and Q sampling worsen the overall performance. These effects generate an image signal which can limit the dynamic range of the receiver. Moreover, they are not easy to control because of their dependence on temperature and aging. For the above reasons this solution has been discarded.

From this figure, it can be easily noted that, after the sampling, the sub-band $B1$ is mirrored with respect to the origin. In order to reconstruct the correct spectrum, it is sufficient to apply a phase shift of π. This operation can be easily implemented in hardware, corresponding to a multiplication by $(-1)^n$.

Real Sampling Solution

The block diagram of the real sampling structure is sketched in Fig. 3.

Two SAW filters with a bandwidth of 16.5 MHz are used to separate the input signal in two parts. The output signals are composed by 3 channels with a total bandwidth of 16.5 MHz. The analog to digital conversion is performed after the filtering section, reducing the sampling frequency (in principle only 33 MHz are required). Moreover, it is possible to choose an IF value corresponding to an integer multiple of the sampling rate. This allows to sample the IF signal, obtaining a simpler analog structure, with respect to the complex sampling one. The input analog signal (a) and the two output sampled signals (b) and (c), whose spectrum is indicated as $B1$ and $B2$, are shown in Fig. 4.

System Considerations

The demultiplexer presented in this paper, will be used in a hostile environment (satellite application). To avoid problems related to the complex down-conversion scheme, the real sampling solution has been chosen and the architecture shown in Fig. 3 has been used. This architecture requires 2 ADCs, instead of 6 used in the present analog realization of the frequency demultiplexer. Moreover, the RF section of the proposed architecture is simplified with respect to either the classic double down-conversion scheme and the complex sampling solution.

In the proposed system, the IF is 132 MHz and the sampling frequency Fs is 44 MHz (IF = 3Fs). The SAW filters central frequency Fc1 and Fc2 are 148.5 and 115.5 MHz, respectively. As the bandwidth of each sub-band is 16.5 MHz, we have a 4/3 oversampling factor.

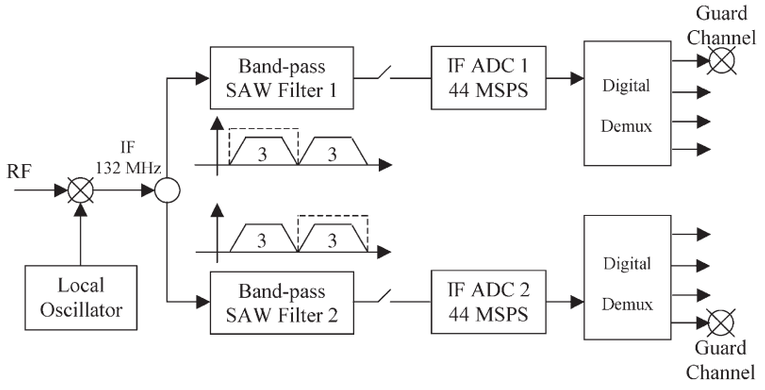

FIGURE 3 Real sampling architecture.

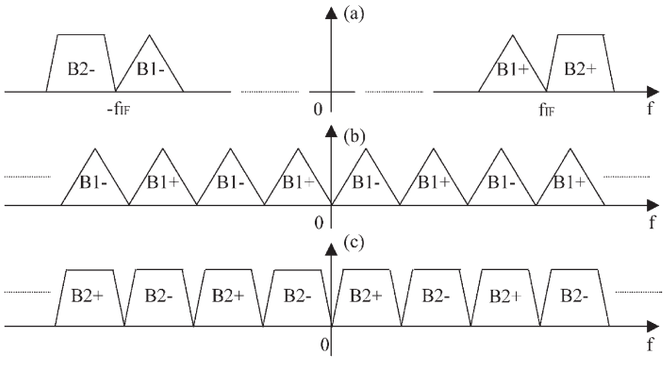

FIGURE 4 Real sampled signal.

This choice gives an output signal composed by 3 useful channels and a guard channel. The 2 ADCs sample at a higher frequency (44 MHz) with respect to the analog implementation (14.667 MHz). In spite of that, a considerable reduction in the power consumption is however obtained due to the use of only 2 ADCs (6 are necessary in the analog implementation).

ALGORITHMS ANALYSIS AND CHARACTERIZATION

In order to find the best solution for the implementation of the digital demultiplexer, the following three algorithms have been compared in term of quantization noise effects, performance and computational complexity:

1. Polyphase + Inverse Discrete Fourier Transform (IDFT) filter bank (*PFB*).
2. Tree-oriented complementary half-band filter bank (*CTFB*).
3. Tree-oriented polyphase filter bank (*PTFB*).

In the next sections, the above structures are analyzed and their computational complexities are evaluated in terms of number of real multiplications (Multiplication Per Unit or *MPU*) and of real additions (Additions Per Unit or *APU*) needed to obtain a single output sample.

Polyphase and IDFT Filter Bank (*PFB*)

As it is well known, polyphase filter banks process complex signals. The full bandwidth of the input signal $0 \div 2\pi$ is divided into M parts, where M is the number of channels. This means that the positive part of the input signal frequency spectrum will be separated from its negative image. An example is sketched in Fig. 5.

As the incoming signal is composed by 4 real channels with a bandwidth of 11 MHz, we have designed a 8 channels polyphase filter bank. Its output will be composed by 8 complex channels with a bandwidth of 5.5 MHz, but only the first 3 channels are used. The others are not connected.

The polyphase + IDFT filter bank architecture is illustrated in Fig. 6. The $E_i(z)$ filters are obtained from the prototype filter by applying the polyphase decomposition:

$$H(z) = \sum_{k=0}^{M-1} z^{-k} E_k(z^M) \tag{1}$$

$$e_k(n) = h(nM + k) \;\; 0 \le k \le M - 1 \tag{2}$$

where $h(n)$ is the impulse response of the prototype filter, $H(z)$ is its Z-transform and $e_k(n)$ are the coefficients of the k-th polyphase filter. The prototype filter is band-pass and its bandwidth is 5.5 MHz. The inputs of the polyphase components $E_i(z)$ are obtained by delaying the incoming signals of a single sample, and then decimating them by a factor equal to the number of channels [2,14].

An 8-point IDFT and a multiplication by a factor of 8 are performed to reconstruct the filtered signals. In fact, the reconstruction formula for polyphase filter

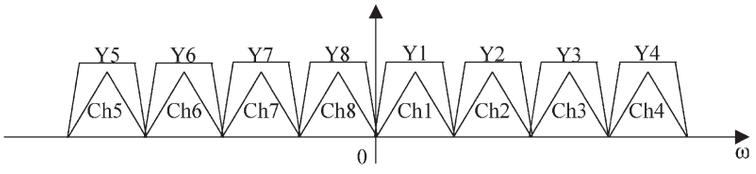

FIGURE 5 The polyphase + IDFT filter bank processing.

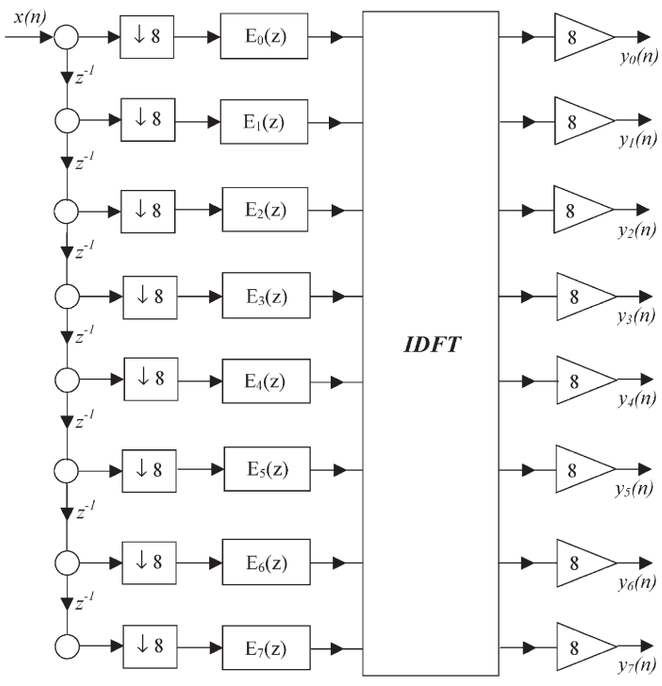

FIGURE 6 Polyphase filter bank architecture.

banks is:

$$H_\alpha(z) = \sum_{n=0}^{M-1} W^{-\alpha n} z^{-n} E_n(z^M) \tag{3}$$

which corresponds to the IDFT formula, except for the $1/M$ factor. The output signal is a complex BB signal, with a sample rate of 5.5 MSamples/s.

Polyphase Filter Bank Complexity

If N_T is the number of taps of the prototype filter, each polyphase component has $N_{Tp} = N_T/M$ taps ($M = 8$ is the number of channels to be considered in our case). If the length of the input sequence is L_S, the length of the sub-sequences processed by each polyphase filter is $L_{Sp} = L_S/M$. Consequently, the number of real multiplications in order to process L_S input samples is:

$$N_{Mf} = 2L_{Sp}N_{Tp}M = 2L_SN_{Tp} \tag{4}$$

where the factor 2 is needed because the prototype filter is complex, and the factor M is needed because we have M polyphase filters.

The number of real additions is given by:

$$N_{Af} = 2L_{Sp}(N_{Tp} - 1)M = 2L_S(N_{Tp} - 1) \tag{5}$$

since we have $2{\cdot}N_{Tp}$ partial results from the multipliers.

The IDFT complexity (number of real multiplications N_{Mi} and additions N_{Ai}) is described by the following equations:

$$N_{Mi} = 4M^2L_{Sp} = 4ML_S \tag{6}$$

$$N_{Ai} = 2M(2M - 1)L_{Sp} = 2(2M - 1)L_S \tag{7}$$

Finally, the total number of *MPU* and *APU* is given by the following equations:

$$MPU = \frac{N_{Mf} + N_{Mi}}{L_S} = 2(N_{Tp} + 2{\cdot}M) \tag{8}$$

$$APU = \frac{N_{Af} + N_{Ai}}{L_S} = 2[(N_{Tp} - 1) + (2M - 1)] \tag{9}$$

Complementary Half-band Filter Bank (*CTFB*)

The complementary half-band tree-oriented filter bank architecture is shown in Fig. 7. The input sequence is sent to two complementary real filters, a low-pass filter H_0 and a high-pass filter H_1, with a cut-off frequency at the half of the Nyquist frequency ($\pi/2$) [2]. The complementary filters have the same number of taps. At the filter output the signal bandwidth results divided by 2 and, consequently, the sequences can be decimated by the same factor without any loss of information. This process can be iterated as many times as needed (2 in our case). The bandwidth of the output signals is a $1/2^n$ portion of the bandwidth of the input one.

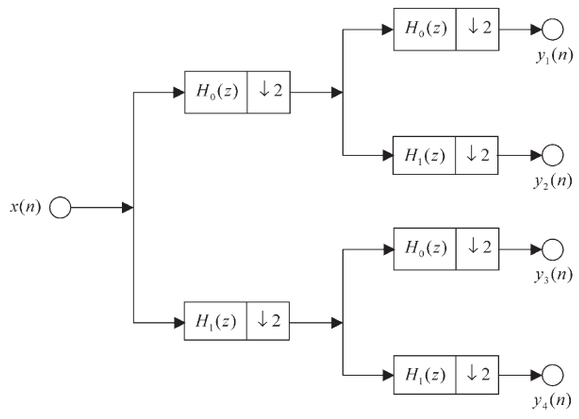

FIGURE 7 Tree-oriented complementary half-band filter bank architecture.

The output signal is real, centered on 2.75 MHz, and its sample rate is 11 MSamples/s.

CTFB Complexity

Reminding that for the tree-oriented CTFB we have $M = 4$ (real channels), and using the same notations as in "Polyphase filter bank complexity" section, we obtain the following expressions for the *MPU*:

$$MPU = \frac{1}{4N_S}\sum_{i=1}^{K} 2^i \frac{N_S}{2^{i-1}} N_T = \frac{1}{2} N_T \log_2 M \tag{10}$$

where $K = log_2\ M$ is the number of stages, 2^i is the number of filters at the i-th stage and $N_S/2^{i-1}$ is the sequence length at the i-th stage. The factor 1/4 is obtained from the following considerations. The filters have a linear phase response and, consequently, the taps are symmetrical ($h(n) = h(n - N + 1)$). Moreover, the half-band filters have half of the taps equal to 0.

As for each sample of the input signal N_T partial results are generated by each filter, we can obtain for the number of *APU*:

$$APU = \frac{1}{2N_S} N_S (N_T - 1)\log_2 M$$
$$= \frac{1}{2}(N_T - 1)\log_2 M \tag{11}$$

Tree-oriented Polyphase Filter Bank (*PTFB*)

The PTFB architecture is shown in Fig. 8. The input signal is routed in two paths where the signal sequences are decimated and then filtered by using the corresponding polyphase component filters, obtained from the prototype low-pass half-band filter [2].

To restore the correct output signals a 2 point IDFT × 2 are performed. These operations are equivalent to calculate the following expressions:

$$Y_0(n) = \mathrm{Out}_1(n) + \mathrm{Out}_2(n) \tag{12}$$

$$Y_1(n) = \mathrm{Out}_1(n) - \mathrm{Out}_2(n) \tag{13}$$

where Out_1 and Out_2 are the polyphase filter output sequences. The output signal is a real signal, centered at 2.75 MHz and its sample rate is 11 MSamples/s.

PTFB Complexity

Starting from the results obtained for the complementary half-band structure, it is easy to calculate the number of *MPU* and *APU* needed in the polyphase half-band filter bank. In fact, if we note that the length of the sequence at the i-th stage is $N_S/2^i$ and that we use a polyphase decomposition of factor of 2 (the number of filters at the

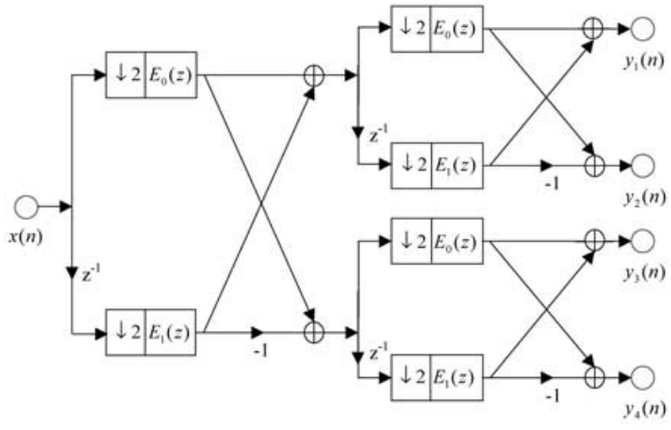

FIGURE 8 Tree-oriented polyphase filter bank architecture.

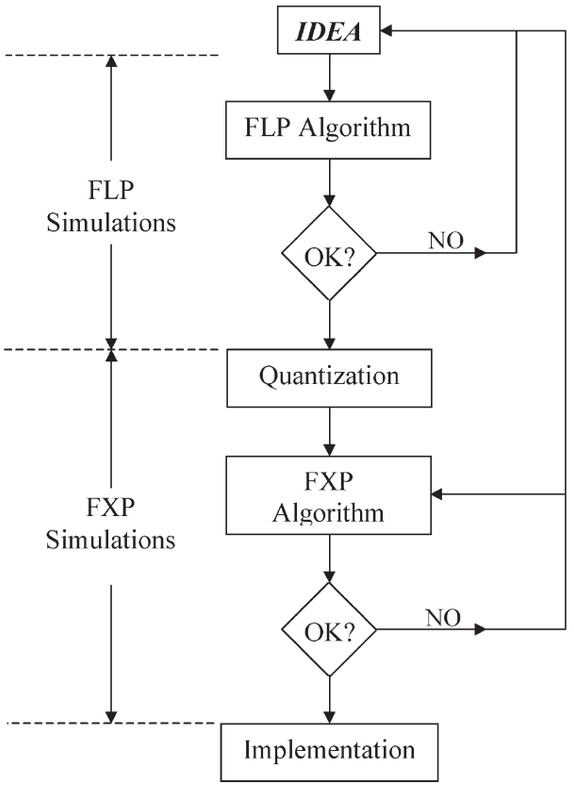

FIGURE 9 Typical DSP algorithm design flow.

i-th stage is $2^{(i-1)}$), we can obtain:

$$MPU = \frac{1}{4N_S}\sum_{i=1}^{K} 2^{i-1}\frac{N_S}{2^i}N_T = \frac{1}{8}N_T \log_2 M \qquad (14)$$

$$APU = \frac{1}{N_S}\sum_{i=1}^{K} 2^{i-1}\frac{N_S}{2^i}\frac{N_T - 1}{2}$$

$$= \frac{1}{4}(N_T - 1)\log_2 M \qquad (15)$$

In the last equation, we have considered that, to implement half the number of taps, exploiting the taps symmetry, we need to sum the input samples two by two, before they enter into the filter.

FIXED POINT (FXP) ANALYSIS

The floating point (FLP) to FXP translation is one of the most important design steps in the optimal implementation of complex Digital Signal Processing systems. The actual and future portable multimedia applications, characterized by low-power requirements, very high throughput, shorter development time, higher complexity of the embedded DSP algorithms, make the use of FXP arithmetic more and more important.

TABLE I Prototype filter parameters

	PFB 8 ch	*CTFB* 4 ch	*PTFB* 4 ch
Filter Att.	47.5	47.3	47.3
BW −1 dB (MHz)	5.24	21.74	21.74
BW −3 dB (MHz)	5.38	21.88	21.88
BW −40 dB (MHz)	5.91	22.4	22.4

Consequently, while area and speed has been the most used cost functions to characterize DSP architectures, in the last few years, a lot of research work has been done to study architecture transformations aimed to lower the power consumption [15,16]. Another important research topic related to the power consumption is the wordlength optimization for FXP implemented algorithms.

The typical DSP algorithm design flow is sketched in Fig. 9. A FLP version of the algorithm is implemented firstly. A first refinement loop is usually necessary to choose the right algorithm and successively, a FXP implementation is developed. If its performance does not match the system requirements, a modification of the number of bits used to represent the variables or a change of the algorithm structure can be effected. This successive refinement process is very costly in term of simulation time and, where possible, a mixed theoretical and simulative approach is used for the evaluation of the dynamic range (number of integer bits) and of the quantization noise (number of fractional bits) [17].

In the demultiplexer design, a number of simulations has been carried out to validate the chosen algorithms and to define the number of bits needed to avoid saturation (number of bits for the integer part), to match the SQNR requirements (number of bits of the fractional part) and to match the frequency specification (filter mask, i.e. number of bits for the coefficients). FLP and FXP models of the demultiplexer have been developed for each of the three selected structures. Comparing the results obtained by using the FLP and FXP models the Signal to Quantization Noise Ratio (SQNR) has been evaluated. It has been proved, by simulation, that 12 bits are necessary in all the three structures to avoid saturation and to match the SQNR requirements, while 13 bits used for coefficients representation permits to match the constraint imposed by the filter mask.

The design of the prototype FIR filter, i.e. number of taps and coefficient definition, has been carried out by

TABLE II Output signals characterization

	PFB 8 ch	*CTFB* 4 ch	*PTFB* 4 ch
Ripple *H* (dB)	0.055	0.084	0.069
Ripple *L* (dB)	0.221	0.218	0.228
Ripple *M* (dB)	0.102	0.197	0.096
SQNR *H* (dB)	52.43	57.56	56.07
SQNR *L* (dB)	40.03	45.59	44.54
SQNR *M* (dB)	46.11	50.86	49.98

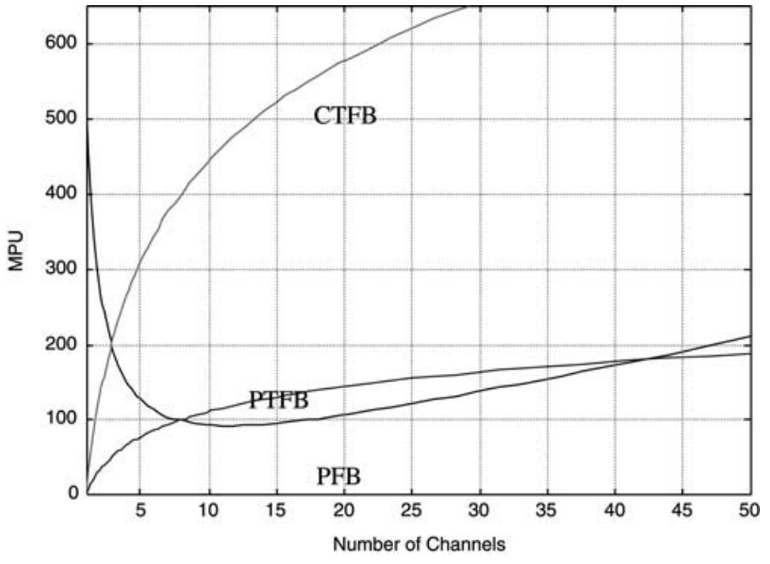

FIGURE 10 *MPU* versus the number of channels.

using the Matlab Signal Processing Toolbox. The final prototype filter requires 267 taps and is Blackman windowed.

PERFORMANCE COMPARISON

The performance comparison of the proposed algorithms has been carried out by characterizing the prototype filters and the demultiplexer output signals (obtained by stimulating the demultiplexer input with a signal whose spectrum emulates a raised cosine filtered QPSK spectrum). The parameters used for the prototype filters are: attenuation, -1, -3 and -40 dB bandwidth. The values obtained by FXP simulations are shown in Table I. For the output signals, the following quality factors have been taken into account: ripple on the maximum (H), minimum (L), medium (M) level channels and signal to quantization noise ratio, measured comparing the FXP results with the FLP ones. The results are shown in Table II.

Tables I and II show similar performance for the proposed algorithms, with the exception of the polyphase filter bank which results more sensible to the quantization noise.

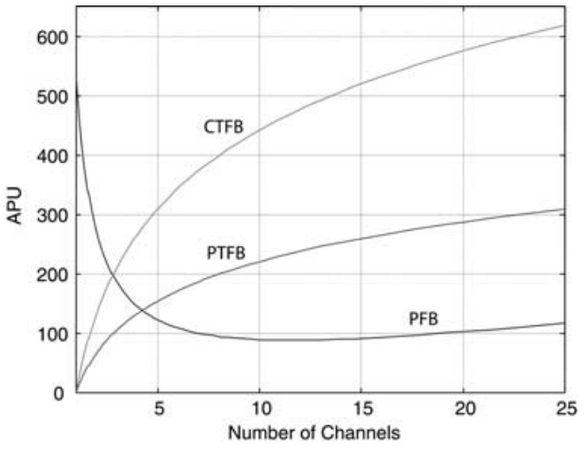

FIGURE 11 *APU* versus the number of channels.

COMPUTATIONAL COMPLEXITY COMPARISON

Another fundamental parameter in the comparison of the proposed architectures, is their computational complexity. Its evaluation has been carried out in terms of *MPU* and *APU* samples, i.e. the number of multiplications and additions to be performed to obtain an output sample from the system. Figure 10 shows the number of *MPU* versus the number of channels for the different architectures.

From the analysis of Fig. 10, the *PTFB* and the *PFB* architectures result more advantageous with respect to the *CTFB* one. In particular, the *PFB* architecture appears the most efficient for $8 \leq M \leq 41$. Nevertheless, considering that we work with real signals, the number of channels to be processed in the *PFB* structure is double with respect

TABLE III Multiplications per unit

Algorithms	*MPU* Expr.	*MPU*
PP 8 ch.	$2(N_{Tp} + 2M)$	98.75
HB 4 ch.	$1/2N_T \log_2 M$	267
PT 4 ch.	$1/8N_T \log_2 M$	66.75

TABLE IV Additions per unit

Algorithms	*APU* Expr.	*APU*
PP 8 ch.	$2[(N_{Tp}-1)+(2M-1)]$	94.75
HB 4 ch.	$1/2(N_T-1)\log_2 M$	266
PT 4 ch.	$1/4(N_T-1)\log_2 M$	133

to the *PTFB* solution. Comparing the computational complexity with the above assumption, the *PFB* architecture results more efficient for $8 \leq M \leq 12$.

In Fig. 11, the number of *APU* for the three architectures are shown. The obtained shapes are similar to *MPU* ones.

Starting from the expressions obtained in "Algorithms analysis and characterization" section, the values of *MPU* and *APU* for the three selected architectures has been computed and the results are shown in Tables III and IV, where M is the number of channels, N_T the number of taps of the complementary filters and of the prototype filter for the tree-oriented demultiplexers and $N_{Tp} = N_T/M$ is the number of taps of the polyphase filter.

The analysis of Tables III and IV shows that (for the number of channels of our application) the best implementation corresponds to the polyphase tree-oriented filter bank. In fact, the last architecture requires 39 more additions but the saving of 32 multipliers with respect to the polyphase filter bank gives a global advantage.

RATE CONVERTER DESIGN

Taking into account that the Skyplex demodulator requires as input a real signal centered at 3.667 MHz and characterized by a sample rate of 14.667 MSamples/s, none of the previously discussed filter bank architectures show a direct compatibility with this demodulator.

In particular, the output signal of the selected architecture (*PTFB*) is characterized by a sample rate of 11 Msps, and it is modulated with a carrier of frequency 2.75 MHz. In order to make it compatible with the Skyplex demodulator, a rate converter has been designed. Due to the fact that the same rate converter must be used for all the three proposed architectures, we do not take into account its computational complexity in the algorithm comparison. Note that, for the *PFB* architecture small modifications in the rate converter are required (a shift factor of $e^{j\pi/6}$ instead of $e^{j\pi/24}$, an output interpolator by a factor of 2 and a complex to real conversion) but its architecture presents substantially the same complexity of the other ones.

Block Diagram

The rate converter block diagram is shown in Fig. 12. The interpolation factor is 4/3 (= 14.667/11), $H(z)$ represents a complex 357 taps band-pass anti-aliasing filter. Moreover the shift factor $e^{j\pi/24}$ is required to center the signals at the right frequency $f_c = 3.667$ MHz for the compatibility with the Skyplex demodulator as previously discussed. In Fig. 12, bold arrows and lines mean that the signal is complex.

The structure of the rate converter shown in Fig. 12 is not optimized from the computational complexity point of view; in fact the working frequency of the filter $H(z)$ is $4 \cdot 11 = 44$ MHz. To lower the computational complexity noble identities 1 and 2 [2] has been used (Fig. 13).

In the following subsections, the three steps needed to minimize the rate converter implementation complexity are illustrated.

Minimum Complexity Realization

The block diagram shown in Fig. 12 is modified first by moving the decimation block before the anti-aliasing filter $H(z)$ (Noble Identity 1). The result is shown in Fig. 14 where $E_i(z)$ represent the polyphase components of the anti-aliasing filter, obtained from Eqs. (1) and (2).

The second step to lower the computational complexity is based on the Noble Identity 2. This property permits to move the interpolation block after the polyphase components of the anti-aliasing filter. This operation will be effected for the three signal paths (Fig. 14). The result for $E_0(z)$ branch is shown in Fig. 15. The $R_{0i}(z)$ filters corresponds to the polyphase components of the $E_0(z)$ filter.

The result for the $E_1(z)$ branch is shown in Fig. 16. The $R_{1i}(z)$ filters are the polyphase components of the $E_1(z)$ filter.

The result for $E_2(z)$ branch is shown in Fig. 17. The $R_{2i}(z)$ filters are the polyphase components of the $E_2(z)$ filter.

The final architecture is obtained by adding the sequences coming from the three branches. The resulting structure, obtained by rearranging the delays, is shown in Fig. 18B, while in Fig. 18A the rate converter block diagram is replicated. The complex filters referred as R_{xx}, work at $11/3 = 3.667$ MHz (instead of $11 \times 4 = 44$ MHz as in the scheme of Fig. 12). The number of taps of each R_{xx} filter is $N_{Tp} = 357/3 \cdot 4$.

FIGURE 12 Rate converter block diagram.

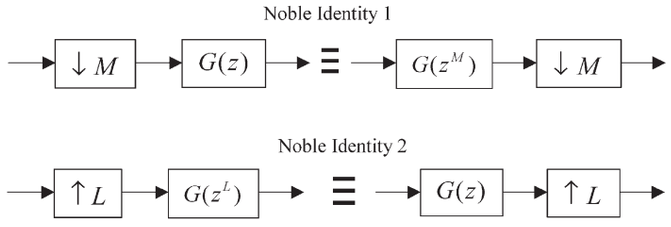

FIGURE 13 Noble identities exemplification.

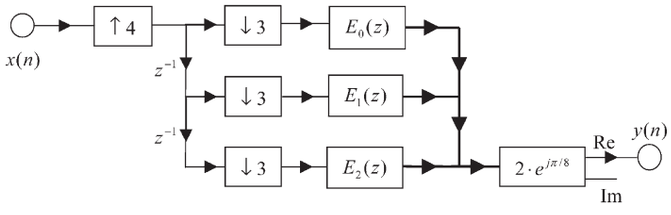

FIGURE 14 Polyphase decomposition: first step.

As we need a real signal at the input of the Skyplex demodulator, and taking into account that a frequency shift factor $e^{j\pi n/8}$ must be implemented (Fig. 18B), the two operation can be mixed and simplified by using the following expression:

$$Re(\text{Out}) = Re(\text{In})\cdot Re(e^{\frac{j\pi n}{8}}) - Im(In)\cdot Im(e^{\frac{j\pi n}{8}}) \qquad (16)$$

The number of used multipliers is 2. The coefficients $e^{j\pi n/8}$ shows a periodicity of 16 and are stored in a circular shift register.

PROTOTYPE IMPLEMENTATION

For the test bed, a prototype board, based on 6 Altera Flex 10K-100 FPGAs, has been implemented. The necessity of the FPGA based test bed is related to the difficulty to obtain a Bit Error Ratio (BER) characterization by software simulations (too long simulation time). The board block diagram is shown in Fig. 19. The analog input signal is sampled by using a CLC5956 ADC by National Semiconductor (12 Bit, 65MSPS). The input mux is required because, in the test bed, a single rate converter

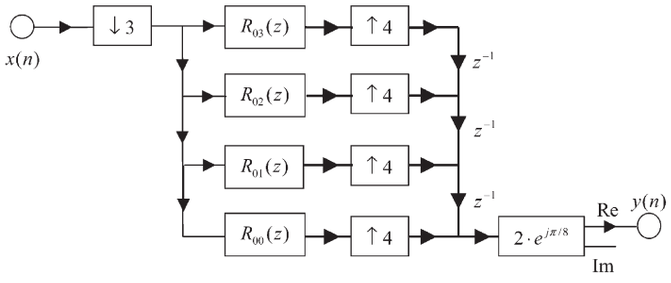

FIGURE 15 Polyphase decomposition: second step—First branch.

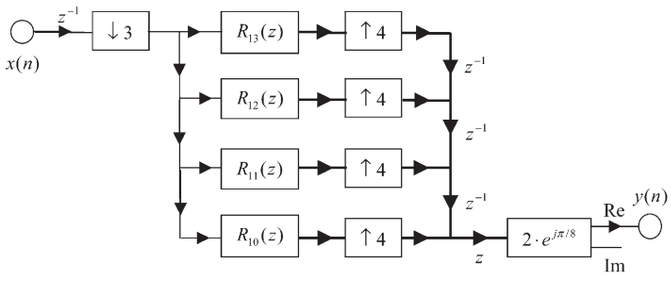

FIGURE 16 Polyphase decomposition: second step—Second branch.

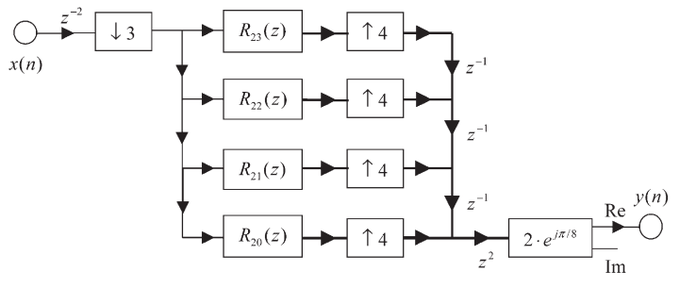

FIGURE 17 Polyphase decomposition: second step—Third branch.

has been implemented. The output mux is required to route, to the Skyplex demodulator, the rate converter output signal or a test signal.

The test can be decomposed in the following main blocks:

1. Clock Generation and Timing (Timing block).
2. Filtering (Half-Band 1,2,3 blocks).
3. Rate Converter (Rate Converter 1,2,3 blocks).
4. Multiplexers.

In Fig. 20 the schematic diagram is shown. In the following subsections, a short description of each block will be given.

Clock Generation and Timing Section

A high stability reference clock, with a frequency of 14.667 MHz is provided by the used demodulator [10]. The demultiplexer clock is derived from that provided by the demodulator by using a Philips

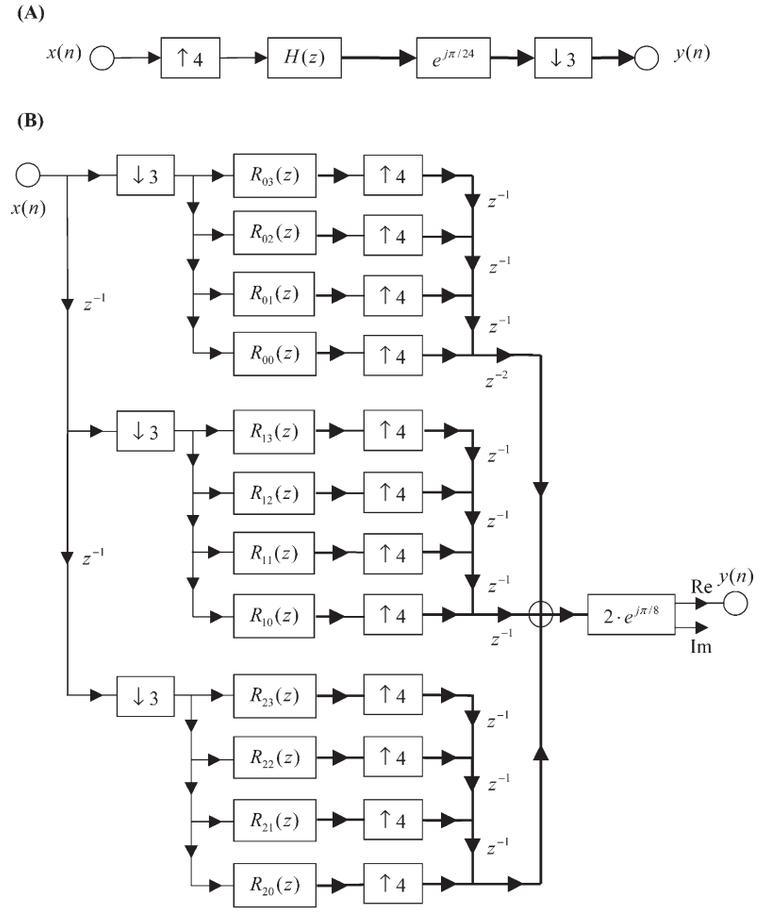

FIGURE 18 Rate converter.

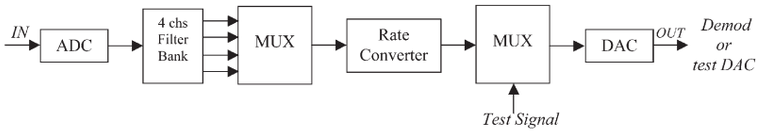

FIGURE 19 Prototype board block diagram.

74HC7046AD PLL circuit and a custom 44 MHz VCXO. By using a PLL based timing architecture, the clock signals are generated with a minimum skew. Altera 7160 PLD and a Motorola MPC930 (Low voltage PLL based clock driver) provide clocks needed for the different architectural sections. They are listed in the following:

- 44 MHz clock to the ADC.
- 22 MHz clock to the *PTFB* first stage filters and to the *PTFB* second stage decimators.
- 14.667 MHz clock to the DAC (useful in the rate converter test phase) and to the frequency shifter at the output of the rate converter.
- 11 MHz clock to the output DAC (useful in the *PTFB* test phase) and to the *PTFB* second stage filters.
- 3.667 MHz clock to the rate converter input decimators.

Filtering Section

The *PTFB* architecture shown in Fig. 8 has been implemented by using 3 Altera Flex10K-100 TQFP240 FPGAs: one is used for the first stage and the other two for the second stage. Due to the limitations of the selected devices in terms of Logic Elements (LE), only a significant subset (137 over 267) of the taps of the designed filters is implemented. In that way, exploiting the half-band filter properties, we need only 32 constant coefficient multipliers to implement the filter section; these multipliers have been fitted in a single device, with an occupation of almost 60% of the available LEs. Matlab simulations have evaluated the degradation of the

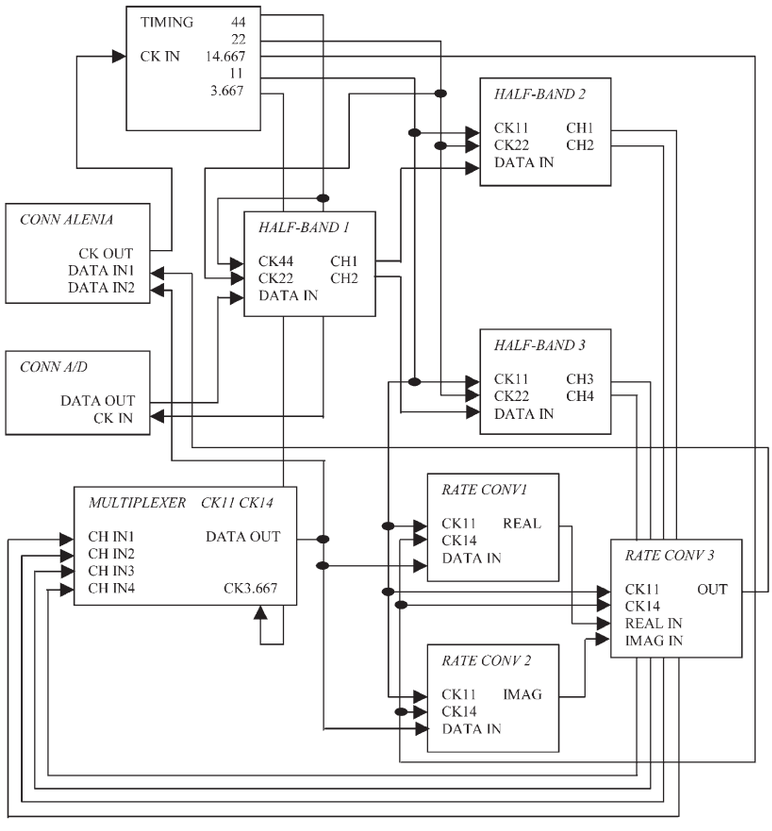

FIGURE 20 Prototype board sections interconnect diagram.

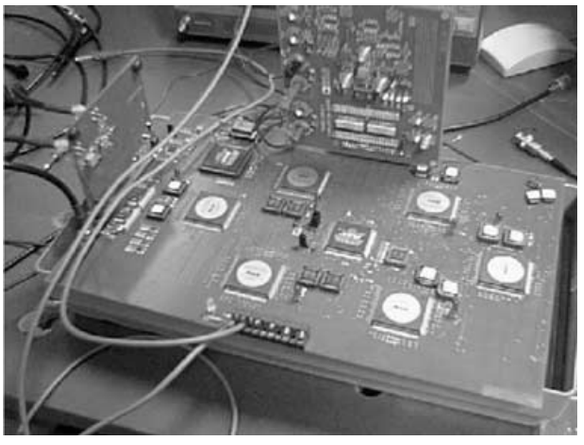

FIGURE 21 Prototype board.

performance previously. The results obtained from the prototype measurements match the simulation results.

Rate Converter Section

A single rate converter with a subset (157 out of 357) of the designed taps has been implemented by using 3 Altera Flex10K-100 TQFP240 FPGAs. Starting from the architecture shown in Fig. 18, the anti-aliasing filter is divided into three sections working in parallel. Each section is composed of by 12 polyphase filters, with 13 taps in each one. The number of multipliers used for that structure is 39 and the overall occupation is near the 75% of the available LEs. As in the case of the filter bank, the performance degradation has been previously evaluated with Matlab simulations and a good matching with the prototype measurements has been obtained.

Multiplexers

Two multiplexers are added to the design. The first one is used to select which filter bank output must be routed to the input of the rate converter. The second one is used to select which (the test signal or the rate converter output) will be routed to the output. Both the multiplexers have been implemented using an Altera 8452 QFP160 device.

Board Implementation

The polyphase half-band filter bank architecture has been mapped on 3 FPGAs Altera Flex 10K-100. In order to achieve a full compliance with the used demodulator a rate converter/frequency shifter module has been designed and mapped on 3 Altera 10K-100 FPGAs. The final test bed, consisting of 6 FPGAs, has been implemented on a four-layers Printed Circuit Board (PCB), which is shown in Fig. 21.

The demux board has been interfaced to the analog section by using two evaluation boards (CLC-5956 EVB For the A/D conversion stage and the Analog Devices AD 9762-EVM, 12 bit 100 MSPS, for the D/A conversion stage).

CONCLUSIONS

The aim of this work has been the selection of an efficient architecture, (in terms of power consumption and performance) for a digital demultiplexer according to the system specifications for the Skyplex DVB system. The digital demultiplexer will replace its analog version used, at present, in the Hot Bird satellites [10].

In this paper, alternative algorithms for the implementation of a multirate filters banks has been described. The comparison has been carried out for the selected architectures by developing three different simulation models: FLP, FXP and bit true. Based on the simulation results the polyphase tree oriented filter bank architecture has been chosen. The final test bed has been implemented on 6 Altera 10K-100 FPGAs. As a further step, the integration of the demultiplexer and of the demodulator on a single ASIC is planned.

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Marco Re received the Laurea degree in Electronic Engineering from the University of Rome, La Sapienza in 1991 and the Ph.D. in Microelectronics and Telecommunications Engineering from the University of Rome, "Tor Vergata" in 1996. In 1998 he joined the Department of Electronic Engineering of the University of Rome, "Tor Vergata" as researcher. He was awarded two one-year NATO fellowships with the University of California at Berkeley in 1997 and 1998. At present, he is a visiting researcher at the Cadence Berkeley Laboratories and at the University of California at Berkeley. His main interests and activities are in the area of DSP algorithms, fast DSP architectures, Fuzzy Logic hardware architectures, Hardware–Software Codesign, number theory with particular emphasis on Residue Number System, computer arithmetic and Cad tools for DSP.

Andrea Del Re received the Laurea degree in Electronic Engineering from the University of Rome "Tor Vergata" in May 1999. From November 1999 he is a Ph.D. student at the Department of Electronic Engineering, University of Rome, "Tor Vergata". In July 1999 he was awarded one-year fellowship with the Coritel consortium. His main interests and activities are in the area of Fast Prototyping, hardware for DSP, Filter Bank and Residue Number System.

G.C. Cardarilli was born in Rome, Italy, in 1956 and received the laurea (summa cum laude) in 1981 from the University of Rome, La Sapienza. He works for the University of Rome, "Tor Vergata" since 1984. Actually he is professor of Digital Electronics at the University of Rome, "Tor Vergata". During the years 1992–1994 he worked for the University of L'Aquila. During the years 1987/1988 he worked for the Circuits and Systems team at EPFL of Lausanne (Switzerland). Prof. Cardarilli interests are in the area of VLSI architectures for Signal Processing and IC design. In this field he published over than 80 papers in international journals and conferences. He also participated to the work group of JESSI-SMI for the support to the medium and small industries. For this structure he consulted different SMI's, designing a number ASIC's, in order to introduce the microelectronics technology in the industry's products. He is also a regular consultant for Alenia Aerospazio, Rome, Italy. Scientific interest of Prof. Cardarilli concerns the design of special architectures for signal processing. In particular, he work in the field of computer arithmetic and its application to the design of fast signal digital processor. He also developed mixed-signal neural network architectures implementing them in silicon technology. Recently, he also proposed different new solutions for the implementation of high-speed fuzzy-logic processors, oriented to the signal and image processing.